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Topical Review

Materials, processes, devices and applications of magnetoresistive random access memory

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Abstract

Magnetoresistive random access memory (MRAM) is a promising non-volatile memory technology that can be utilized as an energy and space-efficient storage and computing solution, particularly in cache functions within circuits. Although MRAM has achieved mass production, its manufacturing process still remains challenging, resulting in only a few semiconductor companies dominating its production. In this review, we delve into the materials, processes, and devices used in MRAM, focusing on both the widely adopted spin transfer torque MRAM and the next-generation spin-orbit torque MRAM. We provide an overview of their operational mechanisms and manufacturing technologies. Furthermore, we outline the major hurdles faced in MRAM manufacturing and propose potential solutions in detail. Then, the applications of MRAM in artificial intelligent hardware are introduced. Finally, we present an outlook on the future development and applications of MRAM.

Keywords: spin transfer torque-magnetoresistive random access memory (STT-MRAM), spin-orbit torque (SOT) MRAM, materials for MRAM, field-free writing of SOT-MRAM, MRAM process, artificial intelligence

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1. Introduction

Magnetoresistive random access memory (MRAM) is a novel form of non-volatile memory that distinguishes itself from traditional semiconductor memories by utilizing the spin state of electrons rather than their charge property for information storage. This unique characteristic grants MRAM several advantages, including rapid read and write speeds, low power consumption, and non-volatility. Furthermore, MRAM exhibits nearly infinite endurance, scalability, and compatibility with complementary metal-oxide-semiconductor (CMOS) technology. Consequently, the emergence of MRAM holds the potential to replace static random-access memory (SRAM) and dynamic random-access memory (DRAM), thereby mitigating interconnect delays among memory devices and reducing overall power consumption.

Due to the numerous advantages offered by MRAM, renowned technology companies worldwide have undertaken extensive research and development efforts, leading to remarkable achievements. In 2003, the international business machines corporation (IBM) introduced an MRAM product renowned for its high speed, low power consumption, and high endurance. Major semiconductor companies, such as Everspin, IBM, Samsung, and Intel, have also made significant investments in MRAM research and manufacturing. In 2006, Freescale started to ship toggle-MRAM chips with 4 Mb. However, the capacity is difficult to scale up (current chips are limited to 64 Mb) due to the architecture of its memory cell. Besides, Honeywell and Cobham also launched toggle-MRAM products but used for aerospace. Notably, in 2016, Everspin became the first to offer a 256 Mb spin transfer torque (STT)-MRAM product to customers. In 2018, Global foundries launched its first STT-MRAM based on the 22 nm FinFET process. In 2019, Samsung introduced the industry's first embedded STT-MRAM product based on the 28 nm FDSOI process. During the 2022 international electron devices meeting (IEDM) conference, Samsung announced the advancement of its MRAM technology to the 14 nm FinFET process level. In 2022, Everspin launched a MRAM product family with serial peripheral interface (SPI)/ Quad SPI/ Extended SPI interface ranging from 8 Mbit up to 64 Mbit. These products are targeted for use in industrial IoT and embedded systems applications. As MRAM manufacturing technology continues to mature and market demand expands, more companies are entering the MRAM field, accelerating the expansion of MRAM's application scenarios.

Currently, as shown in figure 1, MRAM finds applications primarily in the military and aerospace as a standalone memory. In outer space environments, traditional semiconductor devices can be susceptible to single-particle flip effects caused by various forms of space radiation, leading to undesired alterations in the logical state of the devices. However, MRAM exhibits remarkable resistance to high levels of radiation and can function reliably under extreme temperature conditions. Moreover, low power consumption characteristic of MRAM aligns well with the requirements of long-distance space missions. Furthermore, owing to its unparalleled advantages in power consumption, speed, and durability, MRAM is viewed as an ideal storage device for constructing logic-in-memory architectures. In the future, MRAM is expected to find applications in various scenarios, including microcontroller units (MCUs) and cache, enabling the provision of enhanced services to human society.

This article offers a comprehensive overview of the research advancements of principles, materials, devices, manufacturing processes and artificial intelligence applications of both STT-MRAM and spin-orbit torque (SOT)-MRAM. Previous reviews had described the progress of MRAM mainly on the theory, materials, devices [1–3] and performances [4]. As the MRAM is in the way toward industry, we place particular emphasis on the MRAM manufacturing and highlight the collaborative efforts undertaken by academy and industry community to tackle challenges of the manufacturing. Lastly, the article presents a forward-looking perspective on the future development of MRAM.

2. Manufacture of STT-MRAM

2.1. Introduction of STT-MRAM

STT-MRAM is a novel form of non-volatile memory that utilizes electrical current to read and write data, which is stored in a magnetic tunneling junction (MTJ) [1], as depicted in figure 2(a). The MTJ consists of a layered structure comprising a ferromagnetic/insulator/ferromagnetic stack. The ferromagnetic layer with a lower coercive force is referred to as the free layer, while the other layer is known as the reference layer. The resistance of the MTJ is determined by the relative orientation of the magnetization in these two magnetic layers. Typically, the MTJ exhibits a low-resistance state when the magnetization of the two layers are parallel, whereas it shows a high-resistance state when they are not aligned. The tunneling magnetoresistance ratio (TMR) is defined as follows [2]:

$$TMR = \frac{R_{AP} - R_P}{R_P} \times 100\% \qquad (1)$$

where R_{AP} and R_P stands for the high and low resistance of the MTJ, respectively. The TMR effect plays a crucial role in evaluating the quality of an MTJ device. Its underlying principle can be easily understood with reference to figure 2(b) [3]. Electrons with a specific spin can tunnel from one ferromagnetic layer to another through a thin insulating layer. In the parallel state, electrons with a majority spin in the first ferromagnetic layer can readily tunnel to the neighboring ferromagnetic layer, occupying majority energy states. This configuration leads to a low resistance state. Conversely, in the antiparallel state, electrons with majority and minority spins from the first ferromagnetic layer occupy the minority and majority energy states of the adjacent ferromagnetic layer, respectively. Consequently, a high resistance state is observed.

To control the switch between the two aforementioned states, the magnetic field generated by a large current was

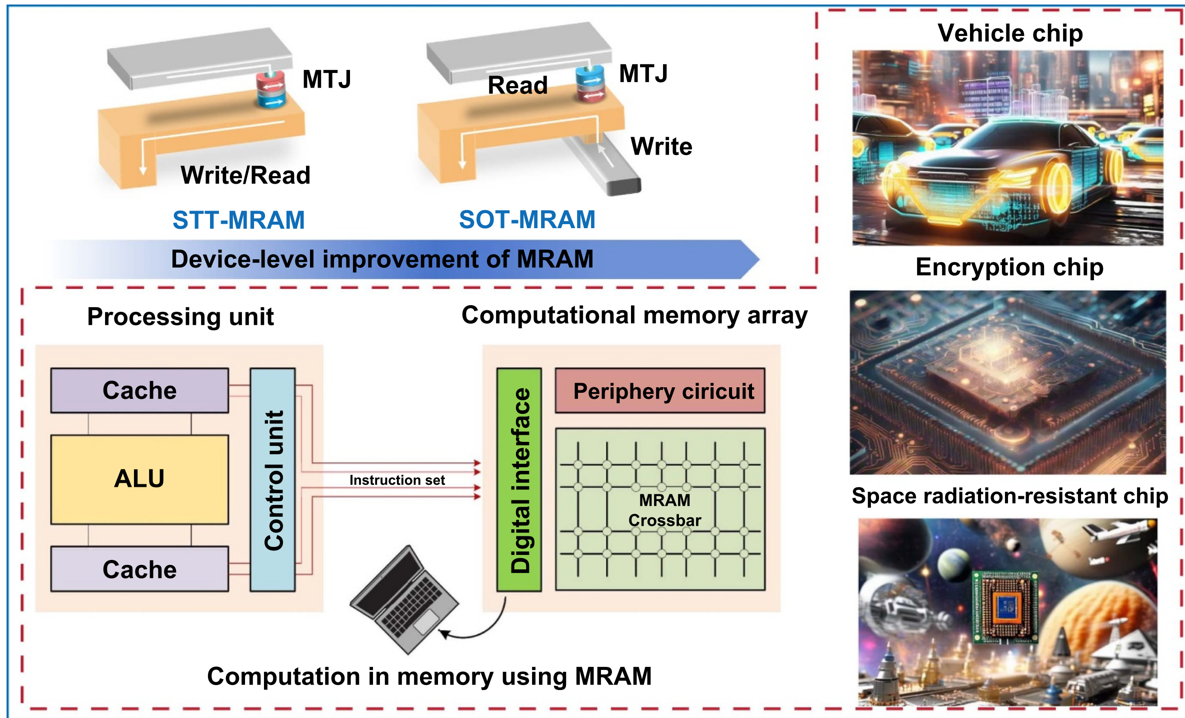

Figure 1. The device structure and application scenarios of STT-MRAM and spin-orbit torque (SOT) MRAM, respectively.

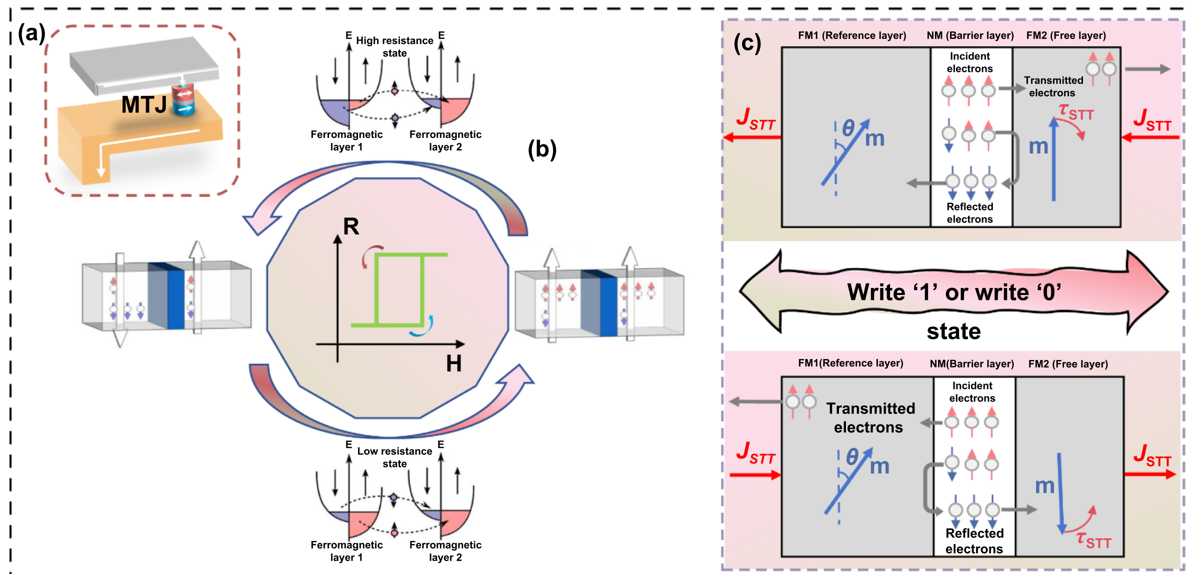

Figure 2. The principle of STT-MRAM. (a) The memory cell and write operation of STT-MRAM. Reproduced from [1], with permission from Springer Nature. (b) The tunneling magnetoresistance (TMR) effect of STT-MRAM. Reproduced from [3]. © IOP Publishing Ltd. All rights reserved. (c) The schematic diagram of STT effect [5].

initially employed. However, in 1996, Slonczewski at IBM proposed spin-transfer-torque writing [4], which significantly reduced the necessary current.

2.2. The mechanism of spin-torque switching

As depicted in figure 2(c) [5], to write the low resistance state of the MTJ, a current passes through the MTJ from the free layer to the reference layer. Initially, the spin of the electrons aligns with the magnetization direction of the reference layer. Subsequently, the spin-polarized current exerts a torque on the magnetization of the free layer. If the current is sufficiently strong, it can switch the magnetization of the free layer to align parallel to the reference layer. Conversely, to write the high resistance state of the MTJ, a current passes through the MTJ from the reference layer to the free layer. The electrons with spins anti-parallel to the magnetization direction of the reference layer are reflected into the free layer. If the reflected

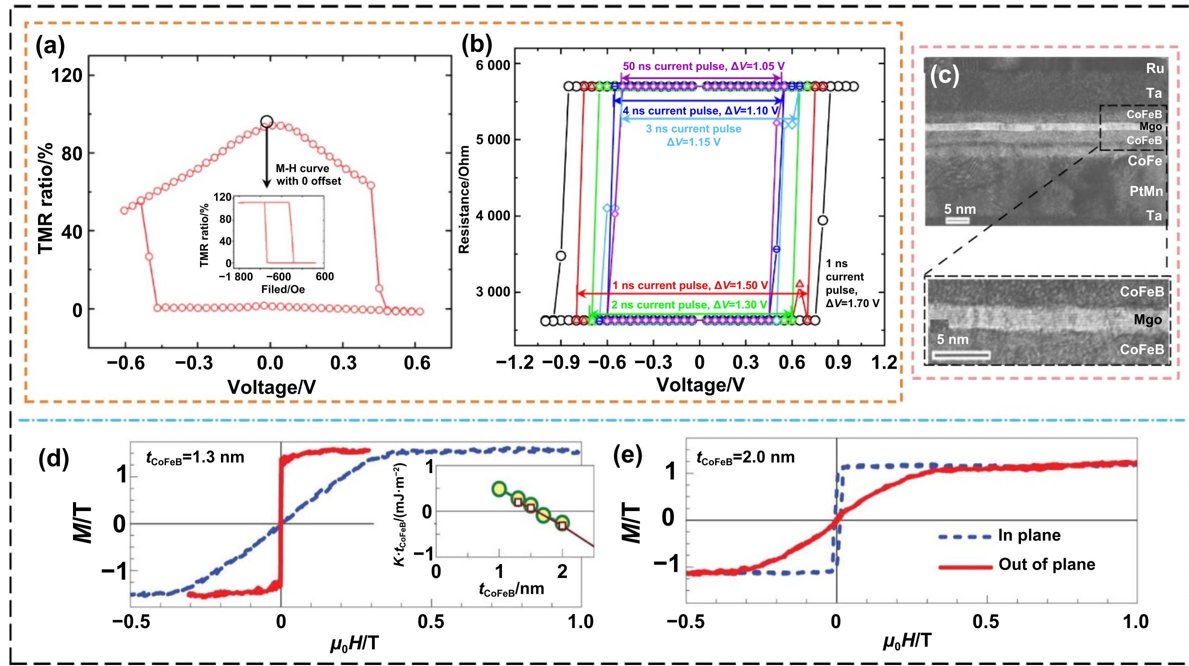

Figure 3. The electrical characteristics of STT-MRAM. (a) and (b) The static and dynamic electrical characteristic of STT-MTJ. (c) The cross-section HRTEM image of CoFeB/MgO/CoFeB MTJ. Reprinted from [14], with the permission of AIP Publishing. (d) and (e) In-plane and out-of-plane magnetization curves for CoFeB/MgO with (d) $t_{\mathrm{CoFeB}} = 1.3$ nm and (e) $t_{\mathrm{CoFeB}} = 2$ nm, respectively [15]. Reproduced from [15], with permission from Springer Nature.

current is of sufficient magnitude, it can flip the magnetization of the free layer in the anti-parallel direction to the reference layer.

The dynamic process of magnetization flipping can be described by the Landau-Lifshitz-Gilbert (LLG) equation [6]:

$$\frac{\partial \boldsymbol{m}}{\partial t} = -\gamma\mu_0 \boldsymbol{m}\times\boldsymbol{H}_{\mathbf{eff}} + \alpha \boldsymbol{m}\times\frac{\partial \boldsymbol{m}}{\partial t} - \frac{\gamma\hbar JP}{2et_{\mathrm{F}}M_{\mathrm{S}}}\boldsymbol{m}\times(\boldsymbol{m}\times\boldsymbol{m}_{\boldsymbol{r}}) \tag{2}$$

where $\boldsymbol{m}$ and $\boldsymbol{m_r}$ stand for the magnetization vector of free layer and reference layer, respectively. $\boldsymbol{H_{eff}}$ stands for the effective magnetic field, γ stands for the gyromagnetic ratio, μ_0 is the permeability of vacuum, α is Gilbert damping constant, $\hbar$ is the reduced Planck constant, e is the charge of electron, P is the spin polarization, t_{F} is the thickness of free layer, M_{S} is the saturated magnetization of the free layer, and J is the bias current density. The last term in equation (2) represents the STT, which opposes the damping term. When the STT term is smaller than the damping term, the magnetization of the free layer undergoes precession for a certain period and eventually returns to its initial equilibrium state. However, when the STT term exceeds the damping term, the magnetization of the free layer processes for a duration and flips to another equilibrium state. The current at which the magnetization undergoes flipping is referred to as the critical switching current.

From the equation (2), one can determine that the static critical switching current density at $T = 0$ K takes the form as described in [7, 8]:

$$J_{c0} = \frac{2e\alpha M_{\mathrm{S}}t\,(H_K + H_{\mathrm{eff}} + 2\pi M_{\mathrm{S}})}{\hbar g} \tag{3}$$

where H_K is anisotropy field strength of free layer and g is STT efficiency factor that is related to the spin polarization of the input current. The LLG equation is also utilized to describe the dynamic behavior when the input current surpasses the critical switching current, and the duration of the current pulse is very short (less than 10 ns). In this case, the magnetization flipping occurs in the precessional regime. The pulse width and input current exhibit the following relationship [9]:

$$t_p = \frac{I_{C0}}{\alpha M_{\mathrm{S}}\,(I_{\mathrm{mtj}} - I_{C0})\,\gamma}\ln\left(\frac{\pi}{2\theta_0}\right) \tag{4}$$

where, $\theta_0 = \sqrt{\frac{k_BT}{2E_B}}$ and E_B represent the anisotropy energy barrier for MTJ. Equation (4), known as Sun's model, describes the deterministic switching process. It can be observed that the input current (I_{mtj}) is inversely proportional to the pulse time. Figure 3 illustrates the standard electrical characteristics of an STT-MTJ device.

On the other hand, the thermal effect gives rise to the stochastic switching of the magnetization in the free layer. The probability of switching is described by Neel–Brown's model [10–13]:

$$P_{SW} = 1 - \exp\left\{-\frac{t_p}{\tau_0}\exp\left[-\frac{E_B}{k_BT}\left(1-\frac{I}{I_{C0}}\right)\right]\right\} \tag{5}$$

where τ_0 is the inverse of the attempt frequency that equals to 10^{-9} s. Neel Brown's model is important for the design of low bit error rate (BER) MRAM circuit.

Figure 3(a) illustrates the direct current (d.c.) resistance as a function of the bias voltage, indicating that the resistance states of the MTJ can be switched by the applied current. Figure 3(b) demonstrates the alternating current (a.c.) resistance as a function of the bias pulse voltage with varying pulse widths. It shows that a shorter pulse duration leads to a higher required writing voltage.

2.3. Material development of STT-MRAM

The development of materials for MTJ devices is a crucial aspect of STT-MRAM research. The first demonstrations of STT-induced switching with MTJ devices were carried out by Huai *et al* in 2004 using AlO_x-based MTJ [16] and in 2005 using MgO-based MTJ [17–19]. In AlO_x-based MTJ, the TMR is only around 70%–80% at room temperature due to the amorphous aluminum oxide tunnel barrier. The lack of crystallographic symmetry in the amorphous barrier allows electrons with different spin polarization to tunnel through, resulting in low spin polarization. In contrast, when the barrier is crystalline, the tunneling process is governed by crystal symmetry. In MgO (001)-based MTJ, only the Bloch state of electrons with spherical symmetry ($\Delta 1$) can tunnel through the barrier [20]. The $\Delta 1$ state in Fe (001) is fully spin polarized, with a spin polarization value (P) of 1. Therefore, it is expected that the TMR in Fe (001)/MgO (001)/Fe (001) MTJ devices will exceed 1000% at room temperature [21]. In 2004, Yuasa *et al* successfully fabricated high-quality fully epitaxial Fe/MgO/Fe MTJs using molecular beam epitaxy (MBE), which exhibited a TMR of 180% at room temperature [22]. From a microscopic perspective, the film texture of the MTJ plays a critical role in achieving high TMR values.

Indeed, Fe exhibits a high saturated magnetization and damping constant, which results in a relatively large critical switching current. In practical applications, the MTJ film is often deposited on an antiferromagnetic film or a synthetic antiferromagnetic (SyAF) film, both of which typically have a (111) texture. As a result, direct deposition of MgO (001)-based MTJs on such films is not feasible due to the symmetry mismatch between the (001) orientation of MgO and the (111) texture of the underlying layer.

To address these challenges, Djayaprawira *et al* developed CoFeB/MgO/CoFeB-based MTJ, which have achieved TMR values exceeding 200% at room temperature [14]. Figure 3(c) illustrates the as-grown state of the amorphous CoFeB layers. However, under suitable conditions, a highly textured MgO (001) film can be grown on top of it. Crucially, when the MTJ film is annealed at around 300 °C, the CoFeB layer undergoes crystallization at the interfaces with MgO (001) due to the favorable lattice matching between MgO (001) and CoFeB (001). This advantageous property allows for the growth of CoFeB/MgO/CoFeB MTJ films on various underlayers such as W and Ta. In recent years, CoFeB/MgO/CoFeB MTJ have emerged as the mainstream material used in STT-MRAM applications.

2.4. Magnetic architecture of STT-MRAM

The easy axis of STT-MRAM is a crucial factor, primarily determined by the anisotropy constant K. The anisotropy constant can be expressed as follows [15]:

$$K = K_{\mathrm{b}} - \frac{M_{\mathrm{S}}^2}{2\mu_0} + \frac{K_{\mathrm{i}}}{t} \tag{6}$$

where K_{b} is the bulk crystalline anisotropy, K_{i} is the interfacial anisotropy, $\frac{M_{\mathrm{S}}^2}{2\mu_0}$ is the demagnetization which originates from shape anisotropy and t is the thickness of CoFeB film. When $\frac{K_{\mathrm{i}}}{t} > \frac{M_{\mathrm{S}}^2}{2\mu_0}$, CoFeB film exhibits perpendicular magnetic anisotropy (PMA) which means the easy axis is perpendicular to the film [23]. When $\frac{K_{\mathrm{i}}}{t} < \frac{M_{\mathrm{S}}^2}{2\mu_0}$, CoFeB film exhibits in-plane magnetic anisotropy (IMA). Currently, the easy axis direction of an STT-MRAM depends on the shape of the MTJ [23]. As depicted in figure 3(d), H. Ohno *et al* have provided comprehensive experimental evidence, demonstrating that when the thickness of the CoFeB layer is less than 1.5 nm, it exhibits PMA. Conversely, as depicted in figure 3(e) [15], it exhibits IMA.

Based on equations (7) and (8), one can calculate the static critical switching current for both the IMA-MTJ and the PMA-MTJ,

$$I_{\mathrm{C0}}^{\mathrm{IMA}} = \frac{2\alpha e\mu_0}{\hbar g}\left(2E_B + 2\pi M_{\mathrm{S}}^2 V\right) \tag{7}$$

$$I_{\mathrm{C0}}^{\mathrm{PMA}} = \frac{2\alpha e\mu_0}{\hbar g}\left(2E_B\right). \tag{8}$$

It is evident that the critical switching current of the IMA-MTJ is higher than that of the PMA-MTJ for the same energy barrier. As a result, the mainstream adoption favors the use of PMA-MTJs.

The typical structure and key parameters of a PMA-MTJ are depicted in figure 4(a) [24]. It consists of more than 30 thin film layers, with each layer having a thickness of approximately 1 nm. The structure includes a synthetic antiferromagnetic (SyAF) pinned layer, a reference layer, a barrier layer, and a free layer. Notably, there is a ferromagnetic coupling between the SyAF pinned layer and the reference layer, which sources from Ruderman–Kittel–Kasuya–Yosida (RKKY) interaction [25]. The SyAF pinned layer enhances the stability of the reference layer to prevent spontaneous switching during write operations. It is crucial to design the thicknesses of the reference layer and the SyAF pinned layer appropriately to minimize the stray field that acts on the free layer.

As the size of the device decreases, MTJ with a single free layer may struggle to provide adequate thermal stability. Currently, several methods are employed to optimize the thermal stability of the MTJ structure. One approach involves replacing the single CoFeB free layer with a hybrid free layer (HFL) like Pt/Co/Spacer/CFB/MgO stack. In this

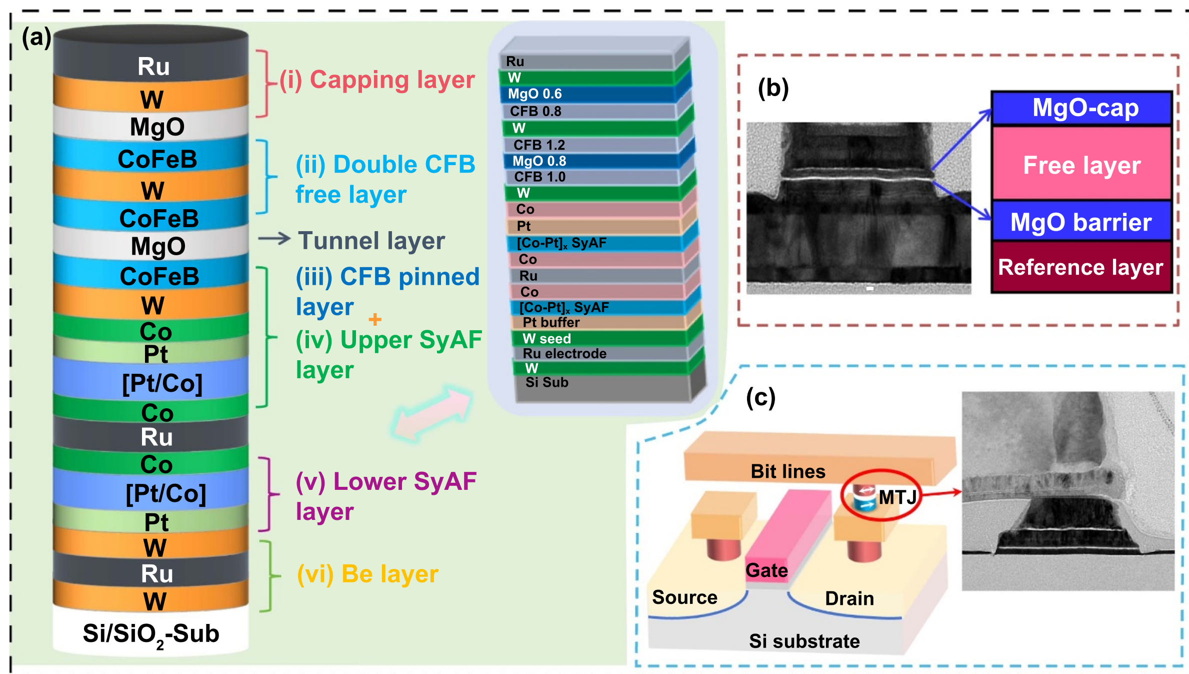

Figure 4. The typical film and physical structure of STT-MRAM. (a) The typical film stack and key film thickness of STT-MTJ [24]. (b) The structural representation and TEM cross section images for double-MTJ. (c) The schematic and TEM of structure of 1 T-1 MTJ memory cell.

configuration, the spacer material usually uses W, Y or Ta, to achieve ferromagnetic coupling between free layer (FL) 1 and FL2 by interlayer exchange coupling, and improve the crystal interface contact and electron band matching of the structure.

Figure 4(b) illustrates the structure of a multi-interface MTJ. As previously mentioned, the PMA in CoFeB/MgO/CoFeB-based MTJs originates from the interfacial anisotropy. To enhance the thermal stability, an additional MgO layer can be inserted into the CoFeB layer, with both layers sandwiched between MgO layers [26]. Careful design of the MgO film thickness is crucial to ensure that the multi-interface free layer behaves as a single ferromagnet, considering magnetostatic and exchange coupling effects. Leveraging this approach, Ohno *et al* extended the PMA-MTJ to a 3 nm scale, while still achieving high performance [27].

In 2018, Watanabe *et al* introduced a method that utilizes shape anisotropy to achieve sub-10 nm MTJ [28]. In contrast to conventional MTJ structures, the thickness of the free layer in the proposed MTJ is significantly larger than its width. As a result, the shape anisotropy axis is aligned with the z-axis. By further optimizing the shape anisotropy, Jinnai *et al* extended the IMA-MTJ to a diameter of 2.3 nm, while maintaining high performance [29].

Reducing the write power consumption of STT-MRAM is a significant research focus, and one promising approach is the use of dual MTJ. This architecture consists of a reference layer/barrier layer/free layer/barrier layer/reference layer structure. The second reference layer in this configuration provides an additional spin torque during the write process. In the antiparallel configuration of the reference layers, where the magnetization of the two reference layers is antiparallel, the spin currents from either reference layer exert torques in the same direction, effectively reducing the critical switching current by approximately 50%.

However, this structure has a drawback of reduced magnetoresistance. Since the magnetization of the two reference layers is antiparallel, one part of the MTJ is consistently in a low resistance state while the other part remains in a high resistance state. To overcome this issue, a nonmagnetic spacer layer can be used to replace the barrier layer in one part of the MTJ. Based on this concept, Hu *et al* at IBM developed a 35 nm double spin-torque MTJ with a switching time of 300 ps, demonstrating lower critical switching current compared to typical MTJ [30].

Precessional switching MTJ (Pr-MTJ) represents another approach to reduce power consumption. It is structured as follows: PMA reference layer/barrier layer/PMA free layer/IMA reference layer [2]. The PMA reference layer is responsible for resistance readout, while the IMA reference layer is utilized in the write process. During the write process, the spin torque from the IMA reference layer causes the magnetization of the free layer to tilt within the plane. This tilt induces a significant demagnetization field in the plane of the free layer. As a result, the magnetization of the free layer undergoes precession around a direction perpendicular to the free layer's easy axis. This precession greatly accelerates the flipping speed of the magnetization. Simulation studies of Pr-MTJs have demonstrated switching times of less than 50 ps, showcasing its potential for fast operation.

2.5. The reliability of STT-MRAM

Device reliability is a crucial factor that significantly impacts the application of MRAM, as issues such as write failure, read disturbance, and retention failure have posed limitations on its further development.

For the device level, write current, pulse width and thermal stability of STT-MRAM device cell are major factors for its write and read reliability. Write error occurs when the current applied to the device cell is too low to switch or the pulse width is too short to switch. More importantly, the write path and the read path of STT-MRAM is the same, the read error occurs when the write and read current is very near to each other, which is especially for the STT-MTJ with small size. The bit error probability is followed as [31, 32]:

$$P_{sw} = -\exp\{-\tau_{pw}/\tau_0 \times \exp[-\Delta(1 - I/I_{c0})]\} \quad (9)$$

where P_{sw} is the switching probability under applied current I, I_{c0} is the critical switching current at 0 K, τ_{pw} is the pulse width of applied current, τ_0 is the attempt time which is considered to be 1 ns. This plays a crucial role in determining the cell state.

On the other hand, for the circuit level, the process variation of MTJ is also an important factor for the read reliability. It is known that the TMR of MTJ is low, which leads to the small read margin of the pre-charge sense amplifier (PCSA) circuit. The resistance variation of MTJ will make the read error even worse.

In practice, the ability to retain the stored data of MRAM is limited. Retention errors occur when the temperature increases or after a certain amount time. The origin of retention errors lies in the thermal factor Δ of the free layer in the MTJ device. The STT-MRAM cell lifetime is provided as follows [33, 34]:

$$T_{life} = \frac{1}{f_0} \times \exp(\Delta) \quad (10)$$

where the Δ is the thermal factor of the free layer, f_0 is the attempt time which is 1 ns.

Regarding the above reliability issues from device level and circuit level, several works have been proposed to improve the field, such as MTJ-based variation monitor that helps to sense process variation from the device level [35, 36], error-correcting code circuit that fix the BER from the circuit level [37, 38]. Furthermore, extensive research and exploration from both academia and industry have been conducted on optimizing device read/write processes using on-chip temperature sensors based on thermal effects, optimizing drive circuits to reduce potential losses during device unit read/write processes, and improving the state of MTJ film stack to enhance the device's intrinsic anti-interference capability.

2.6. Fabrication of STT-MRAM

STT-MRAM uses a simple two-terminal MTJ device which is embeddable in the standard 400 °C CMOS back end of line (BEOL), as shown in figure 4(c). It can be fabricated with the addition of only 3–4 masks.

The process flow of STT-MRAM is illustrated in figure 5, highlighting the significance of magnetic stack deposition through magnetic sputtering. The PMA-MTJ stack consists of several layers, including the seed layer, SyAF pinned layer, reference layer, barrier layer, free layer, capping layer, and hard mask layer. Following deposition, the film undergoes annealing at temperatures ranging from 350 °C to 400 °C in vacuum. Next, the MTJ pattern is exposed using deep ultraviolet lithography (DUV) and transferred to the hard mask layer. The MTJ is then etched through the hard mask pattern. The MTJ etching process is critical and encounters two technical challenges. Firstly, metal residue may be present on the sidewalls of the MgO layer due to the relatively thick seed layer used in STT-MTJ. This metal residue can cause shorting of the MTJ device. To address this issue, ion beam etching (IBE) is employed to tilt the wafer and etch the metal residue on the sidewalls of MgO. Proper adjustment of the etching time and tilt angle is crucial. The second challenge involves achieving highly uniform patterned hard mask pillars with vertical sidewalls and excellent IBE selectivity to ensure the desired performance. Wan *et al* proposed a method to achieve an STT-MRAM array with a pitch of 50 nm, emphasizing the importance of this aspect [39].

After etching the MTJ, the inter-layer dielectric process is performed using plasma-enhanced chemical vapor deposition (CVD), high density plasma CVD, and sub-atmospheric pressure CVD techniques. The dielectric material used is a specific type of SiO_2. Subsequently, chemical mechanical polishing (CMP) is employed to polish the surface and etch back the contact at the top of the MTJ. Finally, the top metal is deposited and fabricated into a standard top electrode.

2.7. The product of STT-MRAM

The initial STT-MRAM products were mainly used in standalone memory applications, which required operating within a temperature range of 0–85 °C, sustaining read and write cycles of up to 10^{10} times, and accessing data within 30–100 ns. Several manufacturers have since launched commercial STT-MRAM products [40–43] with different storage capacities to replace double data rate (DDR) 3, among which Everspin has introduced a 1 Gbit STT-MRAM to meet the increasing storage demand of mobile devices.

On the other hand, STT-MRAM stands out as a highly promising embedded memory technology capable of replacing eFlash in nodes below 28 nm. MRAM finds typical applications in storing microcontroller code and encryption key storage. With further shrinking of the process nodes, STT-MRAM becomes a potential substitute for eFlash and SRAM due to its lower power consumption and area. Samsung [44, 45] and Taiwan semiconductor manufacturing company (TSMC) [46–48] are competing fiercely in this field. Leveraging the low-power feature of STT-MRAM, Samsung [49] and Renesas Electronics [50] have also launched non-volatile Random Access Memory (nvRAM)-type eMRAM products using 2X nm processes. In addition, Avalanche Technology

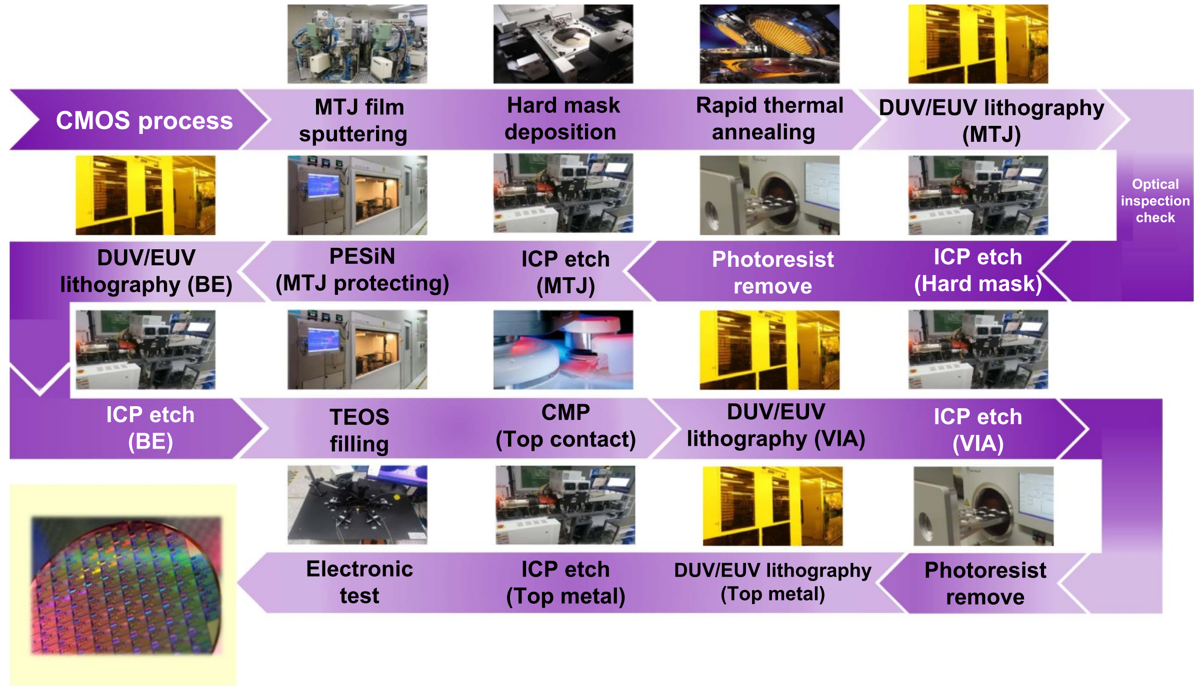

Figure 5. The BEOL process of STT-MRAM. The first vital step is the deposition of the magnetic stacks. Then the lithography and etching to form MRAM bit array aligned to contact are important for electrical performance of MTJ, such as resistance and TMR. The third step is ILD and CMP, and the last step is the top metal electrode interconnection [39].

[51] has introduced a high-capacity (8 Gbit) storage chip for aerospace applications, exploiting the radiation-hardness of STT-MRAM. To achieve higher integration density and lower energy consumption, a 1S1M structure based on selectors and STT-MRAM has been proposed and implemented on a small scale [52, 53]. Currently, TSMC, Samsung, and Global Foundries all offer eMRAM products designed for nodes at 28 nm and below. Table 1 shows the recent academic research results related to STT-MRAM and their key product parameters.

In the foreseeable future, the primary market of STT-MRAM is embedded memory. On the one hand, low TMR ratio and low storage density are the two main issues that restrict it from developing towards stand-alone memory. The first issue is related to the manufacturing process and the structure of MTJ. TMR of 300% is expected for the stand-alone MRAM. The second issue is related to mismatch between switching current of MTJ and driving current of transistor. One should use the large W/L core transistor in the 1 T-1 MTJ memory cell, which makes the pitch and the cell size are much larger compared with 1 T-1 C memory cell of DRAM. To solve this issue, one should not only optimize the manufacturing process of MTJ with lower switching current and RA, but also develop new metal-oxide-semiconductor field effect transistor (MOSFET) with larger saturated current. On the other hand, low write speed and low endurance are the two main issues that restrict it from developing towards cache memory. However, these issues are related to the physical mechanism and the device structure of STT-MTJ which is almost an insurmountable problem. Fortunately, the next-generation MRAM technology, SOT-MRAM, has been proposed, that will be discussed in the next session.

3. SOT-MRAM

SOT-MRAM, the next-generation MRAM technology, offers improved speed and higher endurance. Numerous international research institutions and companies are actively engaged in its investigation and development. Once successfully mass-produced, SOT-MRAM has the potential to replace SRAM and provide fast and durable storage capabilities. Additionally, SOT-MRAM can find applications in logic-in-memory architecture and artificial intelligence hardware, presenting promising and broad prospects. Currently, SOT-MRAM is still in the research and development phase, with significant advancements being made in areas such as physics, materials, and devices. It is believed that, in the near future, diligent efforts from researchers will lead to the successful mass production of SOT-MRAM.

3.1. Mechanisms of SOT

SOT technology utilizes the spin current generated by spin-orbit coupling to apply torque on the free layer of the magnetic tunnel junction, enabling information writing. In 2011, Miron *et al* demonstrated the reversal of magnetization in Co

Table 1. Progress and key parameters of MRAM chip.

	CMOS D/R	MTJ size	Capacity	Read/Write Access time	MR/Rp	Bitcell size	Endurance	Retention	Source
T MAGN 2013 [40]	90 nm CMOS	70–90 nm	64 Mb@8 × 8 Mb	—	>110%/—	0.072 μm^2	>0.5 × 10^6	—	Everspin Technologies
IEDM 2016 [41]	40 nm CMOS	—	256 Mb@8 × 32 Mb	—/50 ns	—	—	>1 × 10^8	>10 years@100 °C	Everspin Technologies
IEDM 2016 [43]	28 nm LLP CMOS	38–45 nm	8 Mb@4 × 2 Mb	—/50 ns	180%/0.8 kΩ	0.036 4 μm^2	>1 × 10^8	>10 years@85 °C	Samsung Electronics
JSSC 2019 [46]	40 nm CMOS	—	16 Mb@16 × 1 Mb	<17.5 ns/—	>140%/—	0.066 μm^2	—	—	TSMC
IEDM 2019 [42]	28 nm FDSOI	—	1 Gb@128 × 8 Mb	>60 ns/—	180%/—	0.036 μm^2	>1 × 10^6	>10 years@105 °C	Samsung Electronics
ISSCC 2020 [47]	22 nm ULL CMOS	—	32 Mb@8 × 4 Mb	10 ns/—	—	0.045 6 μm^2	>1 × 10^6	>10 years@150 °C	TSMC
IEDM 2020 [48]	16 nm FinFET	22 nm	8 Mb	9 ns/50 ns	—	0.033 μm^2	>1 × 10^5	—	TSMC
IEDM 2020 [44]	14 nm FinFET	35 nm	2 Mb@4 × 512 Kb	—/4–20 ns	120% ∼ 145%/8.2 kΩ	0.027 3 μm^2	>1 × 10^{10}	—	IBM
IEDM 2022 [49]	28 nm FDSOI	—	16 Mb	40 ns/160 ns	—	0.024 μm^2	>1 × 10^{14}	>10 years@89 °C	Samsung Electronics
VLSI 2022 [50]	22 nm Planar	—	32 Mb	5.9 ns/—	—	0.045 6 μm^2	—	—	Renesas Electronics
IEDM 2022 [52]	*	∼20 nm	2 Kb	30 ns>/30-200 ns	130%–140%/—	0.002 μm^2	>1 × 10^6	—	SK hynix
IEDM 2023 [51]	22 nm CMOS	—	8 Gb@8 × 1 Gb	<10 ns/—	—	—	>1 × 10^{14}	>10 years@125 °C	Avalanche Technology
VLSI 2023 [45]	14 nm FinFET	Sub 10 nm	16 Mb	15 ns/> 200 ns	>190%/—	0.024 μm^2	>1 × 10^6	>10 years@150 °C	Samsung Electronics
IEDM 2023 [53]	*	60 nm	—	—/30–50 ns	75% ∼ 96%/5.4 kΩ	0.014 μm^2	>2 × 10^6	—	TSMC

[*] One-selector one-resistor access device.

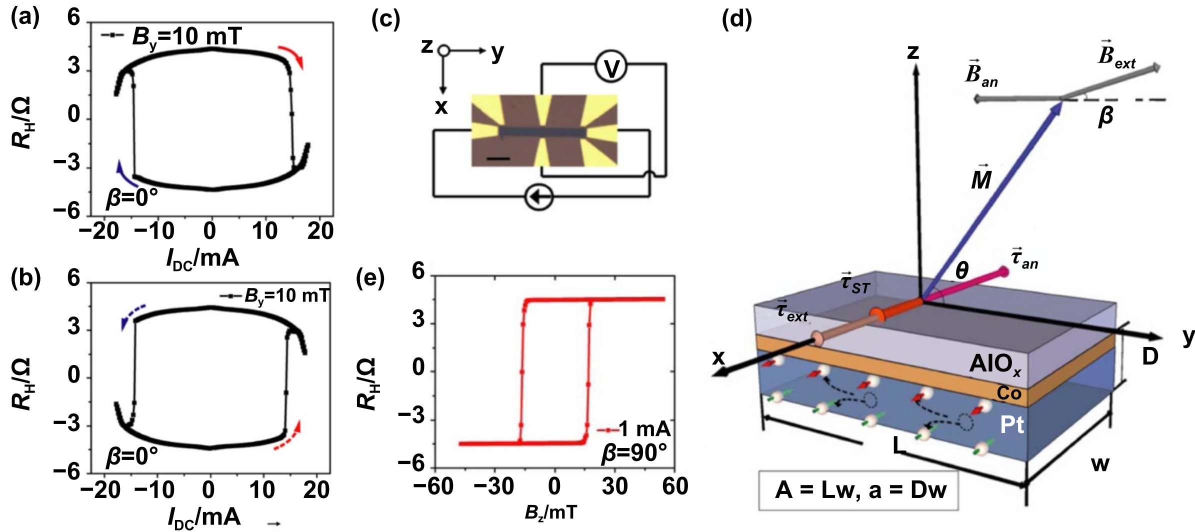

Figure 6. SOT-induced magnetization reversal in Pt/Co/AlO_x system under (a) positive and (b) negative external magnetic field. (c) The images of the device. (d) The directions of field and the torque of the device. (e) The Hall resistance vs. the external field of the device. Reprinted figure with permission from [55], Copyright (2012) by the American Physical Society.

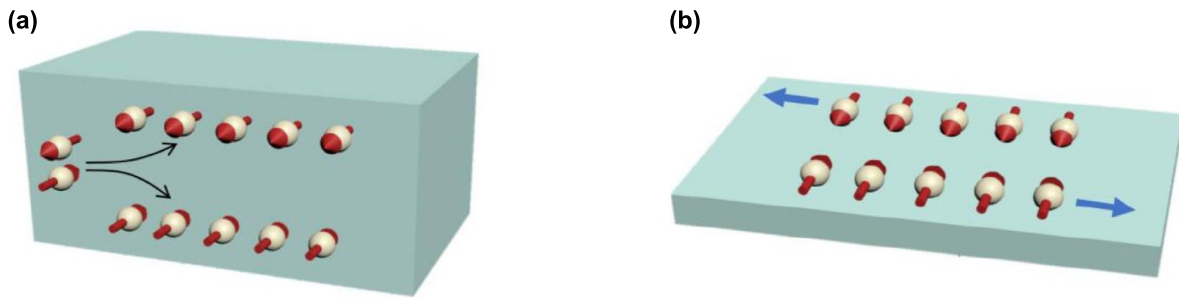

Figure 7. Schematic diagram of (a) SHE and (b) Rashba effect.

magnets with PMA using in-plane fields in a Pt/Co/AlO_x system through the SOT effect [54]. Additionally, in 2012, Liu *et al* discovered that the SOT based on the spin Hall effect (SHE) can induce the flipping of magnetization in Co, as depicted in figures 6(a)–(d) [55]. These findings sparked a new wave of research utilizing SOT technology for next-generation magnetic random-access memory.

The mechanism behind SOT is currently under debate. There are two proposed mechanisms for SOT, SHE [56, 57] and Rashba effect [58, 59]. SHE is illustrated in figure 7(a). A spin current J_s is generated by the current J, and exerts a torque on the magnetization. The SHE can be characterized by the spin Hall angle (SHA) $\theta_{SH} = \frac{e}{2\hbar} J_s/J$. The SOT based on the Rashba effect [60] arises from the spin accumulation at the interface between the magnetic and non-magnetic layers from spin-orbit coupling, as illustrated in figure 7(b). Presently, most researchers believe that both effects contribute to the generation of SOT.

The writing process of SOT can be described by the LLGS equation, with two terms related to SOT: the Slonczewski-like term τ‖ and the field-like term $\tau^{\perp}$ which are expressed as follows [61]:

$$\frac{dm}{dt} = -\gamma \vec{m} \times \vec{H}_{\text{eff}} + \alpha \vec{m} \times \frac{d\vec{m}}{dt} + \tau^{||} + \tau^{\perp} \tag{11}$$

$$\tau^{||} = \gamma \frac{\hbar c^{||} J}{2eM_s t} \vec{m} \times (\vec{\sigma} \times \vec{m}) \tag{12}$$

$$\tau^{\perp} = \gamma \frac{\hbar c^{\perp} J}{2eM_s t} (\vec{\sigma} \times \vec{m}) \tag{13}$$

where τ‖ and $\tau^{\perp}$ are the Slonczewski-like and field-like torque coefficients, and $\vec{\sigma}$ is the polarization direction of the injected spin electrons. It is commonly believed that the SHE dominates the Slonczewski-like term, while the Rashba effect dominates the field-like term in the SOT mechanism. However, it is important to note that there is currently no clear evidence to distinguish these two contributions. In general, the SOT induced magnetization switching is predominantly attributed to the Slonczewski-like term.

3.2. Bottleneck issues in SOT-MRAM manufacturing

There are several challenges in materials, devices, and processes that have hindered the mass production and application of SOT-MRAM. From a material perspective, the efficiency

of charge-to-spin conversion in the bottom electrode is crucial for SOT-MRAM, as it generates spin currents to switch the magnetization of the free layer. Therefore, materials with high charge-to-spin conversion efficiency, especially those compatible with CMOS technology, are desired. At the device level, the requirement of an external magnetic field for writing the storage unit in SOT-MRAM with PMA consumes a significant amount of energy, and is also incompatible to CMOS. Additionally, the dispersed nature of the magnetic field limits the storage unit density. Therefore, the development of SOT-MRAM devices that can be written without an external magnetic field has become essential. At the process level, thin-film deposition and etching pose technical challenges in SOT-MRAM manufacturing. With SOT-MRAM consisting of over 30 layers of thin films and some are single-atomic-layer, achieving high-quality thin-film deposition is critical. The performance of SOT-MRAM is directly influenced by the quality of the interfaces between these thin-film layers. Moreover, the high-temperature annealing in CMOS BEOL processes significantly impacts the interface, raising concerns about the thermal stability of the thin films. Furthermore, most of the film layers in SOT-MRAM are pure metals, with only a $\sim$1 nm thick insulating layer of MgO in the middle. During the etching process, it is essential to prevent short-circuiting of the insulating layer and disconnection of the bottom electrode, which represents a challenging technical bottleneck in SOT-MRAM manufacturing. In the following sections, the research progress, solutions, and ideas from academia and industry to address these issues will be introduced.

3.3. Bottom electrode materials for SOT-MRAM

To reduce the writing energy consumption of SOT-MRAM, researchers have conducted extensive studies to enhance the charge-to-spin conversion efficiency in SOT devices. The SHA is commonly utilized as a measure of the efficiency in converting charge current into spin current. A larger SHA can significantly reduce the energy consumption of SOT devices [62–64]. In efforts to improve the charge-to-spin conversion efficiency of bottom electrode materials in SOT-MRAM, researchers have extensively explored materials with high SHAs. These materials include heavy metals, heavy alloy metals, magnetic materials, and topological materials. The subsequent section will introduce the research progress made on these materials individually.

3.3.1. Heavy metal materials. Currently, heavy metals are widely used materials with relatively large SHAs [65]. In 2008, several 5d transition metals (such as Ta, W, Re, Pt, etc) and 4d transition metals (such as Ru, Pd, Rh, Mo, etc) were predicted to have SHA of using ab initio calculations [66]. Among them, Pt and Pd (Ta, W, and Mo) exhibit relatively large positive (negative) SHA. Then, experiments for quantifying the SHA were conducted with different measurement techniques. For example, SHA of Pd were measured in the range of 0.008–0.012 using various methods, such as spin torque ferromagnetic resonance (ST-FMR), spin pumping, and non-local detection [67–70]. Different measurements have yielded SHA values for Pt, all of which are below 0.12 [71–73].

W and Ta have very large negative SHA, and also have the advantage of high thermal stability, which is compatible with CMOS technology. SHA of β-Ta was measured to be from -0.12 to -0.15 [74]. The spin current generated by β-Ta is capable of effectively inducing magnetic switching in ferromagnetic materials at room temperature in this study. The SHA of Ta was further raised approximately -0.17 in a mixed $(\alpha + \beta)$ phase, which is claimed due to the extrinsic effect by defects of the mixed phase [75]. Similar with Ta, β phase of W has large SHA (0.3) [76], and can be optimized as high as 0.4 [77]. As a result, very low critical current density of only 1.6×10^6 A m^{-2} was achieved by β phase of W in this study. Additionally, through oxidation of W, the SHA can be increased up to 0.5 [78]. A series of evidence in this study indicate that the interface of W(O)/ferromagnet play dominant role for large SHA.

3.3.2. Alloy materials. In recent years, the doping of non-magnetic impurities into heavy metals has been predicted to effectively increase the SHA. Fert and Levy [79] proposed in 2011 that doping 5d elements into Cu can generate a strong SHE, primarily due to the resonance scattering introduced by the doping state. Based on this theory, Bi_xCu_{1-x} [80] and BiPt alloy [81] were discovered to exhibit a large SHA of approximately -0.24 and 0.106. Then, other alloy based on the scattering of defects was investigated. Au_xPt_{1-x} alloy [82, 83] was reported to generate spin current efficiently with a high SHA greater than or equal to 0.58.

W/Ta alloy materials have been theoretically predicted to have a SHA of approximately 0.4 [84, 85], due to the new phase of W_3Ta. It is fascinating because both Ta and W are CMOS compatible materials. Then, experiments of the W/Ta alloys proved this prediction. The SHA of β-Ta_xW_{1-x} alloy was investigated, and the composition rate significantly affected the SHA [86]. SHA of -0.59 can be realized by the forming of W_3Ta. A high SHA of 0.47 and a low resistivity of 81 $\mu\Omega$ cm in a mixed $(\alpha + \beta)$ phase W_3Ta were demonstrated in figures 8(a)–(d) [87], leading to ultra-low energy consumption during magnetic switching.

3.3.3. Magnetic materials. In addition to non-magnetic materials, the SHE has also been observed in certain magnetic materials. Miao *et al* [89] discovered the inverse SHE in ferromagnetic Permalloy thin films, indicating the conversion of spin current into charge current. Du *et al* [90] reported the presence of a SHA in a series of 3D transition metal thin films, including antiferromagnetic Cr and FeMn. Zhang *et al* [91, 92] demonstrated that 5d metal alloys, such as IrMn and PtMn, exhibit larger SHAs compared to 4d metal alloys like PdMn and 3d metal alloys like FeMn. Among these, the SHA of PtMn is approximately 0.24 [93].

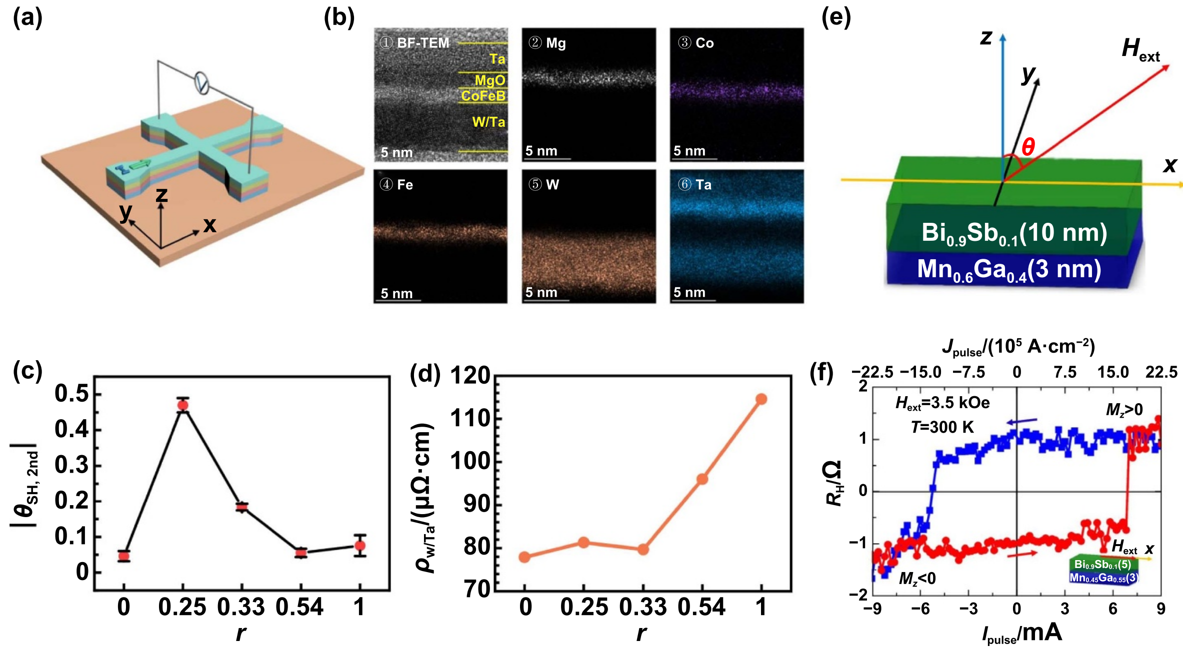

Figure 8. Spin Hall angle of CMOS compatible W/Ta alloys and magnetization switching from the SHE of topological insulator BiSb. (a) Schematics of the W/Ta multilayers thin film system Hall device. (b) TEM cross-section image and EDX elemental distribution of the film. (c) SHA and (d) resistivity as a function of the W/Ta thickness ratio *r*. Reprinted from [87], © 2022 Elsevier B.V. All rights reserved. (e) $Bi_{0.9}Sb_{0.1}/Mn_{0.45}Ga_{0.55}$ bilayer film structure. (f) Magnetic hysteresis loops under positive in-plane magnetic field realized in the $Bi_{0.9}Sb_{0.1}$ (5 nm)/$Mn_{0.45}Ga_{0.55}$ (3 nm) bilayer film at room temperature [88]. Reproduced from [88], with permission from Springer Nature.

3.3.4. Topological insulators. The unique properties of topological insulators, such as strong spin-momentum locking and spin-orbit coupling, have made them promising candidates for SOT bottom electrode materials. Topological insulators, including Bi_2Se_3 and Bi_xSe_{1-x}, have been found to exhibit strong surface conductivity and bulk insulating properties. Various testing methods have demonstrated that the SHA of these materials is greater than 1, which is one to two orders of magnitude larger than that of traditional heavy metal materials [88, 94–97]. Khang *et al* [88] found a remarkably large SHA of ~52 at room temperature in the $Bi_{0.9}Sb_{0.1}$/MnGa system, and only a current density of 1.5×10^6 A cm^{-2} is required to achieve magnetization switching (as shown in figures 4(e) and (f).

Recently, topological semimetals exhibiting strong spin-orbit coupling have been identified as possessing significant SHA. These materials, often van der Waals-based with low crystalline symmetry and topological band structures, have garnered attention for their spintronic properties. For instance, the SHA of WTe_2 was theoretically predicted to be −0.54 [98], but experimental measurements using the inverse SHE yielded a value of −0.015 [99]. $PtTe_2$ demonstrates an impressive SHA of 0.15, along with a high spin Hall conductance ranging from 0.2 to 1.6 × 10^5 (h/2e)(Ω m^{-1}) [100]. Most recently, a low-symmetry type II Weyl semimetal, $TaIrTe_4$, has been shown to effectively switch ferromagnets by current, exhibiting a SHA as high as ~0.3 [101] and 0.113 [102]. These findings highlight the potential of topological semimetals in spintronic applications.

Currently, achieving CMOS compatibility for topological insulators and antiferromagnetic materials remains a challenge, and they are still in the early stages of basic research. On the other hand, heavy metals such as W and Ta show good compatibility with CMOS technology, particularly due to their high thermal stability, and are currently being developed for SOT-MRAM applications.

3.4. Writing without external magnetic field

The spin polarization direction generated by spin-orbit coupling is perpendicular to the easy axis of magnets with perpendicular anisotropy, resulting in equal probabilities of switching the magnetic moment upwards and downwards. As a result, deterministic magnetic switching cannot occur without breaking this symmetry. To achieve writing in SOT devices, an external magnetic field is typically employed to break the symmetry and enable directional flipping of the magnetic moment under the action of current. However, the use of an external magnetic field significantly limits the integration density of the chip. Therefore, extensive research has focused on investigating methods for achieving magnetic deterministic switching driven by SOT without the need of an external magnetic field. Since 2014, various solutions have been reported, which can be categorized into four main categories as detailed below (refer to figure 9): structural asymmetry, creation of an in-plane effective magnetic field, utilization of vertical spin-polarized current, and combination of multiple methods.

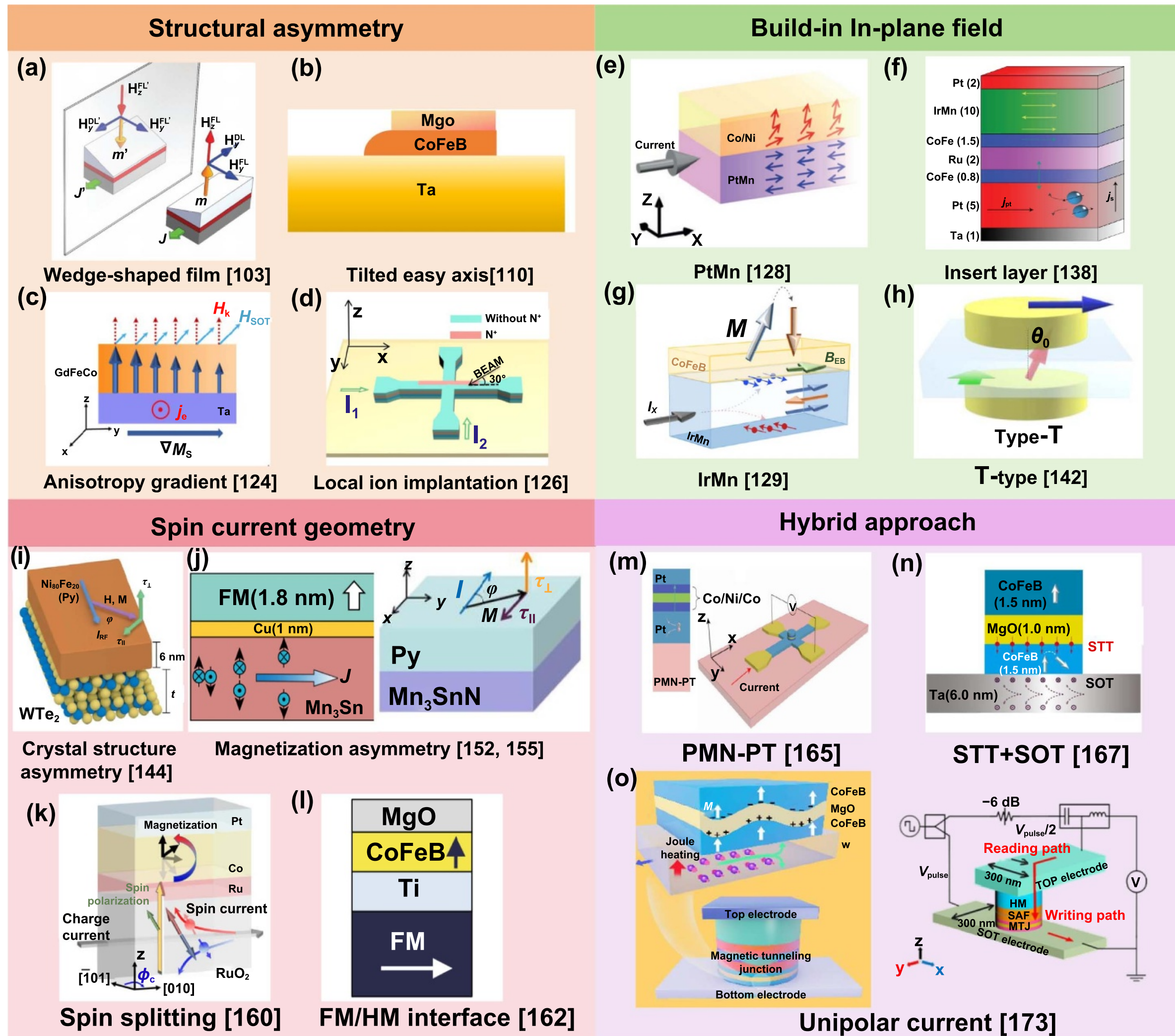

Figure 9. Summary of methods for SOT-driven magnetization deterministic switching without an external magnetic field. (a)–(d) Using symmetry breaking by wedged-shaped film, tilted anisotropy [104], anisotorpy gradient, and local ion implantation. (a) Reproduced from [103], with permission from Springer Nature; (c) Reprinted with permission from [105]. Copyright (2021) American Chemical Society; (d) Reprinted figure with permission from [106], Copyright (2021) by the American Physical Society. (e)–(h) Building in-plane magnetic field by exchange bias field from PtMn, IrMn, and exchange coupling field from ferromagnets. (e) Reproduced from [107], with permission from Springer Nature; (f) Reproduced from [108], with permission from Springer Nature; (g) Reproduced from [109], with permission from Springer Nature; (h) Reproduced from [110]. CC BY 4.0. (i)–(l) Introducing spin current vector by crystal structure asymmetry, magnetic vector asymmetry, spin splitting, and FM/HM interface. (i) Reproduced from [111], with permission from Springer Nature; (j) Reproduced from [112]. CC BY 4.0, Reproduced from [113]. CC BY 4.0; (k) Reprinted figure with permission from [114], Copyright (2022) by the American Physical Society; (l) Reproduced from [115], with permission from Springer Nature. (m)–(o) Using hybrid approach of ferroelectric PMN-PT, STT assisted SOT [117], and unipolar writing via joule heating [118]. (m) Reproduced from [116], with permission from Springer Nature; (n) Reproduced from [117], with permission from Springer Nature.

3.4.1. Structural asymmetry. This method is based on introducing symmetry breaking in the device structure, typically by altering the symmetry of the geometric shape and modifying the uniformity of the magnetic layer. In 2014, a wedge-shaped film structure was proposed to break the spatial symmetry magnetic properties [103], allowing for SOT-driven deterministic flipping of the magnetic moment without the need of an external field. Following this concept, a series of studies were conducted [119–124]. Alternatively, localized etching can be employed to selectively remove a segment of the magnetic layer, thereby inducing a tilt in the magnetic easy axis. This approach breaks the symmetry, enabling the writing process to occur in absence of an external field [104]. Symmetry breaking also can be realized by particular film deposition technique [125, 126]. Furthermore, designing different geometry of ferromagnetic layer for different magnetic domain nucleation is also a way to break the spatial symmetry, enabling magnetic switching without an external field [127]. Subsequent experiments conducted by other researchers using different geometry have yielded promising results [128, 129].

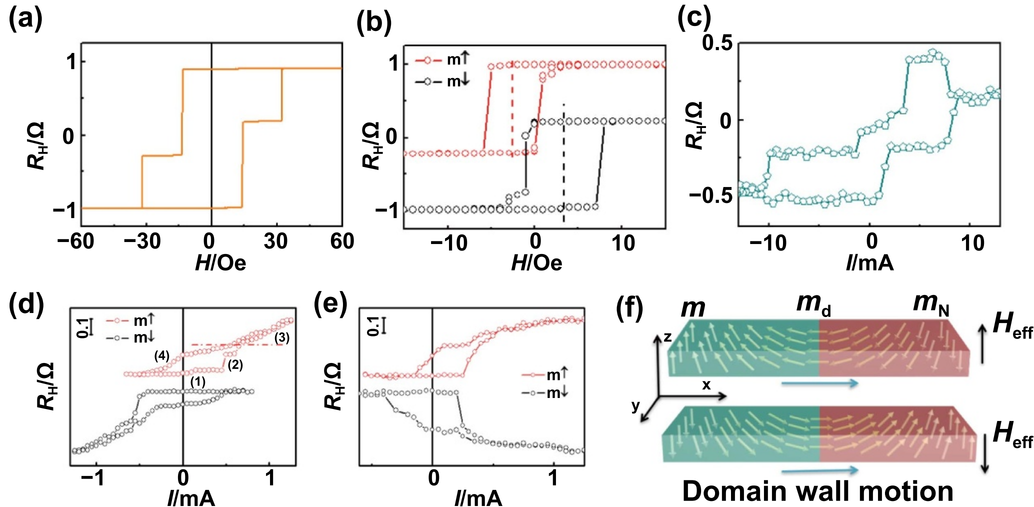

Figure 10. Field-free and multi-state magnetic switching of Hall device by local ion implantation. (a) Anomalous Hall resistance vs. magnetic field curve with ion-implantation. (b) Magnetic hysteresis loops of the non-implanted area with different magnetization directions. (c) Current-induced magnetization reversal curve of the device without external magnetic field. (d) Current-induced magnetization reversal curves of the non-implanted area with different magnetization directions (current I_1). (e) Current-induced magnetization reversal curves of the non-implanted area with different magnetization directions (current I_2). (f) Schematic of domain wall motion (DWM). Reprinted figure with permission from [106], Copyright (2021) by the American Physical Society.

Additionally, researchers have explored the utilization of anisotropic asymmetry to achieve SOT-controlled flipping of the magnetic moment. There exist various methods for realizing this, including local oxidation of the magnetic layer [130–135], local laser annealing of the magnetic layer [136, 137], and the introduction of a magnetic anisotropy gradient in the direction perpendicular to the film [105, 138]. Ion implantation has been reported as a means to introduce an anisotropy gradient, break the symmetry, and accomplish chirality-controlled magnetization flipping without the need of an external field, as depicted in figures 10(a)–(f) [106, 139]. Ion implantation is a common technique in semiconductor technology and holds great promise for compatibility with CMOS technology to achieve this objective.

3.4.2. Creating in-plane effective magnetic field. This method primarily utilizes the effective in-plane magnetic field generated by magnetic coupling to substitute the need for externally applied in-plane magnetic fields. Antiferromagnetic layer PtMn in the PtMn/CoNi system could generate an in-plane exchange bias field (effective in-plane magnetic field). This allowed for the flipping of magnetization direction in the CoNi ferromagnetic layer under SOT without the need for an external field [107]. Similarly, in the same year, Oh *et al* [108], van den Brink *et al* [140], and Kong *et al* [141] achieved magnetization flipping without an external field by utilizing IrMn to provide in-plane exchange bias. This breakthrough sparked a wave of research in this field by subsequent researchers [142–147]. Besides antiferromagnetic materials that offer in-plane exchange bias, IMA can also provide built-in magnetic field by exchange coupling though non-magnetic interlayer [109, 110, 148–151].

3.4.3. Using perpendicular spin-polarized current. Spin current with perpendicular spin vectors can decide the magnetization of a perpendicular magnet. Thus, mechanism to generate the perpendicular spin current is very useful and interesting. In 2016, it was found that crystalline two-dimensional material WTe_2, due to its lattice structure asymmetry, can generate perpendicular spin-polarized current [111]. It was confirmed experimentally [152]. Later, this material is employed to device to deterministic switch magnetization without the need of an external field [153]. Alternately, perpendicular spin current was found in films of $NbSe_2$ [154] and $IrMn_3$ [155], Mn_2Au [156] and CuPt/CoPt [157]. Apart from utilizing lattice structure asymmetry for generating perpendicular spin polarization, non-collinear antiferromagnetic materials like Mn_3Sn [112, 158, 159], Mn_3GaN [160], and Mn_3SnN [113] have also been found to generate perpendicular spin polarization. Additionally, in recent years, it has been predicted and observed that the lattice of collinear antiferromagnet RuO_2 can produce spin splitting, resulting in perpendicular spin polarization [161–164]. Researchers have successfully achieved field-free magnetization switching using SOT in this material [114]. Also, interface between ferromagnetic layers and metal layers is a source to induce perpendicular spin polarization and enables field-free magnetization reversal [115, 165–167].

3.4.4. Hybrid methods. This method utilizes the application of voltage or different directions of electric current to achieve the desired effect. In 2017, Cai *et al* utilized the interface between a PMN-PT ferroelectric substrate and metal to generate a spin current gradient, enabling directed magnetization reversal without the need of an external magnetic field

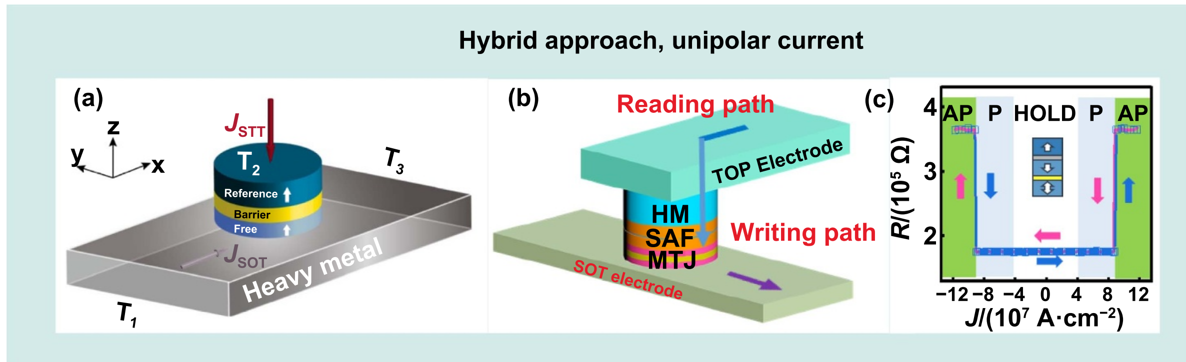

Figure 11. CMOS compatible method of field-free writing of SOT-MTJ. (a) Device structure of STT + SOT. Reproduced from [117], with permission from Springer Nature. (b) Device structure of unipolar SOT-MTJ device. (c) Unipolar current induced field-free switching of SOT-MTJ [118].

[116]. Subsequently, it has been further confirmed that the generation of a spin current gradient in a device can achieve directed magnetization reversal without an external magnetic field [168]. Apart from the utilization of external voltage, researchers have also achieved the desired effect by simultaneously applying vertical and horizontal electric current, employing the STT + SOT method, as shown in figure 11(a) [117, 169–171]. Ferromagnets are integrated into MTJ structures to introduce magnetic field to the free-layer [172, 173], which brings all-electrical writing. Joule heating from writing current is also demonstrated to induce field-free writing of SOT-MTJ by controlled the coupling effect between thin film layers [118] (figures 11(b) and (c)).

3.4.5. Other methods. Competing spin current from materials with different SHA was also proposed to realize the field-free magnetic switching [174–176]. Dzyaloshinskii–Moriya interaction (DMI) effect in multilayer can also break symmetry of the system and thus induce the field-free switching of SOT device [177–179].

Currently, the industry is facing challenges in finding a solution for external-field-free writing of SOT-MRAM, primarily due to the limited availability of methods compatible with CMOS technology. The SOT-MTJ process utilizes CMOS backend processes, and growing single-crystal, two-dimensional materials on insulation dielectrics and contact vias is difficult, which restricts the choice of materials. Furthermore, the SOT-MTJ structure is complex, comprising over 30 atomic layers of thin films, and its performance heavily relies on interface properties. The CMOS process requires annealing at high temperatures (around 400 °C), which leads to metal atom diffusion, damaging the interfacial structure and performance of the thin film layers. This results in reduced TMR and PMA performance of the SOT-MTJ and ultimately leads to device failure. Consequently, the selection of tunnel junction materials is limited, and there is currently a lack of mechanisms and solutions for achieving external-field-free writing among the materials that are compatible with CMOS and can maintain thermal stability (such as W, Ru, Ta, CoFeB, MgO, etc) that has been verified.

There have indeed been some preliminary studies on field-free writing methods in CMOS-compatible systems. For instance, in 2019, Garello *et al* [172] employed a magnetic hard mask made of Co to provide a stray magnetic field in the *x*-axis direction to the SOT layer, enabling control of SOT-MTJ without relying on external magnetic field. The ferromagnetic layer can also be scaled down and embedded in MTJ devices [173]. By intentionally creating an elliptical device, the bias layer's magnetization easy axis aligns with the direction of the SOT current. Using STT to assist SOT is a viable method for achieving deterministic switching of SOT-MRAM without the need for an external magnetic field. In 2018, Wang *et al* [117] experimentally demonstrated for the first time that the combined effect of SOT and STT can achieve deterministic writing of p-MTJ without an external field. By introducing an STT current, the symmetry of SOT torque can be broken, and the threshold current for SOT is reduced with increasing STT current. Compared to applying STT and SOT current separately, the combined application of SOT and STT current can reduce both the time and power consumption required for magnetic switching of the free layer. In 2022, Yang *et al* [118] proposed a unipolar writing method for zero-field writting SOT-MTJ devices (figures 11(b) and (c)). This method enables 1 ns pulse width writing and maintains normal operation at 100 °C. The zero-field flipping is achieved by modulating the ferromagnetic coupling between the free layer and the reference layer through a current pulse. Under a certain current, the magnetization of the free layer aligns with that of the reference layer due to the orange-peel coupling. As the current increases, the free layer is influenced by the stray field of the antiferromagnetic layer, causing the magnetization of the reference layer to reverse. The development of zero-field writing methods compatible with CMOS technology is still actively progressing, and breakthroughs are expected to be achieved in the near future.

3.5. The thermal stability of SOT-MRAM thin films

Improving the thermal stability of thin films is a significant challenge for SOT devices due to the complex thin film structures. In the case of SOT-MRAM, the integration of its unit, the

SOT-MTJ, with CMOS technology is necessary. The BEOL process in CMOS typically involves high-temperature annealing, with annealing times of at least 30 min. As a result, the SOT thin films and tunnel junction devices must undergo high-temperature annealing exceeding 350 °C. It is crucial that this process does not significantly compromise their film and device performance. Specifically, they should maintain strong PMA and large TMR after annealing. Therefore, achieving good thermal stability in SOT thin films and devices is crucial to maintaining their functionality and performance during the CMOS integration process.

To address the issue of thermal stability in SOT devices, researchers have conducted studies from various perspectives. At the material level, one approach is to utilize materials with higher thermal stability, such as Heusler alloys with high Curie temperature [180]. However, the TMR of these materials still requires improvement. In the high CoFeB/MgO system, increasing the number of CoFeB/MgO interfaces can enhance interface anisotropy and improve thermal stability. In 2012, Sato *et al* [181] constructed a double CoFeB film structure of MgO/CoFeB/Ta/CoFeB/MgO in the STT tunnel junction, which increased the thermal stability factor by 1.9 times compared to the single CoFeB structure. Building on this, researchers discovered that changing the intermediate layer between the double CoFeB layers can effectively control the thermal stability coefficient. Kim *et al* [182] optimized the tunnel junction thin film system by inserting ultra-thin W layers between two CoFeB films in 2015, achieving a large thermal stability coefficient of about 78. Subsequent studies further explored the optimization of the thermal stability coefficient by adjusting the thickness of the W interlayer [183–187]. Drawing inspiration from increasing thermal stability in STT devices, the free layer in SOT tunnel junctions can be enlarged by utilizing a CoFeB/intermediate layer/CoFeB structure, thereby improving thermal stability. Additionally, introducing an artificial antiferromagnetic layer above the reference layer to pin it can effectively enhance thermal stability [188, 189]. These approaches highlight the efforts being made to improve the thermal stability of SOT devices through material selection, interface engineering, and layer design.

Recently, studies have indicated that the thermal stability of STT-MTJs is significantly influenced by interlayer coupling effects [190]. In contrast to STT-MTJs, the SAF layer of SOT-MTJs are more susceptible to high-temperature annealing processes [172, 191, 192]. In 2021, Yang *et al* [193] successfully achieved a highly stable SOT-MTJ magnetic thin film structure with high perpendicular anisotropy by subjecting it to annealing process at 350 °C. This was accomplished through the modulation of orange-peel coupling strength between the reference layer and the free layer.

3.6. Etching process of SOT-MRAM

Researchers have proposed several high-yield MTJ etching processes for SOT-MRAM. One idea is to develop method to maintain the continuality of bottom electrode while cleaning the side wall of MTJ. A dual-layer metal bottom electrode with two different metal materials was [194] introduced to SOT-MTJs, preventing trenching of the bottom electrode when removing metal etching by-products deposited on the MTJ sidewall. The process achieved a 96% on-chip MTJ resistance yield on a 12-inch wafer. Another idea is to increase the thickness of the bottom electrode while cleaning the side wall of MTJs by IBE [195]. Then, a large-angle etching is performed to clean the sidewall metal deposition and avoid the 'trenching' effect [196].

Several groups focus on etching stop on MgO other than etching MgO, then there is no side wall and eventually avoid short circuits by etching. In 2018, Rahaman *et al* [197] introduced a 'stop-MgO' etching process to MTJ. This process controls the composition of the reaction gas CO and NH_3 to stop the etching position at the MgO layer. Although the etching is stopped at the MgO layer, the etching gas can deteriorate the magnetic properties of the free layer in areas other than the MTJ through the MgO layer, achieving a similar effect of stopping the etching at the heavy metal bottom electrode. This etching process improves the on-chip yield of MTJ devices. In 2022, Rahaman *et al* [198] employed C-F plasma to etch MTJs with IMA at the MgO layer. Subsequently, through annealing, the magnetic properties of the free layers outside the MTJ region could be eliminated. It is later proved that the stop-on MgO structure did not degrade the switching state, since the switching always starts at the inner free layer. The stop-on MgO technique was first introduced to perpendicular SOT-MTJ [199, 200]. This etching process was carefully designed to ensure that the magnetic properties of the free layer beneath the MgO layer remained unaffected [200]. The stop-on MgO structure shows zero biased field and low switching current densities, leading to a 100% MTJ resistance yield. Table 2 shows the recent key results related to challenges of SOT-MRAM (including bottom electrode, writing without external magnetic field, thermal stability and etching).

3.7. Write and read error

The mechanisms of write and read failure in SOT-MRAM under certain circumstances are akin to that of STT-MRAM. However, due to the separate paths for the write and read channels, the operational windows are significantly broader than those of STT-MRAM. Another difference is that the write error rate (WER) for perpendicular SOT-MRAM is not as high as STT-MRAM. Experiments demonstrated the WER of around 10^{-5} with integrated Co ferromagnets [172] or antiferromangetic layer [201]. Unlike STT effect, the SOT for SOT-MTJ with PMA is perpendicular to the magnetization in the easy axis of SOT-MRAM with PMA, which can overcome the energy barrier with large write current and result in the low WER. The mechanisms and methods to enhance the WER of perpendicular SOT-MRAM necessitate further exploration in this field.

Table 2. Key challenges and achievements of SOT-MRAM.

Key challenge	Materials	Size	Methods	Achievements	References
Bottom electrode	Pt	——	Spin pumping	$\theta_{SH} = 0.08$	[72]
	Ta	4 mm × 3 mm	ST–FMR	$\theta_{SH} = 0.17$	[75]
	W	10 μm wide	ST-FMR	$\theta_{SH} = 0.33$	[76]
	Au_xPt_{1-x}	5 μm × 60 μm	2nd harmonic	$\theta_{SH} = 0.58$	[83]
	W_3Ta	10 μm × 10 μm	2nd harmonic	$\theta_{SH} = 0.47$	[87]
	PtMn	10 μm × 20 μm	ST-FMR	$\theta_{SH} = 0.24$	[93]
	$Bi_xSe_{(1-x)}$	10 μm × 70 μm	ST-FMR	$\theta_{SH} = 8.67$	[96]
	$TaIrTe_4$	4 μm × 24 μm	ST-FMR	$\theta_{SH} = 0.3$	[101]
Writing without external magnetic field	Ta/CoFeB/TaO$_x$	20 μm × 130 μm	Wedged film-TaO$_x$	Field-free	[103]
	Ta/CoFeB/MgO/Ta	50 nm × 300 nm	Tilted anisotropy	Field-free	[104]
	Pt/Co/Pt	2 μm × 2 μm	Local laser annealing	Field-free	[136, 137]
	Ta/Pt/PtMn/MgO/Ta	10 μm × 3 μm	Inside effective in-plane field	Field-free	[107]
	Mn_3Sn/ Cu/[Ni/Co]$_3$	8 μm × 35 μm	Out-of-plane torque	Field-free	[112]
	FM/Ti/CoFeB/MgO	4 μm × 4 μm	Interface induce z-spin polarization	Field-free	[115]
	RuO_2/Ru/Co/Pt	—	Spin splitting	Field-free	[114]
	PMN-PT/Pt/Co/Ni/Co/Pt	3 μm	Spin current gradient	Field-free	[116]
	Ta/CoFeB/MgO MTJ	90 nm	STT + SOT	Field-free	[117]
	Pt/Co/Ta	300 nm	Local ion implantation	Field-free	[106]
	W/CoFeB/MgO MTJ	140 nm	Joule heating	Field-free	[118]
Thermal stability	CoFeB/MgO system	MTJ-30 nm	Double CoFeB films	$T = 300$ °C $\Delta = \sim 88$	[181]
	CoFeB/MgO system	MTJ-20 nm	Insert layer between double CoFeB films	$T = 425$ °C $\Delta = \sim 78$	[182]
	CoFeB/MgO system	Films	Orange-peel coupling	$T = 350$ °C	[193]
Etching	W/CoFeB/MgO MTJ	~100 nm	Stop-MgO	100% MTJ resistance yield	[200]
	——	57 nm	Etching the bottom electrode	96% MTJ resistance yield	[194]

4. The applications of MTJ

4.1. Logic-in-memory

Logic-in-memory refers to performing logic calculations directly in the storage array, without distinguishing between computing units and storage units, thus fundamentally addressing the issues caused by data transmission between the memory and the CPU. Using spin to fulfill logic functions exhibits significant advantages for logic-in-memory architecture, owing to its fast access time.

A theoretical design of using spin as logic is proposed in semiconductor/ferromagnetic system using spin accumulation [202]. Then, spin logic was designed in a full metallic system [203]. These two-logic design using only spin for signal transferring and processing during computation, which potentially saves energy for spin charge conversion.

Utilizing MTJs devices to construct spintronic logic circuits is also investigated. A serious of STT-MTJ/CMOS hybrid circuits were proposed for logic-in-memory computing [204, 205]. For the SOT-MTJs, it exhibits superior endurance and speed compared to STT-MTJs, making it a promising candidate for implementing logic functions. Furthermore, the chirality of magnetic switching induced by SOT, either clockwise or counterclockwise, is reversible, enabling a diverse range of logic operations and garnering increasing interest. For example, the SOT effect induced DWM enables the realization of reconfigurable NAND and NOR logic gates [131]. Additionally, the application of a magnetic field serves as a switch for diverse logic functions, enabling the attainment of the five fundamental Boolean logic gates: AND, OR, NAND, NOR, and NOT [206]. Furthermore, 16 Boolean logic functions are realized in one device by utilizing current and bias voltage as logic inputs [207], or alternatively, by a magnetic field as the input signal [208]. Additionally, all-electrical multifunctional spin logics have been successfully demonstrated through field-free magnetic switching [151, 209–213]. Logic functions using only unipolar voltage signals as inputs were recently demonstrated, which can save significantly circuits for bipolar electric signals [214].

When using MRAM as a logic device for computing, a significant challenge arises from its cascading capabilities. The input signals to MRAM are typically current or voltage, and the output signals often require amplification to achieve sufficient amplitude for input to another MTJ device. This issue demands the increased attention in the field to ensure effective and efficient logic operations using MRAM.

4.2. MRAM for artificial neural networks (ANNs)

4.2.1. Introduction of ANNs. The human brain consists of billions of neural cells, including neurons, synapses, and contacts. Neurons receive signals from approximately 1–10 000 other neurons [215] and transmit them downward to the subsequent ones through synapses on dendrites. Despite being slower than computers in logical calculation, the human brain neural network handles complex tasks such as vision and emotion recognition more quickly due to its distinctive features. This motivates researchers to explore the brain and develop ANNs.

ANNs has been widely researched in the past decade, which has undergone several stages of development. There are many kinds of ANNs, including the single-layer perceptron in the 1950s [216], the multi-layer perceptron [217–220], the convolutional neural network (CNN) [221], the recurrent neural network (RNN) [222], and the spiking neural network (SNN) [223–225], generative adversarial network (GAN) [226], and self-attention mechanism [227]. Since the 21st century, the scale of ANNs has experienced exponential growth owing to the exploding of information. But the processing speed and the model scale has been greatly hindered by the data transfer time and significant energy consumption on the traditional computing platform such as central processing unit (CPU) and graphics processing unit (GPU) [228]. To address these issues, researchers have proposed several specific CMOS-based hardware structures to accelerate the network training process [229, 230]. However, the large energy consumption caused by an excessive number of transistors still limits the model scaling.

MTJs are suitable for low-power ANNs acceleration chips due to its low power consumption, long endurance and non-volatile storage [231–233]. It can be used as parameter storage as well as synapses, neurons, and other neural devices, to handle the enormous workload of storage, reading, and writing operations. At present, MTJs have not been to the internal and external memory applications in computer. The stochastic magnetic switching of MTJs has been a problem in memory technology due to random magnetic flips caused by heat on the potential barrier. However, for ANNs, this random error is similar to the mechanism of biological nerves, making them inherently robust to this error. Therefore, the error rate for MRAM is not high for neural networks [234, 235], and the stochastic behavior can even be used to train some networks such as SNN.

4.2.2. Hardware requirements for ANNs computing.

4.2.2.1. Computational model. Numerous ANNs computing structures have been implemented on hardware [236–241]. Figure 12(a) shows the working mechanism of neural networks in the brain. The neuron receives input signals from the synapse of input nerves, performs weighted accumulation, and then, through inherent activation functions, results are output after nonlinear calculation. The output follows the mathematic equation (14):

$$Y = \phi\left(\sum W_i \bullet X_i - \theta\right) \tag{14}$$

where, Y is the output, Wi is the weight of the ith synapse, Xi is the ith input signal, θ is the biased signal of the neuron, and ϕ is the nonlinear transfer function.

4.2.2.2. Hardware requirements. Multiplying and accumulating operations are intensive in neural network. Figure 12(b) shows a structure called synaptic crossbar array, which uses Ohm's law for weight-input multiplication and Kirchhoff's current law for summation. For weighted accumulation, the weight of Wi is continuously trained by different learning rules, which is called the synaptic plasticity. The synaptic plasticity requires a multi-state memory. This can be realized by MTJs via controlling the movement of the magnetic domain wall [249–251], which has been used for weight storage in neural networks. Figure 12(c) shows the synaptic circuits implemented with MTJs, along with MTJ neurons for nonlinear activation functions.

Various nonlinear transfer functions have been proposed for neural network units, including step, saturated linear, logistics sigmoid, and hyperbolic tangent functions [252, 253]. Binary-based digital integrated circuits face a contradiction between computational complexity and accuracy when realizing soft limit transfer functions. However, soft limit transfer functions are widely used by many mainstream models as activation functions due to their higher accuracy and ability to solve nonlinear problems. The MTJ outputs an analog signal, and its output vs. input is a non-linear function, making it suitable for uses as a neuron hardware device.

4.2.2.3. MTJ-based neuron hardware. MTJs have been applied to multiple neuron hardwares [244]. As shown in figure 12(d), early models approximated neuron perception as a step function, which can be achieved by STT-MTJ or SOT-MTJ directly [242, 243]. Different types of transfer functions to mimic the functions of neuron according to the R vs. input current I curves are shown in figure 12(e). Lateral spin valve and DWM can also be used to realize neuron devices, reducing path resistance and power consumption [246, 254]. Devices for non-step neurons featuring multiple states have been introduced, leveraging the DWM mechanism in the free

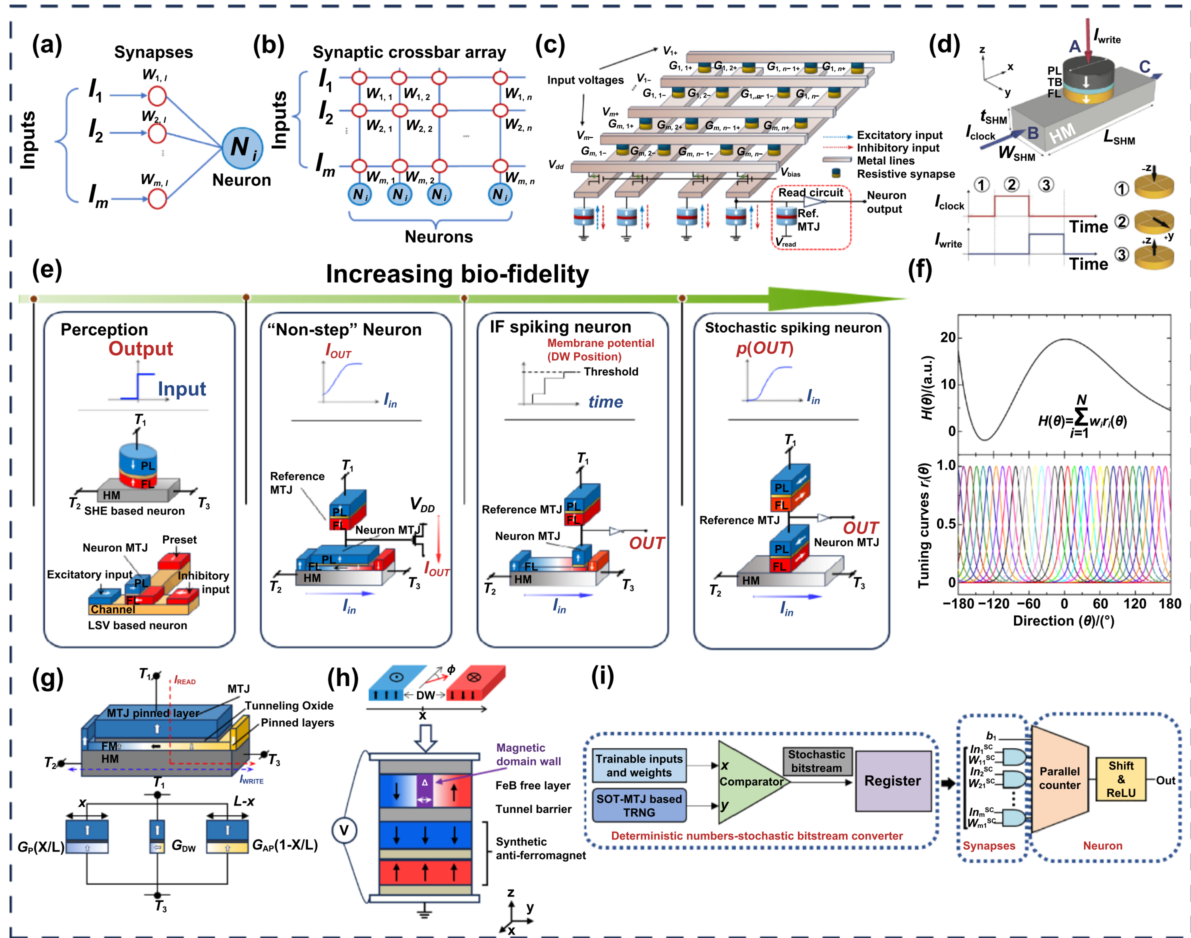

Figure 12. MTJs used in artificial neural network. (a) Working mechanism of synapses and neurons in neural networks (b) synaptic crossbar array. (c) STT-MTJ neuron crossbar array [242]. (d) A three-terminal SOT-MTJ neuron device. Reprinted from [243], with the permission of AIP Publishing. (e) Different artificial neurons based on various MTJ structures [244]. (f) The output curve and tuning curve of the population neurons. Reproduced from [245]. CC BY 4.0. (g) SOT-MTJ synapse device using a multi-domain free layer [246]. (h) STT-MTJ neurosynaptic device. Reproduced from [247]. CC BY 4.0. (i) Stochastic computing based on SOT-MTJ [248].

layer alongside a ferromagnetic layer with multiple domains to attain either multiple steady-state or continuous-state outputs [255]. Sengupta *et al* [256] introduced a integrate-fire (IF) neuron device that relies on spiking and differs from magnetic DWM's continuous output. This device's potential increases continuously under pulse input, aligning with the pulse-based coding method of SNN. Furthermore, designs for single-domain MTJ probability spiking neuron devices have also been proposed [257].

4.2.2.4. Step function. STT-MTJ was initially developed for memory use, but its natural step-function-like output during the writing process made it suitable for designing step function neurons. Sengupta's group introduced an SNN device and circuit structure that are based on STT-MTJ [242], which used the natural step function shape of the voltage vs. current loop to realize the neuron function. Results showed 5–6 bits of precision and 87% recognition accuracy on the modified national institute of standards and technology (MNIST) database, with lower power consumption compared to CMOS-based counterparts. In 2018, Kondo *et al* [258] designed a two-terminal 100 nm perpendicular MTJ device that employed poly-crystalline MgO with various grain sizes to function as a neuron through integration-fire operation. This design required a smaller auxiliary magnetic field for magnetic switching.

To emulate a step transfer function neuron, the synaptic resistance crossbar array must operate at a higher voltage, ensuring that the current input into the neuron is larger than the switching current. This, coupled with the fact that the input current must traverse the oxide layer, results in increased power consumption. Nevertheless, appropriate circuit-level technology can minimize energy consumption. A lower voltage operation has been investigated where the MTJ is always reset to the antiparalell (AP) state before operation and subjected to an input bias current close to the critical switching current, requiring a very low voltage to switch the magnetization. However, due to the high critical current required for the write operation of STT-MTJ, the power and energy advantages are limited.

SOT-MTJ is an alternative device that can address the issue of high writing current. In 2015, Sengupta *et al* [243] proposed a neuron device utilizing SOT-MTJ. The function of neuron goes through a two-step switching to achieve threshold operation. In the first step, spin current generated from the heavy metal layer is injected to set the magnetization direction of the free layer. In the second step, the magnetization of the free layer is reversed by current from the synapse, which flows perpendicularly through the MTJ. This two-step operation effectively lowers the input current required to drive neurons and prevents random magnetization flips due to the SOT effect.

4.2.2.5. Nonlinear activation function. Compared to step functions, nonlinear activation functions are more capable of replicating the function of neurons. In 2015, nonlinear neurons using a three-terminal STT device was realized [252]. The STT device output continuous resistance changes by adjusting input current, allowing for the realization of neuron transfer functions. They also proposed an ANN architecture that incorporates deep-triode current sources (DTCS) as interface circuits and memristor crossbar array (MCA) [259] as synapse, reducing network complexity and achieving lower energy consumption. SOT-MTJ can also be employed to implement nonlinear transfer functions, including sigmoid functions. Jaiswal *et al* [260] used the probabilistic features of SOT-MTJ to achieve sigmoid transfer characteristic. A SNN was proposed and trained by the CIFAR-10 data set. From a biological perspective, neural signal transmission is mostly random. The neurons with sigmoid characteristics exhibit insensitivity to accuracy, highlighting the robustness of neural networks that utilize SOT-MTJ.

4.2.2.6. Spike or probability-based neuron. MTJ devices have been proposed in SNNs [246, 261–263]. The writing pulse current can rise the total energy of the free magnetic layer of MTJs, like an integrate operation. Then, the energy will continuously lower, like a leak operation. The MTJ will 'fire' a switching after the energy exceeding the threshold value, making it an ideal device to realize spiking neuron. The stochastic switching signals of MTJs can also be induced by thermal noise, imitating the probabilistic firing of neuron [264]. The CMOS-based neurons require more than 20 MOSFETs to realize a single probabilistic spiking neuron, and then the MTJs as spiking neurons is advantages for higher integration.

Spiking neuron devices can be created using SOT-MTJ devices to implement the leaky integrate and fire (LIF) model [265, 266], which is closer to real neuron systems than the integrate and fire (IF) model. In 2016, a novel and energy-efficient LIF spiking neuron was designed using magneto-electric (ME) control for magnetization switching [267]. This approach has been successfully demonstrated in practical applications, such as hand-writing number recognition, establishing its feasibility for real-world implementations. In 2019, a device which can achieve IF operation and have the 'forgetting' characteristic was proposed [268], which can be used in neurosynaptic device design.

The LIF model utilizes resistance states to mimic the function of the membrane, simulating the integrate and leaky circuit. When the neuron membrane potential reaches the threshold, it generates a spike and resets at the threshold. The LIF model is an effective implementation for spiking neurons and is widely studied for its potential in non-volatile devices like MTJ.

Back-hopping oscillation (BHO) features by Joule heating of STT-MTJ can also be implemented for neurons. It can be used for a Poisson neuron based on a novel Poisson probability coding method [269]. This kind of neurons encode input information into a probability peak sequence with an adjustable duty cycle. Using the compact design of STT-MRAM, Poisson neuronal structures eliminate the need for an additional capacitor and reset circuit, resulting in a significant reduction in area occupation compared to CMOS accumulation-firing neurons, with only 1/6 of the required space.

In figure 12(f), Mizrahi *et al* [245] utilized magnetic tunnel junctions to achieve population coding, which relies on groups of neurons rather than individual neurons to complete the transfer function. This approach allows for diverse problems to be solved using the same ANN through specific training. Each neuron operates within different excitation ranges, as illustrated in figure 12(g). During the learning process, the residual is calculated by the comparison between the output and the actual result, which is continuously minimized. The SOT effect enables the distribution of neurons across different firing regions.

4.2.3. MTJ based synaptic devices.

4.2.3.1. MTJ for multi-valued synaptic device. The plasticity of synapse can be realized by multi-valued memory state via programmable resistance. Simulation has shown that it is sufficient to deal with pattern recognition and classification tasks using 13–19 resistive states [270]. The multi-state is realized by current induced DWM [247, 254, 271, 272]. As shown in figure 12(g), a SOT-MTJ synapse device using a multi-domain free layer is presented [246]. The current flowing in heavy metal drives DWM, determining the resistance of the heavy metal. The equivalent circuit can be described using three parallel resistors. The conductance of the MTJ determined by the DWM can be expressed by the following equation

$$G_{eq} = G_P\left(\frac{x}{L}\right) + G_{DW} + G_{AP}\left(1 - \frac{x}{L}\right) \tag{15}$$

where G_{eq} is the conductance of the device, G_P is the high conductance region, and G_{AP} is the low conductance region in the MTJ. G_{eq} has the linear dependence on the x, which is the domain wall location. The write current can drive the magnetic domain wall and realize the synaptic function. Recently, a multi-state field-free SOT Hall device for synapse application is proposed by in-plane exchange coupling field [251]. This design demonstrates the possibility of realizing excitatory and inhibitory postsynaptic synaptic electronics.

DWM can also be realized in STT-MTJs for synaptic functions [247, 254, 271]. Compared with SOT-MTJ, the read and write window is small in STT-MTJs, since they are in the same path. The read current may alter the memory state. A STT-MTJ synapse device is proposed based on DWM in 2016 [247], which minimizes the reading current to avoid read error rates, as shown in figure 12(h). The DMW are pinned by defects or edge of in this device. The DWM achieved by STT can be driven with a significantly smaller current compared with entirely magnetic switching, ultimately leading to lower power consumption.

4.2.3.2. MTJ for binary weighted synaptic device. In deep neural networks (DNNs), the MTJ serves mainly as a neurosynaptic device for weight storage. When the dimension of the MTJ continuously scales down, it is very easy to output binary signal for MTJ. Samsung demonstrate a vector-matrix cross bar array using binary MTJ to realize in-memory computing [273]. By leveraging Kirchhoff's and Ohm's law, the crossbar array achieves MAC calculations, resulting in significant power savings. However, the current leakage of MTJs pose limitations on the integration scale for analog circuits [274], which also affects its application in DNNs. Samsung optimized circuits design by connecting capacitor with MTJs to overcome this problem in their work. IMEC [275] also proposed the use of high-resistance SOT-MRAM by adjusting the thickness of MgO as a means of storing analog in-memory computing (AiMC) hardware acceleration weights. The separation of read and write of SOT-MRAM allows adjusting the thickness of MgO without affecting the writing process and increasing writing power consumption. Training tests were conducted based on the MNIST and CIFAR-100 datasets, and the outcomes were in line with expectations. Spin-based in-memory logic gates (such as XNOR and XOR) as binary weight synapse were also proposed in SOT devices [276]. The excellent proprieties of MTJs advance the frontiers of in-memory computing.

4.2.3.3. MTJ for stochastic neural network. In 2021, Song *et al* [248] proposed a stochastic computing (SC) paradigm to implement neural networks by leveraging the random writing characteristics of SOT-MTJ. As illustrated in figure 12(i), the inputs and trainable weights of a neural network are transformed into stochastic bitstreams through comparison with an SOT-MTJ-based random number generator. The logic gates and register circuits perform stochastic computations on these bitstreams, utilizing the AND gate for multiplication and the counter for summation. This approach effectively reduces the area and power consumption in digital devices, providing an innovative method for realizing ANNs.

4.2.4. Summary. With the rapid progress of neuromorphic computing based on ANN, the concept and design of utilizing MTJs to create ANN acceleration chips with a non-von Neumann architecture have increasingly been proposed. The key parts for accelerating ANN chips are the neuron devices and synapse devices. Magnetic tunnel junctions have the potential to replace CMOS-based neural networks, significantly reducing power consumption and increasing computing speed. Moreover, randomness and polymorphism of magnetic tunnel junctions are suitable being for brain-like neural networks such as SNNs. The use of magnetic tunnel junctions in neural network acceleration chips has the potential to greatly enhance the performance and efficiency of artificial intelligence systems.

The application of magnetic tunnel junctions to ANN structures is developing. Challenges in the application of magnetic tunnel junctions for AI computing include low resistance change (TMR) compared to other memristive devices and the difficulty of adjusting algorithms to make them suitable for all-spin circuits. To address these challenges, effective solutions have been proposed, including the use of small-sized magnetic tunnel junctions to enhance linearity and low data precision, as well as binary weights to minimize hardware complexity. Further research is needed to promote the application of MTJs in neural networks and brain-like computing.

In general, magnetic tunnel junction devices hold significant potential for neuromorphic computing due to their low power consumption and nonvolatile properties. The capability of magnetic tunnel junction devices to perform calculations in memory also eases the integration of neuromorphic computing acceleration hardware. Magnetic tunnel junctions have the potential to revolutionize artificial intelligence systems by providing highly efficient and low-power computing capabilities that mimic the functioning of the human brain.

4.3. Replacement of SRAM/DRAM

For a long time, STT-MRAM is considered as the leading candidate to replace DRAM for standalone memory and SRAM for last level cache. For the replacement of DRAM, memory capacity and cost are the most important factors. On the one hand, although STT-MRAM has the same memory cell structure (1 T-1MTJ) as DRAM (1 T-1 C), the cell size of MRAM is much larger than DRAM. That is because the transistor needs to supply large current to switch the MTJ which makes the transistor with large aspect ratio (integration density of STT-MRAM is 6–20 F^2 while DRAM is 6–10 F^2). Therefore, one should develop MTJ technology with lower switching current. On the other hand, the TMR of MTJ is too low to meet the application requirement as standalone memory. Larger TMR can provide faster read time and reduce the read failure. The room temperature TMR of current STT-MTJ with CoFeB/MgO/CoFeB is about 200%, but for standalone memory application, it needs to achieve at least 300%.

For the replacement of SRAM, Alzate *et al* [277] demonstrated that STT-MRAM could be used in the L4 level cache with high endurance and fast access time. Komalan *et al* [278] studied on the replacement SRAM with STT-MRAM design at the L2 cache level with much lower power consumption. However, limited by the dynamics process of magnetic moment flipping in STT-MTJ, the switching time is almost impossible to reach sub-ns. What' s more, the endurance of STT-MRAM is very difficult to reach 10^{15} cycles as SRAM due to the break-down of the MgO layer by writing current.

These two bottleneck issues make current STT-MRAM unable to replace fast cache (L1/L2 cache). Therefore, one should develop STT-MTJ technology with shorter switching time and higher endurance.

5. Outlook

There are promising prospects for the application of MRAM. MRAM has the gradual potential to replace flash, MCUs, main memory, and high-speed cache, according to different bandwidths, thereby eliminating interconnect delays and reducing power consumption. MRAM, a non-volatile memory with high density, endurance, and write speed, is the most suitable candidate for embedded non-volatile cache applications. In 2020, the MCU market exceeded US$25 billion, propelled by 5G IoT, wearable devices, and general-purpose MCUs. By replacing SRAM and NOR flash with MRAM in low-power MCUs, cost reduction and power efficiency enhancement can be achieved. MRAM also has promising prospects for memory replacement in automotive electronics and biosensors. The anti-vibration, anti-interference, and low power consumption characteristics of MRAM can be used for data storage and backup in automotive electronic systems, improving system reliability and security. SOT-MRAM has higher speed and durability and is currently in the research and development stage. It will mainly serve as a replacement for SRAM cache from L3/L4 to L2/L1, as well as a replacement for registers in CPUs and graphics processors.

MRAM also has the potential to build a storage-computing integrated architecture, solving the storage wall and power wall problems encountered in traditional von Neumann computing architecture, thereby promoting the continued development of AI, big data, and cloud computing. In addition, based on its excellent radiation resistance, MRAM has significant advantages in military and aerospace fields. We believe that MRAM offers exciting new opportunities that are attracting significant interest from both scientific and industrial communities, paving the way for more innovative and futuristic applications.

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