PHOTONICS Research

Power-efficient programmable integrated multiport photonic interferometer in CMOS-compatible silicon nitride

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Silicon nitride (SiN_x) is an appealing waveguide material choice for large-scale, high-performance photonic integrated circuits (PICs) due to its low optical loss. However, SiN_x PICs require high electric power to realize optical reconfiguration via the weak thermo-optic effect, which limits their scalability in terms of device density and chip power dissipation. We report a 6-mode programmable interferometer PIC operating at the wavelength of 1550 nm on a CMOS-compatible low-temperature inductance coupled plasma chemical vapor deposition (ICP-CVD) silicon nitride platform. By employing suspended thermo-optic phase shifters, the PIC achieves 2× improvement in compactness and 10× enhancement in power efficiency compared to conventional devices. Reconfigurable 6-dimensional linear transformations are demonstrated including cyclic transformations and arbitrary unitary matrices. This work demonstrates the feasibility of fabricating power-efficient large-scale reconfigurable PICs on the low-temperature ICP-CVD silicon nitride platform.

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1. INTRODUCTION

Photonic integrated circuits (PICs) have emerged as a promising approach to overcome computational limitations in the post-Moore era [1], offering efficient computing acceleration [2] and potential for achieving quantum superiority [3,4] in classical and quantum photonic processors where linear optical operations play a crucial role [5–8]. The programmable Mach–Zehnder interferometer (MZI)-based multiport interferometer, since Reck's groundbreaking work [9], has served as a universal configuration for discrete linear optical operations [10–12] and has been instrumental in fostering the field of programmable integrated photonics [13,14] as the core of numerous application prototypes in neurophotonics [15,16], optical signal recovering [17,18], and quantum information processing [5,19–22].

The recent advancements in integrated MZI-based photonic processors, operating at a wavelength of 1550 nm, have been summarized in Table 1. These devices have been fabricated using two widely established materials: silicon-on-insulator (SOI) and silicon nitride (SiN_x). Low waveguide loss across broad transparency window distinguishes SiN_x as an attractive candidate for the realization of high-performance PICs. Additionally, the Triplex technology [23], which combines SiN_x and SiO_2 in a sandwich-like cross-section, further diminishes optical losses and stands out as the leading platform for large-scale multiport interferometers. Nevertheless, the challenges of low device density and significant power consumption associated with thermo-optic phase shifters set critical obstacles to the scalability of SiN_x-based programmable PICs. Addressing these issues is imperative to fully leverage the low-loss characteristic of the SiN_x platform and enable large-scale photonic processors.

In this paper, we present a 6-mode programmable photonic interferometer fabricated on a low-temperature-deposited SiN_x platform. By incorporating suspended thermo-optic phase shifters, significantly reduced power consumption of around 12 mW per π phase shift has been achieved, which is approximately one order of magnitude lower than that of existing devices. The exceptional thermal efficiency also allows substantial improvements in compactness, enabling a phase-shifter length of only 300 μm. Furthermore, our device exhibits remarkably low thermal crosstalk, allowing higher integration density with transverse gaps as small as 50 μm. We characterize each MZI within the PIC and demonstrate low-loss transmission as well as programmable functionalities. This work showcases a solution to the problems of large footprint and high power consumption associated with SiN_x-based programmable photonic

Table 1. Overview of MZI-Based Photonic Processors Working around 1550 nm

Device	Platform	Manufacturer	Scale	Tuning Efficiency	Tuning Speed	Insertion Loss	Reference
Universal linear processor	SOI	IMEC	4 × 4	15 mW/π	<4 kHz	6.9 dB	[23]
		DTU	4 × 4	6 mW/π	~kHz	11.5 dB	[24]
		ANT	4 × 4	55 mW/π	\	17.5 dB	[16]
		AMF	8 × 8	35 or 3.05[a] mW/π	<10 kHz	13.36 dB	[15]
	Triplex ($SiN_x + SiO_2$)	Lionix	4 × 4	296 mW/π	\	10.5 dB	[16]
			8 × 8	\	\	8 dB	[20]
			12 × 12	385 mW/π	<kHz	3.4 dB	[21]
			20 × 20	\	\	2.9 dB	[22]
	SiN_x (LPCVD)	Ligentec	4 × 4	<100 mW/π [25]	\	8 dB	[26]
	SiN_x (ICP-CVD)	SYSU	6 × 6	12 mW/π	<kHz	6 dB	This work
Switch	SiN_x (PECVD)	\	4 × 4	130 mW/π	<20 kHz	7.2 dB (TE mode), 5.7 dB (TM mode)	[27]
		\	5 × 5	>300 mW/π	<kHz	8 dB	[28]

IMEC, Interuniversity Microelectronics Center; DTU, Technical University of Denmark; ANT, Applied Nanotools Inc.; AMF, Advanced Micro Foundry; SYSU, Sun Yat-sen University.

[a]With suspended phase shifters.

processors, thereby paving a viable way for their scalable integration.

2. SUSPENDED PHASE SHIFTER WITH LOW POWER CONSUMPTION

Scalability is a crucial limiting factor to the potentials of integrated multiport interferometers. An N-mode MZI-based processor contains $N(N-1)/2$ MZIs and N^2 phase shifters in an N-stage cascaded configuration when employing the Clements structure [10]. The limitation to scalability can be attributed to several factors. The linear increase in propagation path length accumulates non-negligible transmission loss, consequently diminishing the processor's performance. The quadratic growth in the number of tuning components not only rapidly expands the chip footprint and increases the manufacturing cost and reduces the yield, but also introduces significant power consumption that can quickly exceed the typical tolerable on-chip heat dissipation. Despite the advantage of ultra-low waveguide loss, the footprint and dissipation issues are more evident in the SiN_x platform [26], due to its moderate light confinement and low thermo-optic coefficient. To maintain a safe operating temperature, phase shifters on the SiN_x platform necessitate a greater length than those on SOI to accumulate the required phase shift. In the literature, phase shifters in SiN_x photonic processor feature a typical length of 1 mm, with a power consumption per π-phase shift of $P_\pi =$ ~100 mW or more. A reported 20-mode chip [22] would consume ~150 W, assuming all phase shifters are operated at an average power of $P_\pi = 385$ mW [21].

One approach to improve tuning efficiency involves suspending the phase shifters by side trenching and substrate undercutting. This approach significantly reduces the heat leakage due to the very low thermal conductivity of air [0.31 W/(m · K)], which is three orders of magnitude lower than that of silicon [150 W/(m · K)]. On the SOI platform, such an approach has already been extensively reported [29–34] and has also been implemented in PICs with scale [29]. However, to our knowledge, the large-scale application of suspended thermal phase shifters on a silicon nitride platform has yet to be investigated.

A. Fabrication

We design and experimentally evaluate the performance of a suspended thermo-optic phase shifter on our signature ICP-CVD deuterated silicon nitride (SiN_x:D) platform, on which we have demonstrated low propagation loss and soliton frequency combs [35,36]. A SiN_x layer with a thickness of 850 nm is deposited at a fully CMOS-compatible temperature of 270°C on a silicon substrate with 3-μm-thick wet oxide using deuterated silane (SiD_4) and pure nitrogen as the precursor gases. The waveguide thickness is chosen to meet the slightly anomalous dispersion requirement for micro-ring-based photon sources [37,38], allowing potential applications in quantum information processing. Due to the low-stress property of the film deposited by the low-temperature process, the thick SiN_x layer is deposited through one continuous run.

We use an electron beam lithography (EBL) equipment (Raith EBPG 5000+) to define the waveguide patterns in AR-P 6200 resist, followed by a reactive ion etching (RIE) process for pattern transfer. Next, photonic circuits on SiN_x are cladded by an ICP-CVD silica layer with a thickness of 3 μm. By spin coating a layer of AZ 2035 photoresist and etching back, the top cladding is planarized and thinned to the desired thickness of 1.5 μm. Subsequently, heaters in Ni-Cr alloy, as well as wires and electrodes in Au, are successively patterned by EBL and deposited by electron beam evaporation (EBE). In order to maximize mode matching with single mode fiber (SMF), a 700-nm-thick SiO_2 layer is deposited at the edges, after which the chip is cleaved and polished to form the edge couplers. The chip is edge-interfaced using inverse tapers with a 200-nm-wide tip, which provide a coupling efficiency of 2.5 dB per facet to a UHNA7 fiber or a tapered fiber with a 3 μm spot. The spacing of the edge couplers is designed to be 127 μm to be compatible with a fiber array.

An additional post-processing step before the cleaving, as shown in Fig. 1(a), is required to suspend the phase shifters. The pattern of side trenches is defined by optical lithography

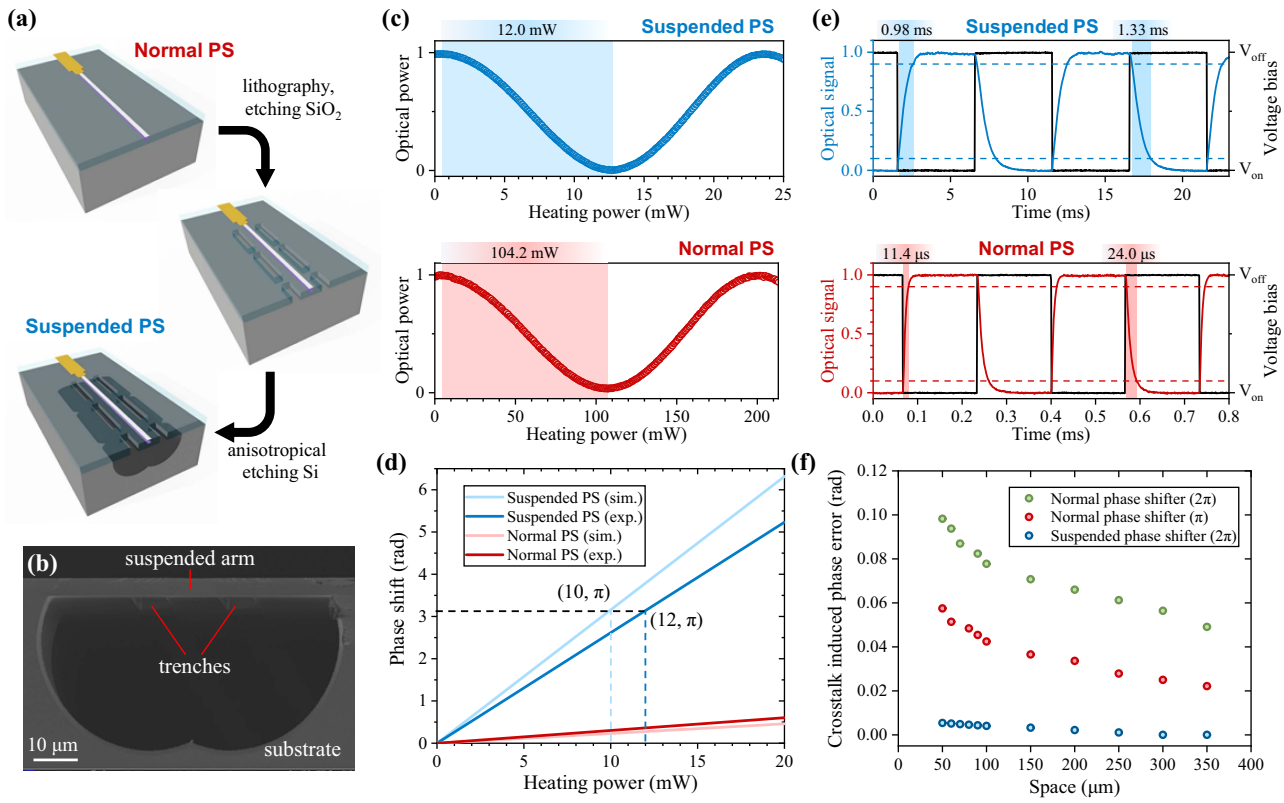

Fig. 1. Fabrication and characterization of the suspended phase shifter. (a) Post process for phase shifter's suspension. (b) The SEM image of a cross-sectional view of a fabricated suspended phase shifter. (c) Normalized optical transmission against the heating power when employing a suspended or a normal phase shifter within the MZI. (d) The numerical and experimental curves of tuning efficiency of suspended and normal phase shifters. (e) The temporal optical response curve of a suspended or a normal phase shifter to square-wave voltage signals. (f) Phase errors induced by thermal crosstalk in both normal and suspended phase shifters.

and then transferred to the SiO_2 layer by RIE. Finally, the Si substrate under the phase shifter is isotropically etched using SF_6 gas in an ICP etching equipment.

The phase shifter is designed with a length of 300 μm, ∼1/3 in length compared with conventional phase shifters with lengths of ∼1 mm. The proposed structure is heat-insulated from the rest of the device layer by side trenches, supported by thin struts spaced at 75 μm, and further insulated from the substrate by undercut etching. In the suspended phase shifter arm, the SiN_x waveguide has cross section of 1.2 μm × 0.85 μm (width × height) on a 3-μm-thick bottom SiO_2 layer. The nickel-chromium (Ni-Cr) alloy heater is positioned directly above the waveguide, separated by the upper cladding layer with a carefully chosen thickness of 1.5 μm. This thickness is the minimum value to avoid significant additional loss due to metal's absorption. The scanning electron microscope (SEM) image of the cross-sectional view of a suspended phase shifter is shown in Fig. 1(b). The silicon substrate is undercut by about 30 μm around the trenches, thoroughly removed under the phase shifter.

B. Characterization

By applying a bias voltage to a phase shifter within an MZI, we obtained the curves of optical power versus heating power for both suspended and normal phase shifters, as illustrated in Fig. 1(c). The simulated and experimental curves of tuning efficiency for both types of phase shifters are summarized in Fig. 1(d). The half-wave power consumption of a suspended phase shifter is measured at $P_\pi \sim 12$ mW, much lower than $P_\pi \sim 104$ mW for a normal one. The slight discrepancy between experiments and simulations may arise from the voltage division of the gold wires, or from errors in material parameters such as thermal conductivity.

The additional effects of thermal insulation are also investigated. First, the limitation on response speed induced by thermal isolation is studied. By applying electrical square-wave signals to the phase shifters within an MZI, their responses in terms of output optical intensity are measured and shown in Fig. 1(e). The response time is measured by the 0.1–0.9 rising or falling edges. The suspended phase shifters feature a response time of ∼1.3 ms, significantly longer than ∼20 μs of our normal phase shifters but comparable to several milliseconds reported in some existing literature [21,28]. A lower tuning speed does not imply a lower computational rate, because even in quasi-static configurations, data carried by photons can undergo high-speed computations when passing through a chip. Since low power consumption is one of the motivations for developing optical computation, the efficiency is more important in cases where high-speed modulation is not a primary requirement. For example, to compensate crosstalk in short-distance multi-input multi-output (MIMO) communication

using a multi-mode fiber, an iteration at every few milliseconds is sufficient due to the low-speed disturbances [39]. We also note that some applications intentionally adopt electronic control signals with rates lower than the device limits, such as the optical neural processor in Ref. [15] operating at kHz and the 12-mode photon interferometer in Ref. [21] controlled at a rate of ∼Hz.

In the context of large-scale PICs based on thermo-optic modulation, exemplified by multi-port interferometers, the thermal crosstalk between adjacent operational components needs to be properly addressed [40–42]. In contrast to a conventional phase shifter, a suspended one operates at a lower power and exhibits stronger thermal localization, thereby reducing the thermal crosstalk significantly. To quantify this effect, we position an additional phase shifter at varied intervals from one arm of an MZI and characterize the crosstalk in terms of phase errors by heating the added phase shifter with power values corresponding to specific phase shifts. As shown in Fig. 1(f), the thermal crosstalk induced by a suspended phase shifter operating at 2π phase shift, with a 50 μm interval, is significantly lower than that of a conventional phase shifter operating at π phase shift with a 350 μm interval. However, in large-scale integration, excessively dense arrangements can lead to the connectivity of substrate cavity. Due to the deformation caused by film stress and lack of mechanical supporting, the suspended area is fragile (see Appendix A). Considering mechanical stability, we set the spacing of the phase shifters to 100 μm in our PICs. This allows significantly higher transverse density compared to the several hundred micrometers needed to avoid significant thermal crosstalk between conventional phase shifters.

3. POWER-EFFICIENT 6-MODE INTERFEROMETER

Figure 2(a) depicts a schematic of a 6-mode photonic processor employed in this work. The adoption of a rectangular architecture, proposed by Clements [10], minimizes the propagation length and guarantees consistent levels of propagation loss across different paths. The processor comprises 15 unit cells, implemented by cascading two 2 × 2 couplers in an MZI structure. Each fundamental unit incorporates both an internal and an external phase shifters, denoted as θ and φ, as illustrated in the subgraph. This configuration allows for the creation of a 2D unitary matrix. When combined, these blocks collectively achieve a unitary SU(6) transformation, converting the input vector into the output vector, written as

$$[O_1, O_2, O_3, O_4, O_5, O_6]^T = \mathrm{SU}(6)[I_1, I_2, I_3, I_4, I_5, I_6]^T. \quad (1)$$

The 6-mode interferometer is fabricated on the same SiN_x:D platform. Figure 2(b) presents the global microscope image of the PIC. Due to the employment of compact phase shifters, each stage of an MZI unit cell is as short as 1400 μm, about half the conventional devices, resulting in a total propagation path of about 1.2 cm. The routing waveguides with a cross section (1.2 μm × 0.85 μm) beyond the single-mode limitation serve to mitigate the scattering loss of the fundamental mode by reducing its mode field with sidewalls. However, it is crucial to employ gradual tapered waveguides and large bending radii (>50 μm) to suppress the higher-order modes.

The experimental test setup is as depicted in Fig. 3(a). We employ a tunable laser as the light source, couple light into (or from) the chip through a tapered fiber with a mode diameter of 3 μm, and use a power meter for output power monitoring. Since our device is polarization-sensitive, we use a fiber polarization controller (FPC) for injecting a fundamental TE mode and fix the fiber to maintain accurate testing. The fabricated PIC is fixed on a copper substrate with printed circuit boards (PCBs) wire-bonded to the on-ship electrodes for power supply. A photograph of this setup is presented in Fig. 3(b).

Due to inherent fabrication imperfections, pre-calibrating the phase bias and tuning efficiency of each phase shifter is necessary. Our initial calibration process focuses on the internal phase shifters, employing the Node Isolation Algorithm [43].

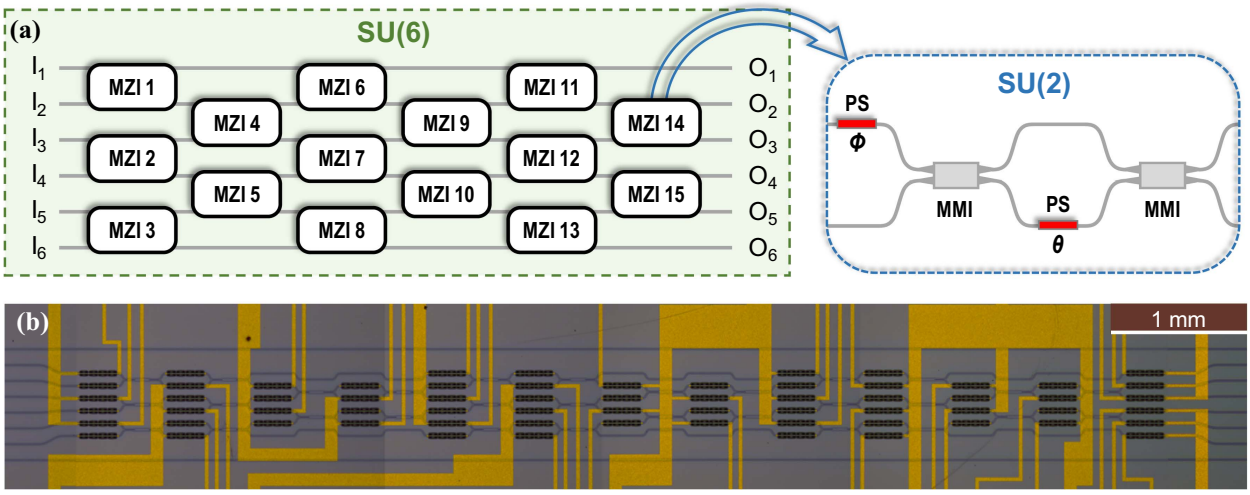

Fig. 2. (a) Schematic diagram of the a 6-mode linear photonic processor using Clements' architecture. (b) Microscope image of the 6-mode interferometer with suspended phase shifters.

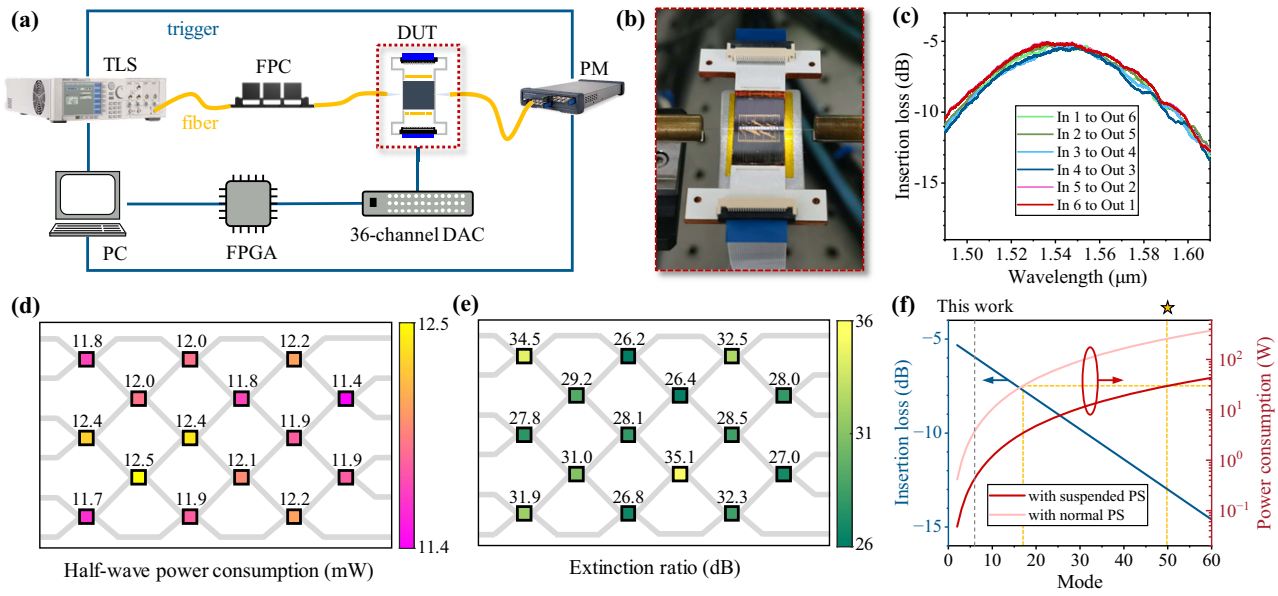

Fig. 3. Calibration and characterization of the device. (a) The experimental testing setup (TLS, tunable laser; FPC, fiber polarization controller; DUT, device under test; PM, power meter; FPGA, field programmable gate array; DAC, digital-to-analog converter). (b) Detailed view of the device under test on a coupling stage. (c) Transmittance spectrum of the calibrated device. (d) Statistics of the half-wave consumption of the internal phase shifters. (e) Statistics of the extinction ratio of all the MZIs. (f) Prediction of insertion loss and power consumption with increasing scale for our device.

To achieve this, we select a specific light path and, while sweeping the internal phase shifter of each MZI along the path, we monitor the output power to establish the relationship between phase and heating power. After all the internal phase shifters are calibrated and set at their unbiased point, the transmission spectra along the routing paths (from Input n to Output $6-n, n=1,2,\ldots,6$) are tested, as illustrated in Fig. 3(c). The curves show a fiber-to-fiber loss of less than −6 dB at the wavelength of 1550 nm. This suggests that the loss within the on-chip circuits is less than −1 dB, with a 1 dB optical bandwidth of approximately 40 nm limited by the cascading of MZIs. Due to the testing flow using single

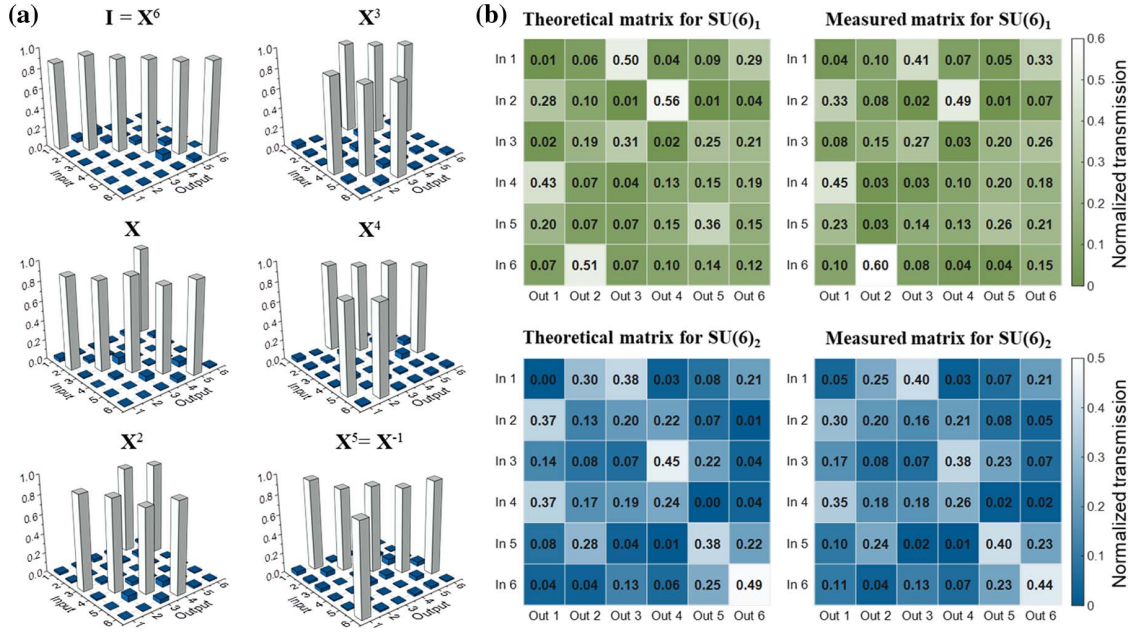

Fig. 4. Experimental 6-mode linear transformation. (a) Measured matrices for all integer powers of 6D cyclic transformations (X-gates). (b) Theoretical and measured transmission matrices of arbitrary 6D unitary transformations $SU(6)_1$ and $SU(6)_2$.

input and single output (SISO), a slight modification is made to calibrate and configure the external phase shifters (see Appendix B for the detailed calibration process).

Subsequently, the modulation efficiency and extinction ratio of each MZI are analyzed using their transmission curves versus power consumption. Figure 3(d) displays the statistical distribution of P_π for the 15 MZIs in the interferometer, with an average value of 12.0 mW and a standard deviation of 0.28 mW. In Fig. 3(e), we present the statistics of switching extinction ratios (ER) for the MZIs monitored at their cross end with an average value of 29.7 dB. It is noteworthy the off-diagonal MZIs [labeled as MZIs 2, 6, 8, 12, 14, and 15 in Fig. 2(a)] might have an actual ER higher than the measured value, because the light incompletely eliminated by preceding stages could deteriorate their measurement results.

The statistics demonstrate good uniformity and repeatability in device manufacturing. For a 6-mode interferometer, the total operational power consumption is 400 mW compared to nearly 3 W in a conventional structure. With the results, we can take an outlook of the performance for a larger scale. In the Clements' structure, because the path as well as the number of MZIs for a photon to propagate through is directly proportional to the mode number N, we can express the insertion loss as IL = $-0.16N - 5$ (dB). Here, the −5 dB comes from the loss of the two edge couplers, and the −0.16 dB accounts for the loss of each stage of MZI with the routing waveguides. We depict the predicted curves for optical loss and operating power with increasing scale in Fig. 3(f). For 50 modes, a photon mode number capable of achieving quantum superiority in Boson sampling, optical loss is predicted to be −13 dB, and the operational power is estimated to be 30 W. The yellow reference lines in the figure indicate that the operational power consumption for 50 modes is equivalent to that of a conventional device operating at 17 modes.

4. DEMONSTRATION OF LINEAR TRANSFORMATIONS

The linear transformation functionality can be achieved by decomposing the matrix into a series of sequence of unitary two-dimensional transformations corresponding to each fundamental block. By injecting light into the input ports in sequence and measuring the transmittance at each output port, the 36 values of normalized power collectively form a 6-dimensional (6D) power matrix. Then the performance can be assessed by comparing this power matrix with the theoretical one.

To assess the consistency between two power matrices, we introduce the root-mean square (RMS) distance [44] expressed as

$$d = \sqrt{\frac{1}{N}\sum_m \sum_n \Delta p_{mn}^2}, \tag{2}$$

where Δp_{mn} is the difference between the elements in the mth row and nth column of the theoretical and measured transmission matrices, and N is the number of elements in each matrix.

An important application of multiport interferometers is the programmable manipulation of high-dimensional quantum states, known as qudits, encoded in the spatial dimension [45,46]. Here, we configure the device to demonstrate 6D cyclic transformation, which has a consistent matrix with a 6D quantum X-gate, described as $\mathbf{X}|j\rangle = |(j+1)\mathrm{mod}6\rangle$. The nth order integer power of cyclic transformation (or X-gate) is denoted as $\mathbf{X}^n$.

Since the cyclic transformation is essentially a switching function, it only requires the internal phase shifters to be set to 0 or π to configure the MZIs to a cross or a bar state. The configurations for integer powers of cyclic transformation are as shown in Appendix C. The transmittances at the wavelength of 1550 nm are tested, normalized, and summarized in Fig. 4(a). The RMS distances of the cyclic transformation for powers 0–5, calculated by Eq. (2), are 0.0381, 0.0420, 0.0439, 0.0426, 0.0487, and 0.0526, respectively, averaged at 0.0446. Referring to the formula for calculating the fidelity of X-gates in Ref. [20], the testing results of X-gates at each order yield a mean fidelity of 95.4%.

To further demonstrate the universality of our device, we randomly generate two 6D linear unitary transformations as the target matrix for our interferometer to construct

$$\mathrm{SU}(6)_1 = \begin{pmatrix} 0.01+0.08i & -0.20+0.14i & 0.68+0.20i & 0.04+0.21i & -0.30-0.05i & 0.40+0.37i \\ 0.38-0.37i & 0.28-0.16i & -0.00+0.08i & 0.16+0.73i & 0.09-0.05i & -0.09-0.19i \\ -0.13-0.08i & 0.38+0.21i & 0.50+0.25i & 0.06-0.11i & 0.30+0.40i & -0.46-0.07i \\ 0.49+0.43i & 0.21+0.16i & -0.20-0.02i & -0.01-0.36i & -0.21+0.33i & -0.03+0.43i \\ -0.27+0.35i & -0.24-0.12i & 0.15+0.21i & 0.39-0.07i & 0.52+0.30i & 0.38+0.07i \\ -0.14+0.22i & 0.49+0.52i & -0.25+0.06i & 0.30+0.09i & 0.11-0.35i & 0.23+0.26i \end{pmatrix},$$

$$\mathrm{SU}(6)_2 = \begin{pmatrix} -0.05+0.01i & 0.28+0.55i & 0.06+0.37i & -0.19-0.57i & 0.16-0.23i & 0.18+0.10i \\ 0.42-0.36i & -0.14+0.38i & 0.29-0.01i & 0.15+0.38i & 0.14-0.51i & -0.03-0.19i \\ -0.17+0.59i & 0.26+0.36i & 0.19-0.18i & 0.37+0.22i & 0.11+0.16i & 0.11-0.34i \\ -0.04-0.16i & 0.26-0.39i & 0.12+0.66i & 0.48+0.10i & 0.08+0.04i & 0.23-0.05i \\ -0.02-0.28i & 0.26-0.01i & 0.31-0.35i & 0.04+0.05i & 0.54+0.30i & 0.09+0.49i \\ 0.46+0.05i & -0.08+0.04i & 0.09-0.18i & 0.13-0.14i & -0.44+0.15i & 0.67+0.20i \end{pmatrix}. \tag{3}$$

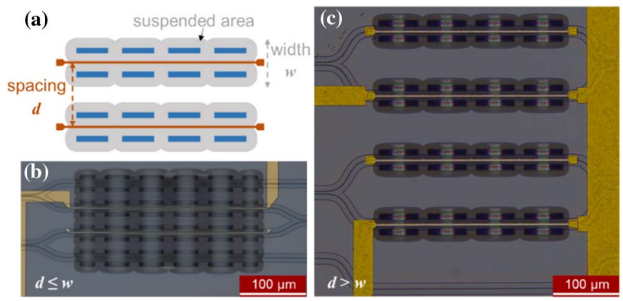

Fig. 5. (a) Schematic of the lateral layout of phase shifters. (b) Phase shifters with a dense lateral arrangement. (c) Phase shifters with a reasonable lateral spacing.

Then we convert the random matrices into phase shift values using the decomposition theory proposed by Clements [10]. For a more comprehensive description of the configuration process and phase lists, please refer to Appendix D. The theoretical and measured power matrices of the random unitary transformations $SU(6)_1$ and $SU(6)_2$ are as shown in Fig. 4(b), exhibiting a maximum error of only 0.09 for an individual element. The RMS distances for $SU(6)_1$ and $SU(6)_2$ evaluated by Eq. (2) are 0.0481 and 0.0341, averaged at 0.0411, indicating the high-quality realization of the target matrices in experiment.

5. CONCLUSION

We report a compact, low-loss, and energy-efficient programmable interferometer with six spatial modes, designed and fabricated on a low-temperature ICP-CVD deuterated SiN_x platform. By utilizing suspended thermo-optic phase shifters, we achieve a significant reduction in power consumption, with approximately 12 mW for a π-phase shift operation, which is an order of magnitude lower than that of existing phase shifters. Furthermore, the outstanding thermal efficiency and minimal thermal crosstalk enable significant reduction in both the length and transverse spacing of the phase shifters, thus increasing component density. The highly uniform distribution of half-wave power and extinction ratio across the chip enables the demonstration of 6D cyclic transformation (or optical switching) and arbitrary unitary matrices functionalities with high fidelity, showcasing the device's good performance. Our research therefore provides a useful approach to address the challenges of power consumption and size constraints in SiN_x-based programmable PICs.

APPENDIX A: DENSITY OF SUSPENDED PHASE SHIFTERS

The width of the suspended area at the bottom of the phase shifter has a width w reaching 50–60 μm, as illustrated in Fig. 5(a). If the lateral spacing of the phase shifters $d \le w$, the cavities in the substrate connect and form a large suspended area, leading to stress deformation as shown by the defocused region in Fig. 5(b). We set $d > w$ to ensure the mechanical stability of each device, as illustrated in Fig. 5(c).

APPENDIX B: CALIBRATION OF EXTERNAL PHASE SHIFTERS

The calibration and configuration of the external phase shifters in an SISO test flow would differ from a multiple-input, multiple-output situation. The proposed Node Isolation Algorithm [43] requires interfering two coherent beams (one through the external phase shifter and one through the reference arm) to calibrate an external phase shifter, which is not applicable to the external phase shifters of MZIs 1–5 with a single input. Here we introduce an equivalent process for calibration and configuration in our SISO testing method.

We start with the matrix realization for rectangular multiport interferometers. According to Clements' proposal, an arbitrary unitary matrix is given by

$$U = DT_{4,5}T_{5,6}T_{2,3}T_{3,4}T_{4,5}T_{5,6}T_{1,2}T_{2,3}T_{3,4}T_{4,5}T_{5,6}T_{1,2}T_{2,3}T_{3,4}T_{1,2}, \tag{B1}$$

where D is a diagonal matrix containing only phase shift elements, and matrix $T_{m,n}$ denotes a two-dimensional operator for a 2D fundamental block lying across the mth and nth rows of waveguides. Their mapping relationships are indicated by

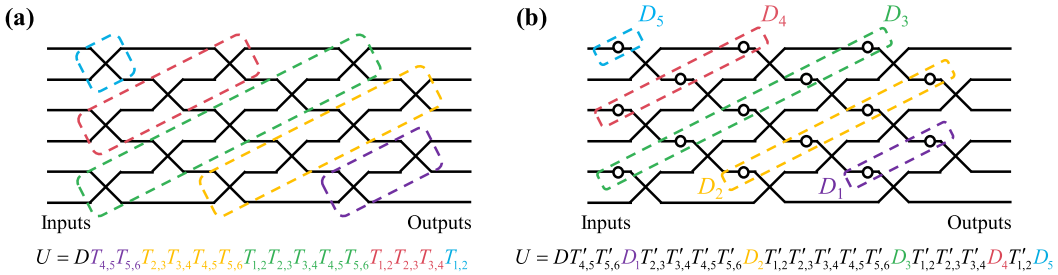

Fig. 6. Schematic diagram of matrix decomposition for a rectangular interferometer. (a) Correspondence of the 2D unit matrices with the basic unit blocks and the order of their multiplication. (b) Connection of external phase shifters in slices.

the dashed boxes and matrices with corresponding color in Fig. 6(a).

Further to this, we extract the external phase shifters from each fundamental block, denoted by the circles in Fig. 6(b), and then the remaining MZI in each block $T_{m,n}$ is denoted by $T'_{m,n}$. Then the decomposition is given by

$$U = DT'_{4,5}T'_{5,6}D_1T'_{2,3}T'_{3,4}T'_{4,5}T'_{5,6}D_2T'_{1,2}T'_{2,3}T'_{3,4}T'_{4,5}T'_{5,6}D_3T'_{1,2}T'_{2,3}T'_{3,4}D_4T'_{1,2}D_5, \tag{B2}$$

where D_j is a diagonal matrix containing a slice of external phase shifters, marked by the dashed boxes in Fig. 6(b). A global phase offset to the phase shifters in the same slice would induce no change to the measured transmission.

We denote the external phase shifter of the kth MZI as PSE_k. Calibration of the external phase shifter of the secondary MZI can be accomplished by splitting the beam at the primary MZI and recombining it at the secondary MZI. Figure 7 presents the specific calibration flow.

First, by injecting light into Input 6, the phase shifters in D_1 and D_2 can be calibrated following the order from the bottom left to the top right, as shown in Figs. 7(a)–7(c).

Next, to calibrate the phase shifters in the slice of D_3, the initial phase of PSE_5 is taken to be zero. PSE_7 is calibrated through a similar "splitting and combining" strategy, as shown in Fig. 7(d). Then, PSE_9 and PSE_{11} are calibrated with the phase reference of the previous stage as shown in Fig. 7(e).

Finally, PSE_6 is calibrated as shown in Fig. 7(f), regarding the initial state of PSE_4 as zero.

APPENDIX C: CONFIGURATION FOR INTEGER POWERS OF CYCLIC TRANSFORMATION

Figure 8 illustrates the method for configuring all integer powers of cyclic transformations, where the MZIs marked with red bars are set to the bar state, while those with blue dots are set to the cross state. It is important to note that only the

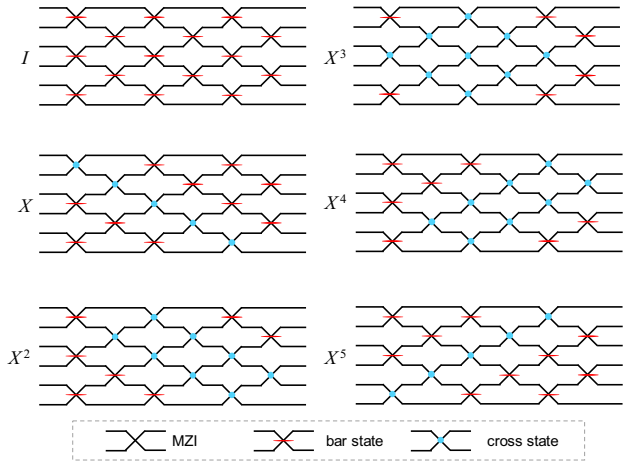

Fig. 8. Configuration for the integer powers of cyclic transformation (X-gate).

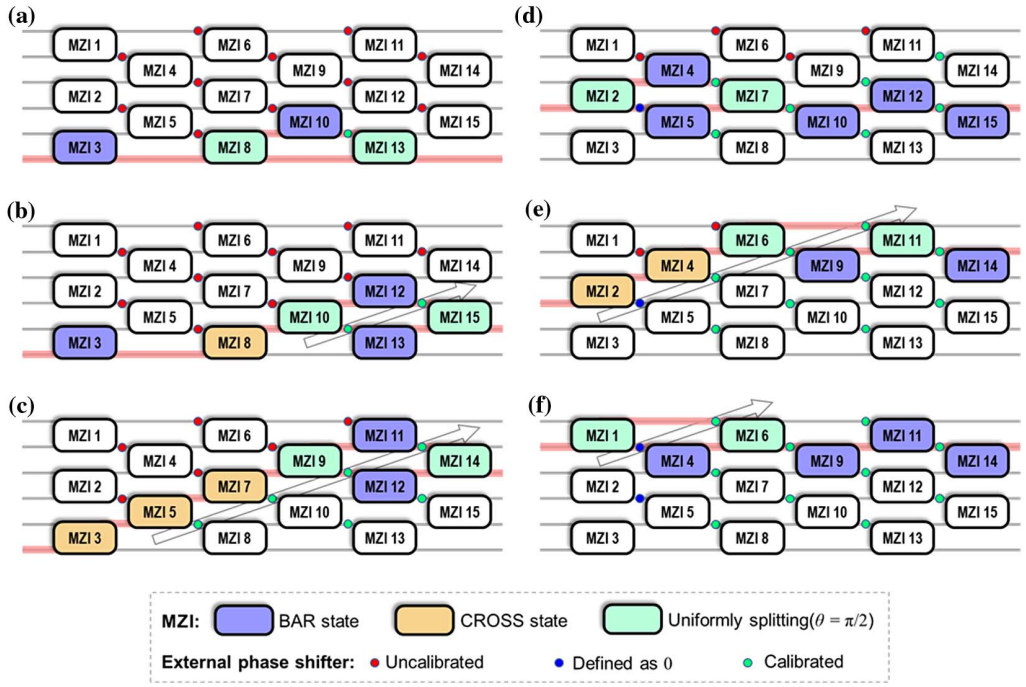

Fig. 7. Calibration flow of the external phase shifters for our SISO testing strategy.

Table 2. Phase Values for Realizing the $SU(6)_1$ Transformation

MZI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
θ	0.0	1.1	1.0	0.4	1.3	1.0	0.4	4.3	5.7	5.2	0.9	6.0	5.7	2.7	4.2
φ	3.4	2.4	5.7	0.1	0.2	3.4	4.5	6.0	0.3	2.8	5.2	1.4	0.0	3.8	5.3
φ'	/	/	/	0	0	3.3	4.3	6.0	0.1	2.8	5.0	1.4	0.0	3.8	5.3

Table 3. Phase Values for Realizing the $SU(6)_2$ Transformation

MZI	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
θ	5.9	6.0	4.4	0.7	1.4	1.5	1.2	0.7	5.0	4.6	1.6	1.0	0.8	4.7	4.0
φ	0.6	3.8	4.8	0.3	5.6	0.8	0.0	1.0	2.1	2.0	1.6	4.5	2.7	2.5	1.3
φ'	/	/	/	0	0	0.5	0.7	1.0	2.7	2.0	2.3	4.5	2.7	2.5	1.3

internal phase shifts require adjustment. For a cross state, the internal phase shifts should be set to 0, whereas for a bar state, they should be set to π.

APPENDIX D: REALIZATION OF ARBITRARY SU(6)

The random matrices $SU(6)_1$ and $SU(6)_2$ are translated into the phase values θ (internal) and φ (external). Then the phase values of phase shifters in D_3 and D_4 are subtracted by φ_4 and φ_5, respectively, to yield a final external phase list φ', as presented in Tables 2 and 3. With this equivalent method, we can skip the calibration and configuration of the PSE_1–PSE_5 while realizing the same transmission matrices of $SU(6)_1$ and $SU(6)_2$.

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