

PHOTONICS Research

Time-space multiplexed photonic-electronic digital multiplier

WENKAI ZHANG,¹ BO WU,¹  WENTAO GU,¹ JUNWEI CHENG,¹ HAILONG ZHOU,^{1,2} LIAO CHEN,¹ WENCHAN DONG,¹  JIANJI DONG,^{1,*}  AND XINLIANG ZHANG¹ 

¹Wuhan National Laboratory for Optoelectronics, Huazhong University of Science and Technology, Wuhan 430074, China

²e-mail: hailongzhou@hust.edu.cn

*Corresponding author: jjdong@hust.edu.cn

Received 6 November 2023; revised 25 December 2023; accepted 8 January 2024; posted 9 January 2024 (Doc. ID 511389); published 1 March 2024

Optical computing has shown immense application prospects in the post-Moore era. However, as a crucial component of logic computing, the digital multiplier can only be realized on a small scale in optics, restrained by the limited functionalities and inevitable loss of optical nonlinearity. In this paper, we propose a time-space multiplexed architecture to realize large-scale photonic-electronic digital multiplication. We experimentally demonstrate an 8×2 -bit photonic-electronic digital multiplier, and the multiplication with a 32-bit number is further executed at 25 Mbit/s to demonstrate its extensibility and functionality. Moreover, the proposed architecture has the potential for on-chip implementation, and a feasible integration scheme is provided. We believe the time-space multiplexed photonic-electronic digital multiplier will open up a promising avenue for large-scale photonic digital computing. © 2024 Chinese Laser Press

<https://doi.org/10.1364/PRJ.511389>

1. INTRODUCTION

Amidst the fast-paced growth of the artificial intelligence and communication industry, the demand for computing resources has surged dramatically. Traditional electronic hardware gradually exhibits the great constraint in accommodating these escalating computing requirements, primarily due to the electronic natural limits of signal processing speed, parallel capacity, and power consumption. To alleviate this bottleneck, photonic computing has emerged as a promising solution, which provides the fast speed for signal processing, multiple dimensions for multiplexing (wavelength, mode, polarization, etc.), and high energy efficiency for data processing [1–4].

Photonic computing can be categorized into two domains: photonic analog computing [5–7] and photonic digital computing [8–10]. Despite impressive breakthroughs in photonic analog computing, it still struggles to excel in high-precision computational scenarios. The analog computing nature along with the noise from optical circuits and the surrounding environment leads to relatively high inaccuracy of results, severely impacting the computing performance and efficiency [11]. In contrast, photonic digital computing offers higher noise tolerance and compatibility with common electronic computer architecture. However, most existing works can only support some simple logic functions such as AND, XOR operations [12–15], one or two-bit adders [16,17], comparators [18–20], and multipliers [21–23]. The limitations of optical

nonlinear functionalities and inevitable loss reveal great challenges to execute large-scale digital computing like addition and multiplication. Recently, a feasible way has been proposed to realize a scalable adder based on photonic-electronic computing architecture [24]. As for the multiplier, a large-bit-width computing architecture still remains null.

In this paper, we present a scalable photonic-electronic digital multiplier based on the time-space multiplexed strategy. The two input operands are encoded in time and space dimensions, respectively. By cascading intensity modulators (IMs) to perform AND operation, we obtain the partial products between two operands while loading signals, and then combine them with corresponding delays, thereby achieving the intensity superposition. The mixed signal is then input into the decimal to binary converter (DBC), whose high-bit outputs are delayed by optical waveguides and fed back into the mixed signal to perform the carry propagation, and lowest-bit output is the final result of the multiplier. We design a proof-of-concept experiment to demonstrate the proposed scheme using an electronic analog to digital converter (ADC) instead of the DBC. The 8×2 -bit photonic-electronic digital multiplier and the multiplication with a 32-bit number are experimentally executed at 25 Mbit/s to demonstrate its extensibility and functionality. There are also potential optical ways to implement the DBC, such as the photonic crystal ADC [25–27] and the optical-electrical-optical (OEO) method mentioned in the discussion section. In addition, an $n \times n$ -bit

photonic-electronic multiplier architecture is discussed, which can be integrated on a single photonic chip. The proposed method provides a novel paradigm for the optical digital multiplier and explores new opportunities for large-scale photonic logic computing architecture.

2. PRINCIPLE

Typically, the multiplication procedure can be divided into two steps: partial product generation and summation. Figure 1(a) depicts the architecture of the time-space multiplexed photonic-electronic digital multiplier. Considering the current optical frequency comb (OFC) technique has been widely applied in photonic systems with a sufficient number of wavelengths and stable working state [28–30], it can serve as a multi-wavelength light source to provide required wavelengths for the multiplier. We encode two input operands in time and space dimensions, respectively. The input operand A ($A_n \dots A_3 A_2 A_1$) is loaded in a sequence of timestamps whose period equals τ . The total number of timestamps corresponds to the bit width of the operand A. And each bit of the input operand B ($B_n \dots B_3 B_2 B_1$) is loaded in different wavelengths ($\lambda_n \dots \lambda_3 \lambda_2 \lambda_1$) by n individual IMs with the duration time of $n\tau$. To generate the partial products, logic AND operation between two input operands is necessary. The cascading IMs shown in Fig. 1(b) provide a favorable way to execute logic AND while loading signals. Only when both input signals are Logic 1, the output optical signal can be Logic 1, corresponding to the AND operation between A_i and B_j . Figure 1(c) depicts the generated partial products of 4×4 -bit multiplication unfolded in time and space dimensions. Here, we treat the time delay of signals as a form of carry. The time delay of $(j - 1)\tau$ is

introduced to achieve the targeted carry for partial products related to B_j . By multiplexing the time and space dimensions, the number of required IMs is linearly related to the bit width of the multiplier, greatly enhancing its scalability.

Having generated the partial products, a wavelength division multiplexer (WDM) is utilized to combine them together. Note that we adopt the WDMs to demultiplex and multiplex multiple wavelengths instead of the multimode interferometer to avoid the coherent superposition of the optical signals. The mixed signal is then input into a DBC, which can convert the multi-level signal into the binary form $C^m \dots C^2 C^1 C^0$. Except for the lowest bit, all remaining channels of DBC are looped back as carry signals into the mixed signal. The k th-bit output undergoes a time delay of $k\tau$. And the number of carry signals m satisfies the following relationship with the bit width n of the multiplier:

$$n + 1 \leq 2^{m+1} - m. \quad (1)$$

Figure 1(d) shows the summation procedure of the generated partial products. The DBC's outputs $C^2 C^1$ are mixed with the partial products after corresponding time delays to realize carry propagation. By this means, the lowest bit output of DBC C^0 can directly serve as the final bitstream of the multiplier.

3. RESULTS

To validate the proposed principle, a proof-of-concept experiment is implemented as shown in Fig. 2(a). Constrained by the inevitable optical fibers and radio frequency cables to connect all the discrete components, the minimum time delay cannot be reduced to support a high-speed data stream. As a result, we decide to set the multiplication speed at 25Mbit/s. The 8×2 -bit multiplication is first demonstrated. The input operand of 8 bits is encoded in the time dimension, and the

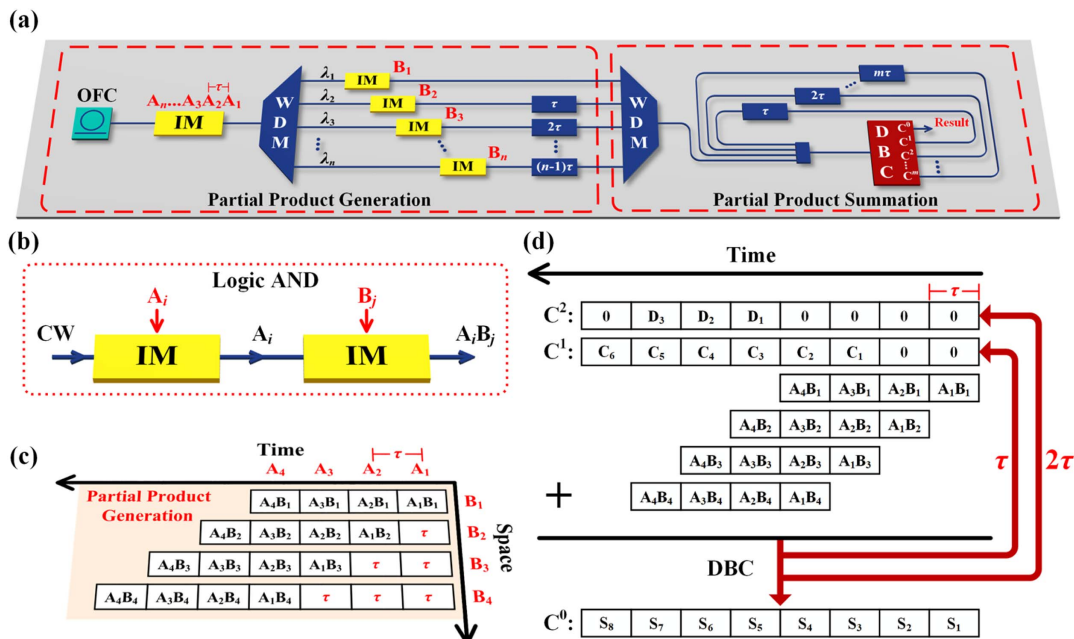


Fig. 1. Principle of the time-space multiplexed photonic-electronic digital multiplier. (a) Schematic of the proposed multiplier architecture. (b) Logic AND operation realized by two cascading IMs. (c) The generated partial products of 4×4 -bit multiplication unfolded in the dimensions of time and space. (d) The summation procedure of the generated partial products. OFC, optical frequency comb; IM, intensity modulator; WDM, wavelength division multiplexer; DBC, decimal to binary converter; CW, continuous wave.

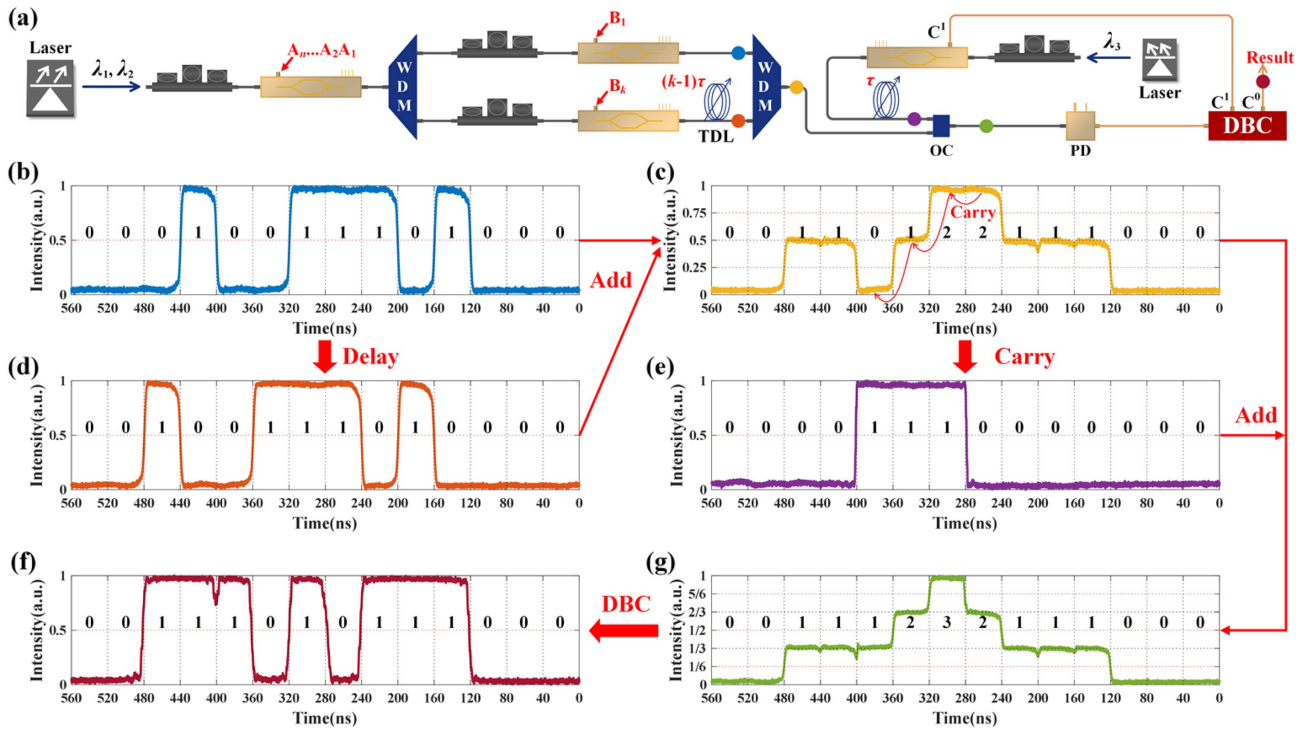


Fig. 2. Experimental results of the 8×2 -bit multiplication for $10,011,101 \times 11$ at 25 Mbit/s. (a) Experimental setup to realize photonic-electronic digital multiplier. The circles in the diagram represent the waveforms with the same color detected at those points. (b) and (d) Waveforms of generated partial products related to B_1 and B_2 , respectively. (c) Waveform of the mixed signals after WDM. (e) and (f) Waveforms of the DBC's output ports C^1 and C^0 , respectively. (g) Waveform of the combination between partial products and carry by OC. OC, optical coupler; TDL, tunable delay line; PD, photodetector.

operand of 2 bits is encoded in the space dimension. We load input signals by IMs (Fijitsu H74M-5210-J128), whose bandwidth is 10 GHz and static extinction ratio is 32 dB. Two wavelengths λ_1 (1549.3 nm) and λ_2 (1550.1 nm) are utilized to generate the partial products. Figures 2(b) and 2(d) show the generated partial products related to B_1 and B_2 , respectively. The time delay of the tunable delay line (TDL) $(k - 1)\tau$ determines the bit width of operand B and is set to delay τ here. The TDL is composed of several optic fiber patch cords with a minimum length of 0.1 m. By controlling the total length of fibers, we can adjust the TDL to the desired delay. After the generation of partial products in the optical domain, a WDM is followed to combine them together and outputs the mixed signal as depicted in Fig. 2(c). For the summation part, the input signal of the DBC has at most four levels (0, 1, 2, 3) in the 8×2 -bit multiplication. Hence a 2-bit DBC is adequate for the task of binarizing the signal. We utilize an electronic ADC to perform the function of 2-bit DBC by quantizing the input signal. Since the ADC's minimum input voltage is about 5 mV, a bias-tee is used to provide the bias voltage for the electronic signal from PD. The decision voltage interval of the ADC is about 20 mV, which means the ADC will output 00 (C^1C^0) when the input voltage is between 5 mV and 25 mV and output 11 when the input voltage is between 65 mV and 85 mV. According to these decision voltage levels, we control the light intensity in each optical channel and the bias voltage of the bias-tee so that the ADC responds accurately to the PD's output signal with different levels. The voltages of ADC's input signals are adjusted

to about 15 mV, 35 mV, 55 mV, 75 mV corresponding to four input levels 0, 1, 2, 3, and ADC's output ports C^1C^0 will output 00, 01, 10, 11 under these four input voltages, respectively. The output voltage of the ADC is 500 mV, which cannot drive the IM directly. Therefore, we add a microwave amplifier to enable the signal from the output port C^1 to drive the IM, thereby converting the electronic carry information into light information. We combine the carry signal with a time delay of τ [shown in Fig. 2(e)] and the mixed partial products together by an optical coupler to realize the carry propagation. The final optical signal [Fig. 2(g)] is fed into the DBC through a PD to obtain final results of the multiplication from the output port C^0 [Fig. 2(g)], which is consistent with the theoretical calculation ($111,010,111 = 10,011,101 \times 11$).

We further expand the multiplier's scale in the time dimension. By increasing the encoding length of A, the setup can perform the multiplication with an input operand of 32 bits. Figures 3(a) and 3(b) present the results of two 32×2 -bit multiplication operations. The 32-bit operand can cover nearly 4.3×10^9 numbers, greatly increasing the application range of photonic digital multipliers. And it is quite easy to achieve a larger bit width of operand A, which only needs to encode a longer signal in the time dimension. Moreover, we can change the bit width of operand B by extending the time delays of the generated partial products. As shown in Figs. 3(c) and 3(d), a 32-bit binary number is multiplied by a 3-bit binary number of 101 and a 4-bit binary number of 1001, where the corresponding time delay is set to 2τ and 3τ , respectively.

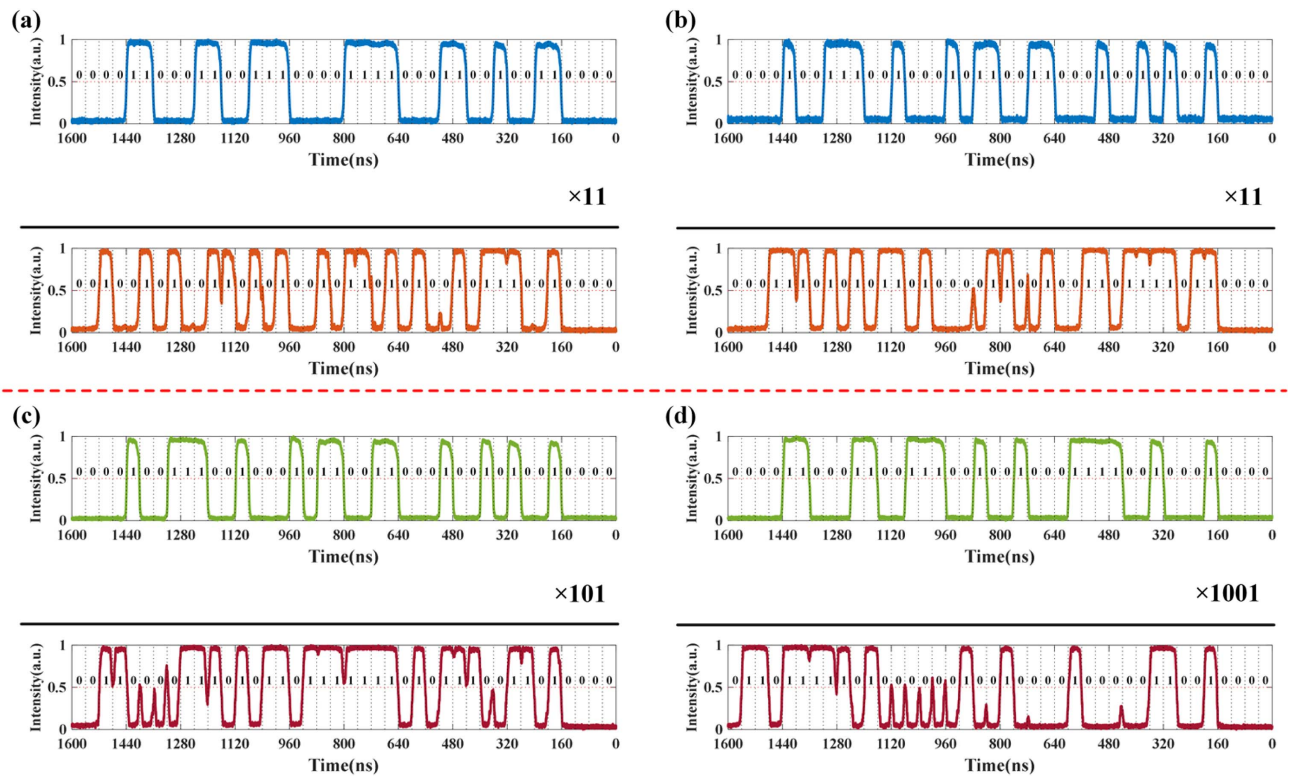


Fig. 3. Experimental results of the photonic-electronic digital multiplier with an input operand of 32 bits. (a) and (b) Multiplication results between a 32-bit binary number $A_{32}...A_2A_1$ and a 2-bit binary number 11. (c) Multiplication results between a 32-bit binary number and a 3-bit binary number 101. (d) Multiplication results between a 32-bit binary number and a 4-bit binary number 1001.

4. DISCUSSION

As the OEO method has been widely used in both optical analog computing and digital computing [31–34], we propose a feasible way to realize one-step multi-bit DBC shown in Fig. 4(a) by the OEO method. The input optical signal of the $(m + 1)$ -bit DBC has t intensity levels, following the relationship by

$$t = 2^{m+1}, \quad (2)$$

which will drive the PD to output t different electric current levels depicted in Fig. 4(b). The electronic signal will change

the position of the microring resonator's (MRR's) resonance peak. We can input the wavelengths at corresponding resonance peak positions shown in Fig. 4(c) and use wavelength filters to obtain the desired wavelengths from the drop port of MRR. Take the example of a 2-bit DBC. For the output port C^1 , it needs to output light when the input signal is at Level 2 (10) or Level 3 (11). Therefore, the wavelengths at those resonance peak positions (Level 2 and Level 3) will be filtered out. Similarly, for the output port C^0 , it will output the wavelengths corresponding to Level 1 (01) and Level 3 (11). The scale of the proposed OEO DBC depends on the number of wavelengths

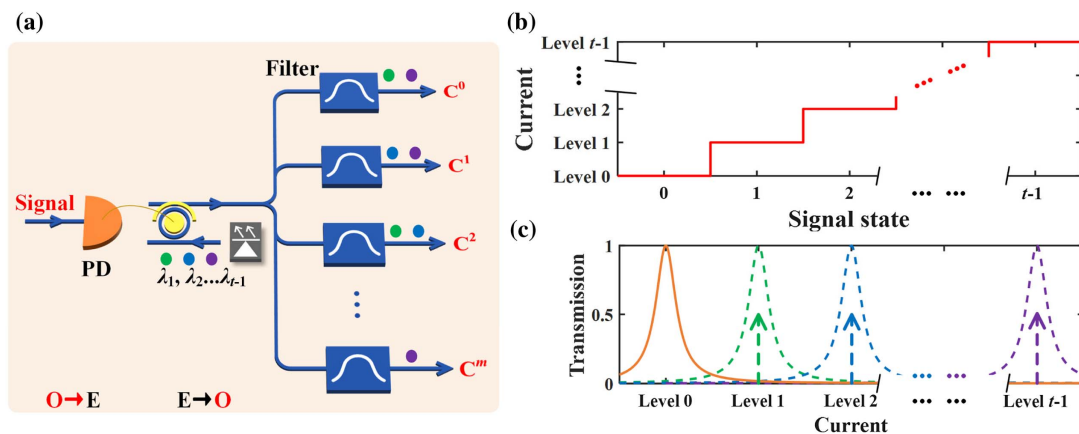


Fig. 4. One-step multi-bit DBC realized by the OEO method. (a) Sketch map of multi-bit DBC. (b) The input signal's state and the corresponding output current level of the PD. (c) Transmission spectrum of the MRR's drop port under different input signal levels and the input wavelengths.

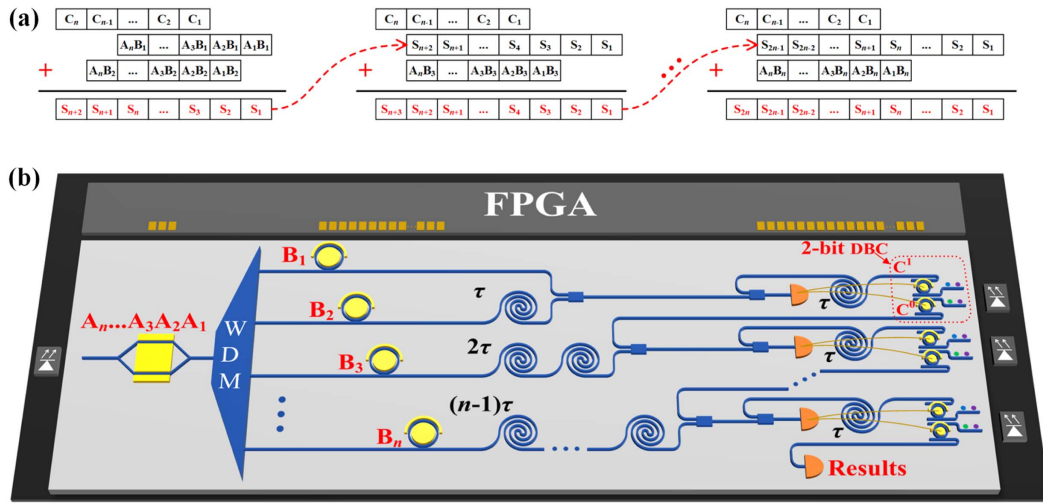


Fig. 5. Integration scheme of the time-space multiplexed photonic-electronic digital multiplier. (a) Step-by-step summation of the partial products. (b) Schematic diagram of the on-chip photonic-electronic digital multiplier. FPGA, field programmable gate array.

the MRR supports to modulate, which is mainly affected by the following factors. First, the free spectrum range (FSR) of the MRR constrains the wavelength range the DBC can contain. It is preferred to design the MRR with a small radius for large FSR. Second, the MRR's Q factor influences the minimum interval of DBC's input wavelengths. The sharper the MRR's resonance peak is, the smaller wavelengths' interval can be set to guarantee the satisfactory extinction ratio of DBC's output port, which will allow for more wavelengths within a certain wavelength range. Third, the transimpedance amplification capability of MRR's drive circuit determines the moving range of MRR's resonance peak. The light current from the PD is required to be amplified and converted into voltage signal, thereby modulating the MRR. To make the MRR's resonance peak move further, the drive circuit needs to output the signals with higher voltage.

The implementation of DBC can be also simplified by employing a step-by-step summation method to calculate the sum of partial products. Figure 5(a) shows the procedure involving $n - 1$ summations of two addends, which needs $n - 1$ 2-bit DBCs and avoids the use of multi-bit DBC. Figure 5(b) presents the schematic diagram of the on-chip photonic-electronic digital multiplier. We can utilize two independent MRRs to execute the function of DBC's output ports C^1 and C^0 , respectively. The desired outputs are realized via controlling input wavelengths of MRRs. By this means, the wavelength filter can be omitted. Despite the increase of delay lines and PDs, the step-by-step summation method can reduce the requirements for the design of DBC compared with the one-step DBC, which will make the realization of the photonic-electronic digital multiplier more feasible. Considering signal A needs to be loaded at different wavelengths simultaneously, the corresponding IM can be implemented with the on-chip Mach-Zehnder modulator (MZM) [35–37], which supports parallel modulation of multiple wavelengths. As for signal B, each bit is modulated at one independent wavelength. To achieve more compact integration, we can select the high speed MRRs to load signal B [38–40]. The integrated WDM can be realized by the on-chip arrayed waveguide grating (AWG)

[41–43]. And the time delay can be introduced by the on-chip delay lines [44,45]. The integrated structure shortens the feedback time for carry signals, enabling a higher computing speed of the proposed multiplier. Here, we give an area estimation of an 8×8 -bit digital multiplier of 10 Gbit/s, which includes one MZM ($3 \text{ mm} \times 0.5 \text{ mm}$), one eight-channel AWG ($1 \text{ mm} \times 1 \text{ mm}$), eight MRRs ($0.05 \text{ mm} \times 0.05 \text{ mm}$), all delay lines (3 mm^2), eight PDs ($0.03 \text{ mm} \times 0.05 \text{ mm}$), and seven 2-bit DBCs with corresponding drive circuit (0.5 mm^2). Assuming the above components account for about 70% of the total area, the multiplier chip will occupy an area of 13 mm^2 . We can utilize an external field programmable gate array (FPGA) circuit to load signals and obtain computation results while maintaining the chip's operational state. The OEO scheme of the 2-bit DBC alleviates the impact of optical transmission loss within the chip, making it possible to realize large-scale multipliers.

5. CONCLUSION

In conclusion, we propose a time-space multiplexed multiplier architecture capable of performing large-scale digital multiplication. By encoding the two input operands in the time and space dimensions, the required components are linearly related to the bit width of the multiplier. We experimentally implement a photonic-electronic multiplier to compute the results of an 8×2 -bit input at 25 Mbit/s. And the multiplication with a 32-bit number is further demonstrated to verify its capability of performing large-scale computations. We also provide two integration schemes with one-step summation and step-by-step summation methods, respectively. The proposed multiplier greatly expands the scale of existing photonic digital multiplication and paves the way for the large-scale optical digital computing.

Funding. National Key Research and Development Program of China (2023YFB2806502); National Natural Science Foundation of China (62075075, 62275088,

U21A20511); Innovation Project of Optics Valley Laboratory (OVL2021BG001).

Disclosures. The authors declare no competing financial interests.

Data Availability. All the data related to this paper are available from the corresponding author upon request.

REFERENCES

- H. Zhou, J. Dong, J. Cheng, *et al.*, "Photonic matrix multiplication lights up photonic accelerator and beyond," *Light Sci. Appl.* **11**, 30 (2022).
- C. Li, X. Zhang, J. Li, *et al.*, "The challenges of modern computing and new opportunities for optics," *Photonix* **2**, 20 (2021).
- K.-I. Kitayama, M. Notomi, M. Naruse, *et al.*, "Novel frontier of photonics for data processing—photonic accelerator," *APL Photon.* **4**, 090901 (2019).
- D. A. Miller, "Attojoule optoelectronics for low-energy information processing and communications," *J. Lightwave Technol.* **35**, 346–396 (2017).
- K. Vandoorne, P. Mechet, T. Van Vaerenbergh, *et al.*, "Experimental demonstration of reservoir computing on a silicon photonics chip," *Nat. Commun.* **5**, 3541 (2014).
- D. Pierangeli, G. Marucci, and C. Conti, "Large-scale photonic Ising machine by spatial light modulation," *Phys. Rev. Lett.* **122**, 213902 (2019).
- X. Xu, M. Tan, B. Corcoran, *et al.*, "11 TOPS photonic convolutional accelerator for optical neural networks," *Nature* **589**, 44–51 (2021).
- J. Hardy and J. Shamir, "Optics inspired logic architecture," *Opt. Express* **15**, 150–165 (2007).
- R. A. Athale and S. H. Lee, "Development of an optical parallel logic device and a half-adder circuit for digital optical processing," *Opt. Eng.* **18**, 513–517 (1979).
- Y. Wang, X. Zhang, J. Dong, *et al.*, "Simultaneous demonstration on all-optical digital encoder and comparator at 40 Gb/s with semiconductor optical amplifiers," *Opt. Express* **15**, 15080–15085 (2007).
- C. Wu, X. Yang, H. Yu, *et al.*, "Harnessing optoelectronic noises in a photonic generative network," *Sci. Adv.* **8**, eabm2956 (2022).
- H. Qi, Z. Du, X. Hu, *et al.*, "High performance integrated photonic circuit based on inverse design method," *Opto-Electron. Adv.* **5**, 210061 (2022).
- K. Li, H.-F. Ting, M. A. Foster, *et al.*, "High-speed all-optical NAND/AND logic gates using four-wave mixing Bragg scattering," *Opt. Lett.* **41**, 3320–3323 (2016).
- H. Mondal, K. Goswami, M. Sen, *et al.*, "Design and analysis of all-optical logic NOR gate based on linear optics," *Opt. Quantum Electron.* **54**, 272 (2022).
- K. Goswami, H. Mondal, P. Das, *et al.*, "Realization of ultra-compact all-optical logic AND Gate based on photonic crystal waveguide," in *Advances in Communication, Devices and Networking: Proceedings of ICCDN* (Springer, 2022), pp. 61–68.
- Z. Ying, Z. Wang, Z. Zhao, *et al.*, "Silicon microdisk-based full adders for optical computing," *Opt. Lett.* **43**, 983–986 (2018).
- J. Dong, S. Fu, X. Zhang, *et al.*, "Single SOA based all-optical adder assisted by optical bandpass filter: theoretical analysis and performance optimization," *Opt. Commun.* **270**, 238–246 (2007).
- Y. Tian, H. Xiao, X. Wu, *et al.*, "Experimental realization of an optical digital comparator using silicon microring resonators," *Nanophotonics* **7**, 669–675 (2018).
- K. Komatsu, G. Hosoya, and H. Yashima, "Ultrafast all-optical digital comparator using quantum-dot semiconductor optical amplifiers," *Opt. Quantum Electron.* **51**, 39 (2019).
- C. Feng, Z. Ying, Z. Zhao, *et al.*, "Toward high-speed and energy-efficient computing: a WDM-based scalable on-chip silicon integrated optical comparator," *Laser Photon. Rev.* **15**, 2000275 (2021).
- W. Dong, L. Lei, L. Chen, *et al.*, "All-optical 2x2-bit multiplier at 40 Gb/s based on canonical logic units-based programmable logic array (CLUs-PLA)," *J. Lightwave Technol.* **38**, 5586–5594 (2020).
- M. Liaghati-Rad, M. Soroosh, and A. Kosarian, "High-speed all-optical 2-bit multiplier based on photonic crystal structure," *Photon. Netw. Commun.* **43**, 193–203 (2022).
- S. Kumar, A. Bisht, G. Singh, *et al.*, "Implementation of 2-bit multiplier based on electro-optic effect in Mach–Zehnder interferometers," *Opt. Quantum Electron.* **47**, 3667–3688 (2015).
- Z. Ying, C. Feng, Z. Zhao, *et al.*, "Electronic-photonic arithmetic logic unit for high-speed computing," *Nat. Commun.* **11**, 2154 (2020).
- M. Mohammadi, F. Habibi, M. Seifouri, *et al.*, "Recent advances on all-optical photonic crystal analog-to-digital converter (ADC)," *Opt. Quantum Electron.* **54**, 192 (2022).
- S. Ramtin Fard, M. R. Salehi, and E. Abiri, "Ultra-fast all-optical ADC using nonlinear ring resonators in photonic crystal microstructure," *Opt. Quantum Electron.* **53**, 120 (2021).
- F. Mehdizadeh, M. Soroosh, H. Alipour-Banaei, *et al.*, "All optical 2-bit analog to digital converter using photonic crystal based cavities," *Opt. Quantum Electron.* **49**, 38 (2017).
- H. Shu, L. Chang, Y. Tao, *et al.*, "Microcomb-driven silicon photonic systems," *Nature* **605**, 457–463 (2022).
- L. Chang, S. Liu, and J. E. Bowers, "Integrated optical frequency comb technologies," *Nat. Photonics* **16**, 95–108 (2022).
- J. Cheng, Y. Xie, Y. Liu, *et al.*, "Human emotion recognition with a microcomb-enabled integrated optical neural network," *Nanophotonics* **12**, 3883–3894 (2023).
- C. Huang, S. Fujisawa, T. F. de Lima, *et al.*, "A silicon photonic–electronic neural network for fibre nonlinearity compensation," *Nat. Electron.* **4**, 837–844 (2021).
- F. Ashtiani, A. J. Geers, and F. Aflatouni, "An on-chip photonic deep neural network for image classification," *Nature* **606**, 501–506 (2022).
- A. N. Tait, T. F. De Lima, M. A. Nahmias, *et al.*, "Silicon photonic modulator neuron," *Phys. Rev. Appl.* **11**, 064043 (2019).
- R. Soref, F. De Leonardis, Z. Ying, *et al.*, "Silicon-based group-IV OEO devices for gain, logic, and wavelength conversion," *ACS Photon.* **7**, 800–811 (2020).
- P. Dong, L. Chen, and Y.-K. Chen, "High-speed low-voltage single-drive push-pull silicon Mach-Zehnder modulators," *Opt. Express* **20**, 6163–6169 (2012).
- M. Li, L. Wang, X. Li, *et al.*, "Silicon intensity Mach–Zehnder modulator for single lane 100 Gb/s applications," *Photon. Res.* **6**, 109–116 (2018).
- J. S. RG, "High modulation efficient silicon MZM with core-based split PN junction phase shifter," *Silicon* **14**, 7033–7041 (2022).
- Q. Xu, B. Schmidt, S. Pradhan, *et al.*, "Micrometer-scale silicon electro-optic modulator," *Nature* **435**, 325–327 (2005).
- X. Xiao, H. Xu, X. Li, *et al.*, "25 Gbit/s silicon microring modulator based on misalignment-tolerant interleaved PN junctions," *Opt. Express* **20**, 2507–2515 (2012).
- Q. Xu, S. Manipatruni, B. Schmidt, *et al.*, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," *Opt. Express* **15**, 430–436 (2007).
- P. Cheben, J. Schmid, A. Del age, *et al.*, "A high-resolution silicon-on-insulator arrayed waveguide grating microspectrometer with sub-micrometer aperture waveguides," *Opt. Express* **15**, 2299–2306 (2007).
- T. Ye, Y. Fu, L. Qiao, *et al.*, "Low-crosstalk Si arrayed waveguide grating with parabolic tapers," *Opt. Express* **22**, 31899–31906 (2014).
- T. Fukazawa, F. Ohno, and T. Baba, "Very compact arrayed-waveguide-grating demultiplexer using Si photonic wire waveguides," *Jpn. J. Appl. Phys.* **43**, L673–L677 (2004).
- H. Lee, T. Chen, J. Li, *et al.*, "Ultra-low-loss optical delay line on a silicon chip," *Nat. Commun.* **3**, 867 (2012).
- Y. Xie, S. Hong, H. Yan, *et al.*, "Low-loss chip-scale programmable silicon photonic processor," *Opto-Electron. Adv.* **6**, 220030 (2023).