PHOTONICS Research

High-efficiency reflector-less dual-level silicon photonic grating coupler

Valerio Vitali,[1,2,*] Thalía Domínguez Bucio,[1] Cosimo Lacava,[2] Riccardo Marchetti,[3] Lorenzo Mastronardi,[1] Teerapat Rutirawut,[1] Glenn Churchill,[1] Joaquín Faneca,[1,4] James C. Gates,[1] Frederic Gardes,[1] and Periklis Petropoulos[1]

[1]Optoelectronics Research Centre, University of Southampton, Southampton, SO17 1BJ, UK
[2]Electrical, Computer and Biomedical Engineering Department, University of Pavia, 27100 Pavia, Italy
[3]Advanced Fiber Resources Milan S.r.l., 20098 San Donato Milanese, Italy
[4]Currently at Instituto de Microelectrónica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain
*Corresponding author: valerio.vitali@unipv.it

Received 1 March 2023; revised 29 April 2023; accepted 6 May 2023; posted 9 May 2023 (Doc. ID 488970); published 26 June 2023

We present the design and experimentally demonstrate a dual-level grating coupler with subdecibel efficiency for a 220 nm thick silicon photonics waveguide which was fabricated starting from a 340 nm silicon-on-insulator wafer. The proposed device consists of two grating levels designed with two different linear apodizations, with opposite chirping signs, and whose period is varied for each scattering unit. A coupling efficiency of −0.8 dB at 1550 nm is experimentally demonstrated, which represents the highest efficiency ever reported in the telecommunications C-band in a single-layer silicon grating structure without the use of any backreflector or index-matching material between the fiber and the grating.

https://doi.org/10.1364/PRJ.488970

1. INTRODUCTION

Silicon photonics leverages the mature and monolithic processing techniques inherited from microelectronics to achieve the fabrication of highly integrated optical chips at a wafer-scale level [1,2]. Thanks to the strong refractive index contrast between the Si core ($n_{Si} = 3.48$ at 1550 nm) and the SiO_2 cladding ($n_{SiO_2} = 1.44$ at 1550 nm) achieved in the silicon-on-insulator (SOI) platform, single-mode waveguides with tight bending radii [3,4] can be fabricated. As a result, and because of the SOI compatibility with CMOS processes and the possibility to fabricate low-cost and high-performance optical devices, interest in silicon photonics has continued to grow and covers a wide range of research fields including all-optical processing [5,6], sensing [7,8], metrology [9], and quantum technologies [10,11]. However, an important challenge that remains in silicon photonics is the efficient fiber-to-chip coupling, which originates from the significant dimension difference between the optical fiber [with a mode field diameter (MFD) of 10.4 μm for a standard single-mode fiber (SMF-28)] and the integrated SOI waveguides (which have a typical cross section of 500 nm × 220 nm) [12].

To tackle this challenge, the two most widely adopted solutions are based on the use of edge couplers (ECs) and grating couplers (GCs). ECs enable remarkably low coupling losses (<0.5 dB is achievable) over a wide wavelength range (>100 nm) and can be realized using different configurations such as inverse tapers, multi-layer structures [13], or subwavelength grating metamaterial mode expanders [14] located at the chip facets. Although this approach is effective in achieving a high coupling efficiency (CE), it is not suitable for wafer-scale automated testing and high-volume production, since ECs require accurate post-fabrication processes, such as high-quality polishing of the chip facets and precise optical alignment. Conversely, GCs represent a better coupling interface for rapid wafer-scale testing because they can be fabricated anywhere on the chip surface and are characterized by much more relaxed alignment tolerances compared to those achievable using ECs [12]. However, standard uniform grating couplers (UGCs) typically show a narrow 1 dB bandwidth (BW) (usually in the range of 30–40 nm) and poor CE, which is usually lower than −2.2 dB [12]. Several design and fabrication techniques have been reported in the literature to overcome this limit and increase the CE of SOI GCs, whose best results in the telecommunications C-band are summarized in Table 1.

In general, the CE is proportional to the GC directionality (defined as the percentage of the optical power that is scattered from the direction of the waveguide and GC upwards toward the optical fiber) and GC-fiber mode matching, and inversely proportional to the reflectivity at the waveguide–GC interface. Directionality enhancement can be achieved by employing different techniques, such as a staircase design with dual- or multi-etching depths [32,34,41] or the use of poly-silicon [17,19,42]

Table 1. Summary of the Best Numerically Simulated (CE_S) and Experimentally Measured (CE_E) Coupling Efficiencies Reported in the Literature for Different GCs in the C-Telecom Band[a]

Si [nm]	Description	CE_S [dB]	CE_E [dB]	Ref.	Si [nm]	Description	CE_S [dB]	CE_E [dB]	Ref.
220	GA*	−2.15	–	[15]	220	GA*	−1.9	–	[16]
220	GA + DBR*	−0.36	–	[15]	220[b]	Dual-level	−0.28	−0.8	This work
220	Poly-Si overlay	−1.08	–	[17]	250	Full-etch PhC	−1.8	−1.74	[18]
220	Poly-Si overlay*	–	−1.6	[19]	250	Lag effect etch*	−1.31	−1.9	[20]
220	Linear apodiz.	−2.6	−2.7	[21]	250	Linear apodiz.	−2.2	−2.7	[22]
220	Gold BR	−1.43	−1.61	[23]	250	Aluminum BR*	−0.33	−0.5	[24]
220	DBR*	−0.86	−1.58	[25]	250	Aluminum BR*	−0.33	−0.62	[26]
220	Linear apodiz.	−1.6	–	[27]	250	Aluminum BR	−0.43	−0.58	[28]
220	DBR*	−1.02	–	[29]	260	Linear apodiz.	−0.8	−0.9	[27]
220	Si overlay*	−1.8	−2.6	[30]	260	GA*	−1.0	–	[16]
220	Ge overlay	−1.19	–	[31]	300	Dual-etch	−0.25	–	[32]
220	Dual-etch	−1.24	−2.2	[33]	300	Dual-etch	−2.2	−2.7	[34]
220	Dual-etch	−1.05	–	[35]	340	GA*	−0.5	–	[16]
220	Dual-etch	−1.1	−1.3	[36]	340	Apodized GC	−0.76	−1.2	[37]
220	Aluminum BR	−0.67	−0.69	[38]	340	Apodized GC	–	−1	[39]
220	SWG+prism	−0.5	−1.0	[40]	340	Apodized GC*	–	−0.7	[39]

[a]The symbol * in the Description columns indicates the use of an index-matching material between the fiber and the GC.
GA, genetic algorithm; DBR, distributed Bragg reflector; BR, backreflector; SWG, subwavelength grating; PhC, photonic crystal.
[b]220 nm thick Si waveguide fabricated starting from a 340 nm SOI wafer.

or germanium (Ge) [31] over-layers. For example, CE values as high as −0.36 dB [43] and −0.85 dB [44] in devices designed for 1200 nm and 1300 nm, respectively, were experimentally demonstrated using a bi-layer GC with a poly-silicon overlay and a 5 μm MFD lensed fiber. Another common approach to increase the GC directionality is the use of backreflectors (BRs) embedded in the substrate, either based on metallic mirrors [23,24,26,28,38] or distributed Bragg reflectors (DBRs) [15,25]. As can be seen from Table 1, GCs with embedded BRs typically outperform all other solutions in the telecom C-band. However, this approach presents some limitations and difficulties from a fabrication perspective. Regarding the use of metallic mirrors, the fabrication of metal BRs may require the adoption of non-CMOS compatible materials which can be unviable in a metal-free fabrication environment [28]. As for DBRs, they can be fabricated using a stack of several amorphous Si and SiO_2 layers, but this requires additional fabrication steps and may result in low fabrication tolerances and large difference from the simulated performance [25]. Therefore, GC designs that do not require the use of BRs are generally preferable.

An effective way to increase the CE is the application of an apodization profile, which can tailor the amount of power scattered by each grating period so as to decrease the mode mismatch between the field profile radiated by the GC and the Gaussian-like fiber mode. Apodization also results in a reduction of the backreflection at the waveguide–GC interface. It is typically performed by varying either the fill factor of each period [15–17,21,22,26–28,37,45] or the etching depth [20]. Two main design strategies are usually employed, and sometimes combined, to perform a GC apodization. In the first approach, numerical simulations, commonly based on genetic algorithms, are used to define the apodization profile by maximizing a specific figure of merit (generally the CE) [26]. The second approach makes use of analytical expressions to tailor the apodization profile and match the power-distribution profile of the optical fiber. An example is the use of a linear apodization, in which one of the GC parameters (e.g., the fill factor) is linearly chirped while keeping the other parameters constant (or modifying them accordingly) [27]. In addition to these techniques, to avoid loss of power due to reflections at the air interface, an index-matching material between the fiber and the GC can be used, which typically results in a CE increase of about 0.3 dB [24,39].

In this work, we propose and experimentally demonstrate an apodized dual-level GC for a 220 nm thick SOI platform with a measured CE of −0.8 dB. To the best of our knowledge, this represents the highest CE ever achieved in the telecommunications C-band for SOI GCs without the use of any BR or index-matching material between the fiber and the grating. The proposed structure consists of two grating levels where two different linear apodizations, with opposite signs, are applied. The bottom and top gratings have the same period, whose value is varied for each scattering unit to ensure that the Bragg condition is satisfied along the entire GC length. The GC was fabricated starting from a 340 nm thick SOI wafer by means of two etching steps, which allowed achieving a dual-level configuration without the need of depositing an additional poly-Si overlay. An additional etching step was performed to define 500 nm × 220 nm single-mode waveguides and linear tapers to connect two GCs together to allow their characterization. Thanks to its versatility, the presented design strategy can in principle be applied to any SOI thickness or other integrated photonic platforms.

2. GRATING COUPLER LAYOUT

In standard UGCs, trenches with a fixed length L_e and constant etching depth e are etched in the Si waveguide with a period Λ. By defining the grating fill factor F as the ratio between the tooth length L_o (the un-etched section of the period) and the total length Λ of the scattering unit, it is possible to express the effective refractive index n_{eff} of the GC as follows:

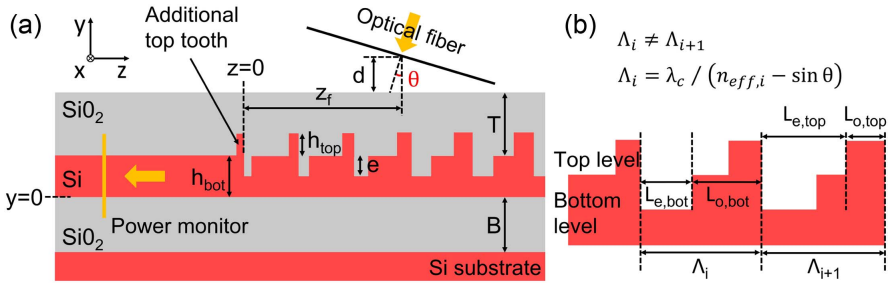

Fig. 1. (a) 2D schematic view and simulation layout of the proposed dual-level Si GC; (b) cross-sectional schematic with the parameter names used to indicate the GC dimensions.

$$n_{\text{eff}} = F \cdot n_o + (1 - F) \cdot n_e, \tag{1}$$

where n_o and n_e are the effective refractive indices of the original Si slab and the etched section, respectively. The periodic variation in the effective refractive index between the trenches and the un-etched teeth results in the diffraction of the optical mode propagating in the Si waveguide to free space at a certain angle. According to the first-order Bragg condition, the GC period Λ can be calculated as

$$\Lambda = \frac{\lambda_c}{n_{\text{eff}} - \sin\theta}, \tag{2}$$

where λ_c is the coupling wavelength and θ is the diffraction angle in air. As previously mentioned, a linear apodization of the F factor can help increase the CE thanks to an improvement in the GC-fiber mode matching and a reduction in the optical impedance mismatch between the waveguide and the grating section [16]. In most of the linearly apodized GC demonstrations reported in the literature, Λ is kept constant along the whole grating length [16,21,22]. As we discussed in our previous work [27], this approach does not allow for the Bragg condition to be simultaneously satisfied by all of the scattering units: as the F parameter is varied along the GC, the effective refractive index n_{eff} of each grating element changes, and therefore the Bragg law is satisfied only at a specific position of the GC but not along its whole length. To mitigate this issue, we proposed a new design methodology based on the simultaneous linear apodization of F and a corresponding variation of Λ along the GC length, so as to satisfy the Bragg condition along the whole structure.

While keeping these considerations into account, the design we present in this work aims at further improving the CE by maximizing the GC directionality. The schematic layout of the apodized dual-level SOI GC proposed here is shown in Figs. 1(a) and 1(b). The bottom level, which acts as the light guiding level, has a thickness h_{bot} and an etching depth e, while the top GC level has a thickness h_{top} and is fully etched. For each radiative unit, the two GC levels have the same period Λ and their teeth are aligned on the furthermost border. The fill factors of the two levels are defined by two linear apodization functions, with opposite chirping signs. This architecture ensures that the design objective of increasing directionality is achieved, while facilitating the reduction of the mode mismatch thanks to the GC apodization. The following expression is used to apodize the bottom GC:

$$F_{\text{bot}} = F_{\text{in,bot}} - R_{\text{bot}} \cdot z, \tag{3}$$

in which $F_{\text{in,bot}}$ is the initial fill factor of the first bottom radiative unit, R_{bot} stands for the bottom linear apodization factor, and z is the distance of each radiative unit from the start of the GC. The starting position of the GC is indicated by $z = 0$ in Fig. 1(a), while the end point corresponds to the last period of the GC (not shown in the figure). In a similar way, the equation used to define the apodization of the top level is the following:

$$F_{\text{top}} = F_{\text{in,top}} + R_{\text{top}} \cdot z, \tag{4}$$

in which $F_{\text{in,top}}$ is the initial fill factor of the first top radiative unit and R_{top} stands for the top linear apodization factor. An additional tooth in the top level, whose width was set equal to the minimum dimension achievable in our fabrication process (60 nm), is added before the first GC period to increase the CE, as already discussed in Refs. [45–47].

The adoption of two linear apodizations with opposite signs for the two levels has two main benefits: the first is that it allows minimizing the backreflection at the GC interface and the mismatch between the bottom Si mode and the composite dual-level GC mode [45]. The second benefit is that it reduces the space of simulation variables: since the values of $F_{\text{in,bot}}$ and $F_{\text{in,top}}$ are constrained by the minimum feature dimension achievable in fabrication and the common period Λ is recalculated for each scattering unit using Eqs. (1)–(3), the tooth and trench lengths for both levels are defined only by two variables, namely R_{bot} and R_{top}. This allows exploring a broad variable space and a large number of possible GC configurations by simultaneously varying the dimensions of both levels; this is in contrast to previously reported designs where each grating period and fill factor were optimized independently [46]. Considering a thickness of $h_{\text{bot}} = 220$ nm for the bottom Si level and $B = 2$ μm for the bottom SiO_2 layer, the other free GC parameters to be optimized are e, h_{top}, and the thickness of the top SiO_2 cladding (TOX) T. A standard SMF-28 optical fiber was considered, with an outer diameter of 125 μm and an MFD of 10.4 μm at 1550 nm. The angle of incidence θ was set equal to 14.5° with respect to the vertical direction to help reduce any backreflections into the fiber [27]. The point of the optical fiber closest to the TOX surface was set at a distance of 0.5 μm, corresponding to a distance between the center of the optical fiber core and the TOX surface $d = 16.15$ μm for $\theta = 14.5°$ [see Fig. 1(a)]. Therefore, the only fiber parameter to

be optimized is the offset z_f, i.e., the distance of the central position of the fiber to the start of the GC.

3. DESIGN METHODOLOGY AND SIMULATIONS

The design of the dual-level GC was carried out in three steps. In the first step, only the bottom GC level was considered [setting $h_{top} = 0$ referring to Fig. 1(a)]: a linear apodization of the fill factor was applied [see Eq. (3)] and Λ was varied along the whole structure to satisfy the Bragg condition for $\lambda_c = 1550$ nm in each point of the GC. Concerning the choice of $F_{in,bot}$, it has been shown that increasing its value (and, thus, decreasing the first bottom trench width), results in an increase in the grating CE [22]. Considering a minimum feature size of 60 nm, which is compatible with the use of E-beam lithography, we set the value of $F_{in,bot}$ equal to 0.9. The optimal values for e and R_{bot} that maximize the CE of the bottom GC were then found by performing a set of full vectorial 2D-FDTD simulations using FDTD Solutions (from ANSYS Inc.). Specifically, the CE was calculated by modeling the GC as an in-coupling device, i.e., coupling power from the fiber into the SOI waveguide by means of the grating [see the simulation layout of Fig. 1(a), considering $h_{top} = 0$ for this first design step]. The electric field polarization of the Gaussian beam was set along the $\hat{x}$ direction, which resulted in the incoming optical power being coupled to the fundamental TE mode of the SOI waveguide. A frequency-domain power monitor was used to calculate the total power coupled in the fundamental TE waveguide mode and, hence, the grating CE. For each value of the $e - R_{bot}$ pair of parameters, the value of the fiber offset z_f was also optimized. This was performed by sweeping z_f from 3 to 10 μm at 0.2 μm steps for each combination of the $e - R_{bot}$ pair of parameters and by selecting the fiber offset value z_f maximizing the GC CE. The results of the parameter sweep for the bottom GC level with $h_{bot} = 220$ nm are reported in Fig. 2(a), which shows a contour plot of the peak CE at 1550 nm as a function of the e and R_{bot} parameters. A maximum CE equal to −1.59 dB can be achieved by setting $e = 110$ nm and $R_{bot} = 0.0275$ μm^{-1}, with the optimized fiber offset z_f value equal to 6.2 μm. A full vectorial 3D-FDTD simulation was then performed on the optimum single-level GC to account for the grating width and verify the GC performance. Figure 2(b) shows the resulting CE as a function of wavelength λ for the optimized single-level GC considering a grating width in the $\hat{x}$ direction of 14 μm, with a peak CE at 1550 nm of −1.67 dB and a 1 dB BW of 34.8 nm.

A major factor contributing to the CE reported above for the optimum single-level GC is the directionality of the grating, which was calculated to be equal to 72.6% at 1550 nm. To address this, in the second design step, the top grating level was added and its impact on the overall GC performance was investigated. The parameters of the bottom grating were set equal to those of the optimum configuration found in the first step. A linear apodization of the fill factor, with a chirping sign opposite to the one of the bottom level, was applied to the top level [see Eq. (4)]. In order to minimize the mode mismatch between the waveguide mode and the dual-level GC mode, a small dimension for the first top tooth is required [45]. Therefore, by considering a smallest feature of 60 nm as before, the value of $F_{in,top}$ was set to 0.1. Since the top level is fully etched and has the same period as the bottom grating for each scattering element, the only two top GC parameters that need to be optimized are h_{top} and R_{top}. To get a complete understanding of the effect of these two parameters on the overall performance, the grating was initially simulated as an out-coupling device. A fundamental TE mode source was set in the SOI waveguide and a power monitor was positioned above the GC to evaluate its directionality. Specifically, a 1D horizontal power monitor was placed at $y = 1.6$ μm spanning from $z = -2$ μm to $z = 17$ μm [see Fig. 1(a) for the Cartesian axes] to collect all of the optical power scattered upwards by the GC. Figure 3(a) shows the directionality of the dual-level GC at 1550 nm as a function of h_{top} and R_{top}. As can be seen, the addition of the top level enables directionality values in excess of 96%, showing a significant improvement compared to the case of the best-performing single-level GC (directionality at 1550 nm equal to 72.6%). Moreover, it can be noticed that directionality values greater than 90% can be achieved over a large range of the h_{top} parameter, from 50 to 140 nm.

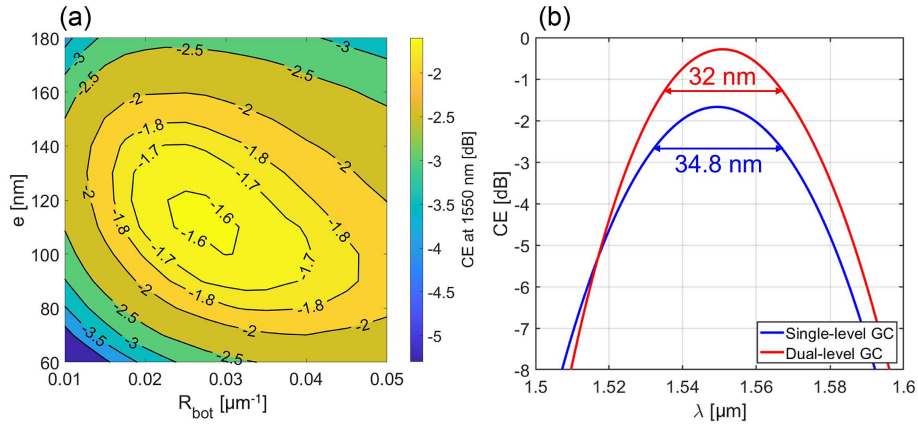

Fig. 2. (a) 2D numerical simulations of the CE at 1550 nm as a function of the bottom linear apodization factor R_{bot} and the etching depth e considering a single-level GC with a waveguide thickness $h_{bot} = 220$ nm. Other parameters used in the simulations are $B = 2$ μm, $F_{in,bot} = 0.9$, $\theta = 14.5°$, and $T = 720$ nm. (b) 3D numerical simulations of the CE as a function of wavelength for the best-performing single-level and dual-level GC considering $h_{bot} = 220$ nm.

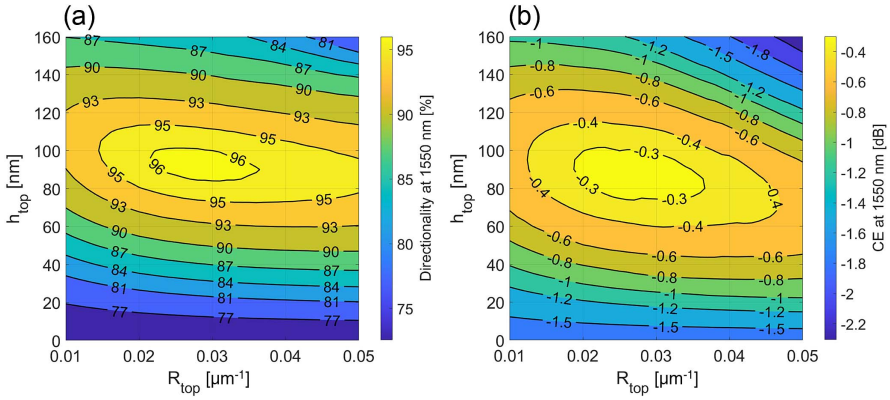

Fig. 3. 2D numerical simulations of (a) directionality and (b) CE at 1550 nm as a function of the top linear apodization factor R_{top} and thickness of the top level h_{top} for a dual-level GC with $h_{bot} = 220$ nm. Other parameters used in the simulations are $e = 110$ nm, $R_{bot} = 0.0275$ μm^{-1}, $B = 2$ μm, $F_{in,bot} = 0.9$, $F_{in,top} = 0.1$, $\theta = 14.5°$, and $T = 720$ nm.

The increased directionality can be explained considering that the addition of the top level further "breaks" the GC symmetry compared to the case of the partially etched single-level GC and, therefore, it allows for properly designing the GC structure to maximize the diffracted contribution in the upward direction and minimize the optical power scattered toward the substrate [12], as in the case of blazed GCs [48]. The CE of the dual-level GC was then simulated for the same parameter range modeling the grating as an in-coupling device, as in the first design step, with the final results shown in Fig. 3(b). A maximum CE of −0.27 dB can be achieved at 1550 nm by setting $h_{top} = 90$ nm and $R_{top} = 0.025$ μm^{-1}. It is interesting to note that a CE greater than −0.6 dB (which is 1 dB greater compared to the optimum single-level GC case) can be achieved across a wide range of h_{top} – R_{top} combinations, thus showing relaxed fabrication tolerances.

In the third design step, a final particle swarm optimization (PSO) was carried out on the parameter space $\{R_{bot}, R_{top}, T, z_f\}$ to further increase the CE by setting e and h_{top} to the best values found in the previous two steps. In this work, we set $h_{top} = 120$ nm due to the availability of SOI wafers with a Si thickness of 340 nm in our cleanroom. Considering $e = 110$ nm, a peak CE of −0.19 dB was found with the PSO algorithm (using 2D-FDTD numerical simulations) for $R_{bot} = 0.03$ μm^{-1}, $R_{top} = 0.02$ μm^{-1}, $T = 600$ nm, and $z_f = 6.6$ μm. The GC dimensions for each period of the optimized structure are listed in Table 2, while Fig. 2(b) shows the results of the final 3D-FDTD simulation carried out considering a grating width of 14 μm, exhibiting a peak CE of −0.28 dB and a 1 dB BW of 32 nm. The addition of the top grating level results in a CE increase of 1.39 dB compared to the optimum single-level GC. The tolerance of the GC performance to a deviation of the fiber offset from the optimized value $z_f = 6.6$ μm was then calculated for the final dual-level configuration. A 1 dB BW of the CE equal to 5.2 μm around the central value $z_f = 6.6$ μm was numerically simulated, showing a good tolerance of the GC CE to the fiber misalignment. Finally, the use of an index-matching material (refractive index 1.444) between the optical fiber and the TOX surface was considered. A 3D-FDTD simulation that was carried out considering the final dual-level GC design with a grating width of 14 μm resulted in the same peak CE value of −0.28 dB as in the case of an air gap, with an increased 1 dB BW equal to 33.9 nm. The fiber angle was changed to 10.5° to have the GC response centered at 1550 nm and the optimized fiber offset value z_f was calculated to be equal to 6.4 μm. This demonstrates the possibility to use the proposed device in a packaged system, where the use of an epoxy layer may be required to secure the fiber position on the chip surface.

Table 2. Optimal Dimensions (Common Period Λ, Bottom Tooth Width $L_{o,bot}$, and Top Tooth Width $L_{o,top}$) Obtained from the Optimization of the Apodized Dual-Level Si GC with Waveguide Thickness $h_{bot} = 220$ nm and Top Level Thickness $h_{top} = 120$ nm[a]

No.	Λ [nm]	$L_{o,bot}$ [nm]	$L_{o,top}$ [nm]	No.	Λ [nm]	$L_{o,bot}$ [nm]	$L_{o,top}$ [nm]
1	610	549	61	13	643	434	161
2	613	540	69	14	646	424	170
3	616	532	77	15	649	413	179
4	618	522	85	16	652	402	188
5	621	513	93	17	656	392	198
6	623	503	101	18	659	381	208
7	626	494	109	19	662	369	217
8	629	484	117	20	665	358	227
9	632	475	126	21	669	347	237
10	635	465	134	22	672	335	247
11	637	454	143	23	675	323	257
12	640	444	152	24	679	311	268

[a]The additional tooth in the top level which is added before the first GC period has a width equal to 60 nm.

4. DEVICE FABRICATION AND CHARACTERIZATION

To experimentally measure the CE of the dual-level GC, we fabricated structures consisting of two GCs connected by a 1 cm long straight single-mode waveguide with a width of 500 nm and a thickness equal to 220 nm. Linear tapers with 500 μm length were used to connect the GCs to the single-mode waveguides. In order to isolate the contributions of the

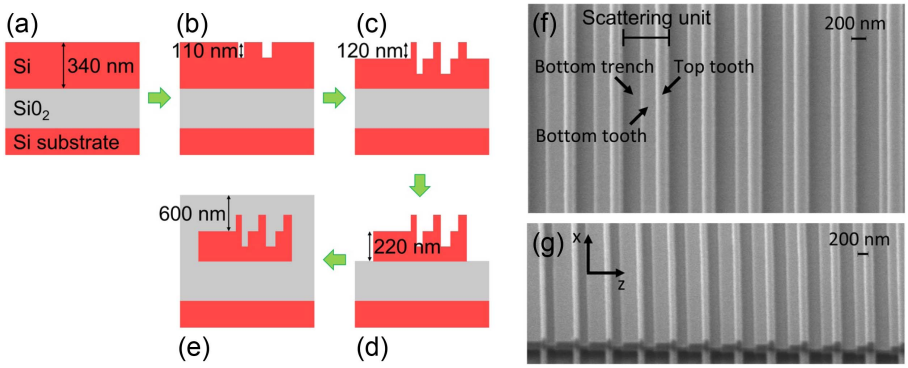

Fig. 4. Fabrication process diagram for the dual-level GC: (a) starting from SOI wafer with a Si thickness of 340 nm; (b) bottom GC level etching; (c) top GC level etching; (d) waveguide etching; (e) SiO_2 cladding deposition. (f) Top-view and (g) angled-view SEM images of a fabricated device.

GC losses from the waveguide propagation losses, a set of spiral waveguides (cross section: 500 nm × 220 nm) with different lengths was fabricated to perform cut-back measurements. The fabrication process flow for the designed GC devices is outlined in Fig. 4. The test structures were fabricated using a 200 mm SOI wafer with a 340 nm thick Si layer and a 2 μm buried oxide layer as a starting substrate [Fig. 4(a)]. The bottom [Fig. 4(b)] and top [Fig. 4(c)] grating levels were defined using two E-beam lithography steps with a high-resolution 200 nm thick ZEP520A resist and were then transferred to the Si layer in two separate reactive ion etching (RIE) steps, based on a SF_6:C_4F_8 chemistry, with an etching depth of 110 and 120 nm, respectively. An additional E-beam lithography step with a 600 nm thick ZEP520A resist and an RIE etching step with a 220 nm etch depth [Fig. 4(d)] were performed to define linear tapers and single-mode strip waveguides connecting two GCs together to allow their experimental characterization. Finally, the dual-level GC was covered with a 600 nm thick SiO_2 cladding [Fig. 4(e)] deposited through plasma-enhanced chemical vapor deposition. Figures 4(f) and 4(g) show scanning electron microscope (SEM) images with a top view and angled view of a fabricated device, respectively, in which it is possible to appreciate the staircase structure and the apodizations with opposite chirping signs applied to the two levels.

Experimental measurements were performed by using a vertical coupling scheme with polarization-maintaining (PM) SMF-28 fibers to properly couple light into the fundamental TE mode of the waveguide. Both fibers were tilted at an angle of 14.5° with respect to the vertical direction. A PM external cavity laser was used as the optical source, while a power meter was employed to record the output power collected from the device under test. No index-matching fluid was used between the fibers and the sample TOX. Figure 5 shows the measured CE as a function of wavelength for the dual-level GC. A peak CE of −0.8 dB at a wavelength of 1558 nm and a 1 dB BW of 31.3 nm were measured. Considering that the tooth and trench dimensions of both levels measured by critical dimension SEM well matched the nominal design dimensions, the 8 nm shift of the GC response toward longer wavelengths may be the result of several contributions such as a non-perfect quality of the

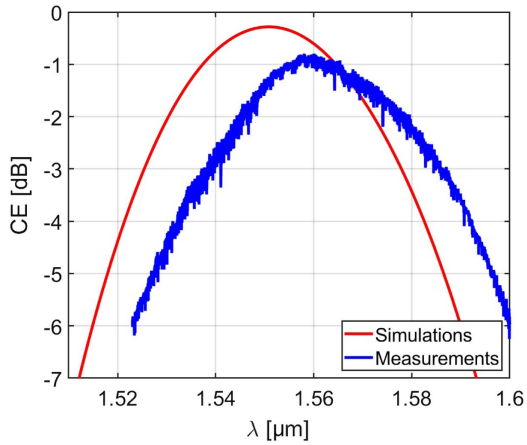

Fig. 5. Simulated (red curve) and experimentally measured (blue curve) CE as a function of wavelength for the fabricated dual-level GC with a bottom waveguide thickness $h_{bot} = 220$ nm and top-level thickness $h_{top} = 120$ nm.

optical fiber facets in the vertical coupling setup (e.g., dependent on the quality of the fiber cleaving) or a slight tilt in the fiber angles relative to the nominal 14.5° value used in the simulations. Another possible reason may be an under-etch in the two etching steps employed to define the dual-level GC geometry [see Figs. 4(b) and 4(c)]. In particular, according to numerical simulations, an etching depth 2.5 nm smaller than the nominal one for the two etching steps results in an 8 nm redshift of the central wavelength of the GC response.

5. CONCLUSIONS

In this paper, we reported the experimental demonstration of an apodized dual-level GC for a 220 nm silicon photonics platform which was fabricated starting from a 340 nm thick SOI wafer. The device consists of two GC levels in which two different linear apodizations, with opposite chirping signs, are applied. Both gratings have the same length in each scattering element. Unlike most of the configurations reported in the

literature, where a fixed period is used for the apodized grating, the period in our design is recalculated for each radiative element to fulfill the Bragg condition along the whole structure. The combination of this design approach together with the addition of a top grating level with 120 nm thickness enables a simulated directionality of 97.3% and a CE equal to −0.28 dB. The numerically optimized GC was then fabricated starting from a 340 nm thick Si layer with a fabrication process consisting of three etching steps. A peak CE and a 1 dB BW of −0.8 dB and 31.3 nm were experimentally measured. To the best of the authors' knowledge, this result represents the highest CE ever reported in the telecommunications C-band for SOI GCs without the use of any BRs or index-matching material between the fiber and the grating. We believe that, thanks to its versatility, the design procedure discussed in this work can also be applied to other photonic integrated platforms for the realization of high-efficiency coupling solutions.

APPENDIX A: TOLERANCE OF THE GRATING COUPLER PERFORMANCE TO MASK MISALIGNMENT

Since the alignment of the two masks in the two E-beam lithography steps used to define the bottom [see Fig. 4(b)] and top [see Fig. 4(c)] levels of the GC may represent a critical parameter in fabrication, the tolerance of the grating performance to its deviation was numerically simulated. 2D-FDTD simulations were carried out considering the final dual-level GC design. The fiber offset z_f was optimized for each value of the mask misalignment, which was defined as the $\hat{z}$ offset in the position of the mask used to define the top-level dimensions in the second lithography step compared to the aligned condition (mask misalignment = 0). Figure 6(a) shows the variation of the peak CE (CE_{peak}) and peak wavelength (λ_{peak}, the wavelength corresponding to the peak CE) as a function of the mask misalignment. To graphically show the effect of mask misalignment on the GC layout, Figs. 6(b)–6(d) report the dimensions of the first top tooth [additional tooth in Fig. 1(a)] and first bottom trench for three example cases: when the masks are aligned, at a −30 nm mask misalignment, and at a +30 nm mask misalignment, respectively. Considering a ±30 nm variation of the mask misalignment, which represents a reasonable maximum value for E-beam lithography systems, a maximum decrease of CE_{peak} of around 0.1 dB and a maximum variation of λ_{peak} of around 10 nm were numerically simulated. As can be noticed, a positive value of the mask misalignment results in a larger wavelength shift of λ_{peak} compared to a negative one. This can be explained by considering that for a negative value of the mask misalignment, the top teeth are simply shifted to the $-\hat{z}$ direction [see Fig. 6(c)], without affecting the bottom trenches. However, for a positive value of the mask misalignment, the bottom trench widths decrease [see Fig. 6(d)], which results in a greater effective refractive index n_{eff} of the GC and, hence, in a further shift of λ_{peak} toward longer wavelengths. Finally, it should be noted that positive values of the mask misalignment may result in relatively small features for the top teeth and bottom trenches, in particular for the first few periods of the GC, which may not be properly resolved in the lithography and etching steps. Therefore, in order to achieve an even more robust design suitable for large-volume fabrication processes, it may be beneficial to perform a dual-level GC design with relatively larger features for the first few periods or with the top level slightly shifted toward the $-\hat{z}$ direction compared to the bottom level, at the expense of a slight decrease of the simulated peak CE.

Funding. Engineering and Physical Sciences Research Council (EP/T007303/1); Agencia Estatal de Investigación and NextGenerationEU/PRTR (FJC2020-042823-I).

Acknowledgment. The use of the IRIDIS High Performance Computing Facility at the University of Southampton is acknowledged. Joaquin Faneca acknowledges the support of the Agencia Estatal de Investigación and NextGenerationEU/PRTR.

Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper are available in Ref. [49].

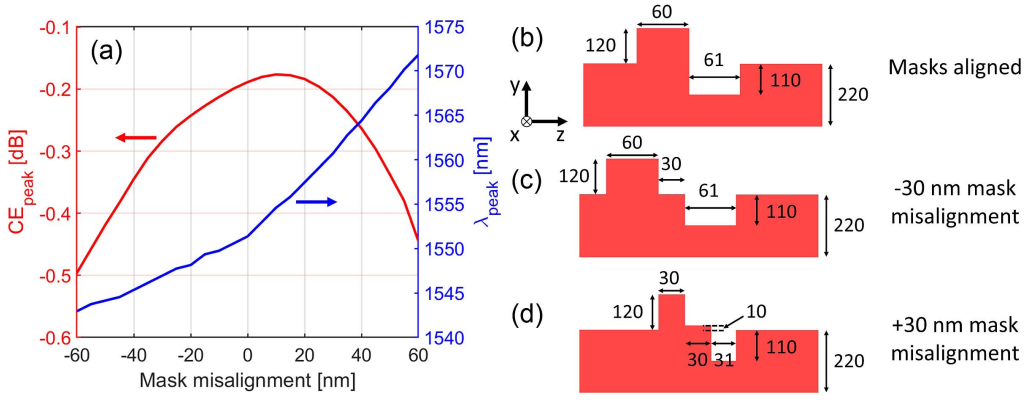

Fig. 6. (a) Peak CE (CE_{peak}, left y axis) and peak wavelength (λ_{peak}, right y axis) as a function of the mask misalignment; variation of the dimensions of the first top tooth and first bottom trench in the cases of (b) aligned masks, (c) −30 nm mask misalignment, and (d) +30 nm mask misalignment.

REFERENCES

1. B. Jalali and S. Fathpour, "Silicon photonics," J. Lightwave Technol. **24**, 4600–4615 (2006).
2. D. Thomson, A. Zilkie, J. E. Bowers, T. Komljenovic, G. T. Reed, L. Vivien, D. Marris-Morini, E. Cassan, L. Virot, J.-M. Fédéli, J.-M. Hartmann, J. H. Schmid, D.-X. Xu, F. Boeuf, P. O'Brien, G. Z. Mashanovich, and M. Nedeljkovic, "Roadmap on silicon photonics," J. Opt. **18**, 073003 (2016).
3. R. Marchetti, V. Vitali, C. Lacava, I. Cristiani, B. Charbonnier, V. Muffato, M. Fournier, and P. Minzioni, "Group-velocity dispersion in SOI-based channel waveguides with reduced-height," Opt. Express **25**, 9761–9767 (2017).
4. R. Marchetti, V. Vitali, C. Lacava, I. Cristiani, G. Giuliani, V. Muffato, M. Fournier, S. Abrate, R. Gaudino, E. Temporiti, L. Carroll, and P. Minzioni, "Low-loss micro-resonator filters fabricated in silicon by CMOS-compatible lithographic techniques: design and characterization," Appl. Sci. **7**, 174 (2017).
5. I. Sackey, A. Gajda, A. Peczek, E. Liebig, L. Zimmermann, K. Petermann, and C. Schubert, "1.024 Tb/s wavelength conversion in a silicon waveguide with reverse-biased p-i-n junction," Opt. Express **25**, 21229–21240 (2017).
6. Y. Long, A. Wang, L. Zhou, and J. Wang, "All-optical wavelength conversion and signal regeneration of PAM-4 signal using a silicon waveguide," Opt. Express **24**, 7158–7167 (2016).
7. B. Troia, A. Z. Khokhar, M. Nedeljkovic, S. A. Reynolds, Y. Hu, G. Z. Mashanovich, and V. M. Passaro, "Design procedure and fabrication of reproducible silicon Vernier devices for high-performance refractive index sensing," Sensors **15**, 13548–13567 (2015).
8. A. K. Goyal, H. S. Dutta, and S. Pal, "Recent advances and progress in photonic crystal-based gas sensors," J. Phys. D **50**, 203001 (2017).
9. A. Bag, M. Neugebauer, U. Mick, S. Christiansen, S. A. Schulz, and P. Banzer, "Towards fully integrated photonic displacement sensors," Nat. Commun. **11**, 2915 (2020).
10. N. C. Harris, D. Bunandar, M. Pant, G. R. Steinbrecher, J. Mower, M. Prabhu, T. Baehr-Jones, M. Hochberg, and D. Englund, "Large-scale quantum photonic circuits in silicon," Nanophotonics **5**, 456–468 (2016).
11. S. Cammarata, A. Fontana, A. E. Kaplan, S. Cornia, T. H. Dao, C. Lacava, V. Demontis, S. Iadanza, V. Vitali, F. De Matteis, E. Pedreschi, G. Magazzù, A. Toncelli, F. Spinella, S. Saponara, R. Gunnella, F. Rossella, A. Salamon, and V. Bellani, "Polarization control in integrated graphene-silicon quantum photonics waveguides," Materials **15**, 8739 (2022).
12. R. Marchetti, C. Lacava, L. Carroll, K. Gradkowski, and P. Minzioni, "Coupling strategies for silicon photonics integrated chips," Photonics Res. **7**, 201–239 (2019).
13. M. Papes, P. Cheben, D. Benedikovic, J. H. Schmid, J. Pond, R. Halir, A. Ortega-Moñux, G. Wangüemert-Pérez, N. Y. Winnie, D.-X. Xu, S. Janz, M. Dado, and V. Vašinek, "Fiber-chip edge coupler with large mode size for silicon photonic wire waveguides," Opt. Express **24**, 5026–5038 (2016).
14. P. Cheben, J. H. Schmid, S. Wang, D.-X. Xu, M. Vachon, S. Janz, J. Lapointe, Y. Painchaud, and M.-J. Picard, "Broadband polarization independent nanophotonic coupler for silicon waveguides with ultra-high efficiency," Opt. Express **23**, 22553–22563 (2015).
15. D. Taillaert, P. Bienstman, and R. Baets, "Compact efficient broadband grating coupler for silicon-on-insulator waveguides," Opt. Lett. **29**, 2749–2751 (2004).
16. A. Bozzola, L. Carroll, D. Gerace, I. Cristiani, and L. C. Andreani, "Optimising apodized grating couplers in a pure SOI platform to -0.5 dB coupling efficiency," Opt. Express **23**, 16289–16304 (2015).
17. G. Roelkens, D. Van Thourhout, and R. Baets, "High efficiency silicon-on-insulator grating coupler based on a poly-silicon overlay," Opt. Express **14**, 11622–11630 (2006).
18. Y. Ding, H. Ou, and C. Peucheret, "Ultrahigh-efficiency apodized grating coupler using fully etched photonic crystals," Opt. Lett. **38**, 2732–2734 (2013).
19. D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform," Opt. Express **18**, 18278–18283 (2010).
20. Y. Tang, Z. Wang, L. Wosinski, U. Westergren, and S. He, "Highly efficient nonuniform grating coupler for silicon-on-insulator nanophotonic circuits," Opt. Lett. **35**, 1290–1292 (2010).
21. L. He, Y. Liu, C. Galland, A. E.-J. Lim, G.-Q. Lo, T. Baehr-Jones, and M. Hochberg, "A high-efficiency nonuniform grating coupler realized with 248-nm optical lithography," IEEE Photonics Technol. Lett. **25**, 1358–1361 (2013).
22. M. H. Lee, J. Y. Jo, D. W. Kim, Y. Kim, and K. H. Kim, "Comparative study of uniform and nonuniform grating couplers for optimized fiber coupling to silicon waveguides," J. Opt. Soc. Korea **20**, 291–299 (2016).
23. F. Van Laere, G. Roelkens, M. Ayre, J. Schrauwen, D. Taillaert, D. Van Thourhout, T. F. Krauss, and R. Baets, "Compact and highly efficient grating couplers between optical fiber and nanophotonic waveguides," J. Lightwave Technol. **25**, 151–156 (2007).
24. N. Hoppe, W. S. Zaoui, L. Rathgeber, Y. Wang, R. H. Klenk, W. Vogel, M. Kaschel, S. L. Portalupi, J. Burghartz, and M. Berroth, "Ultra-efficient silicon-on-insulator grating couplers with backside metal mirrors," IEEE J. Sel. Top. Quantum Electron. **26**, 8200206 (2019).
25. S. K. Selvaraja, D. Vermeulen, M. Schaekers, E. Sleeckx, W. Bogaerts, G. Roelkens, P. Dumon, D. Van Thourhout, and R. Baets, "Highly efficient grating coupler between optical fiber and silicon photonic circuit," in *Conference on Lasers and Electro-Optics and 2009 Conference on Quantum electronics and Laser Science Conference* (IEEE, 2009), pp. 1–2.
26. W. S. Zaoui, A. Kunze, W. Vogel, M. Berroth, J. Butschke, F. Letzkus, and J. Burghartz, "Bridging the gap between optical fibers and silicon photonic integrated circuits," Opt. Express **22**, 1277–1286 (2014).
27. R. Marchetti, C. Lacava, A. Khokhar, X. Chen, I. Cristiani, D. J. Richardson, G. T. Reed, P. Petropoulos, and P. Minzioni, "High-efficiency grating-couplers: demonstration of a new design strategy," Sci. Rep. **7**, 16670 (2017).
28. Y. Ding, C. Peucheret, H. Ou, and K. Yvind, "Fully etched apodized grating coupler on the SOI platform with -0.58 dB coupling efficiency," Opt. Lett. **39**, 5348–5350 (2014).
29. D. Taillaert, F. Van Laere, M. Ayre, W. Bogaerts, D. Van Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," Jpn. J. Appl. Phys. **45**, 6071 (2006).
30. G. Roelkens, D. Vermeulen, D. Van Thourhout, R. Baets, S. Brision, P. Lyan, P. Gautier, and J.-M. Fedeli, "High efficiency diffractive grating couplers for interfacing a single mode optical fiber with a nanophotonic silicon-on-insulator waveguide circuit," Appl. Phys. Lett. **92**, 131101 (2008).
31. S. Yang, Y. Zhang, T. Baehr-Jones, and M. Hochberg, "High efficiency germanium-assisted grating coupler," Opt. Express **22**, 30607–30612 (2014).
32. D. Benedikovic, C. Alonso-Ramos, S. Guerber, X. Le Roux, P. Cheben, C. Dupré, B. Szelag, D. Fowler, É. Cassan, D. Marris-Morini, C. Baudot, F. Boeuf, and L. Vivien, "Sub-decibel silicon grating couplers based on l-shaped waveguides and engineered subwavelength metamaterials," Opt. Express **27**, 26239–26250 (2019).
33. X. Luo, G. Mi, Y. Li, and T. Chu, "High-efficiency grating coupler based on fast directional optimization and robust layout strategy in 130 nm CMOS process," Opt. Lett. **47**, 1622–1625 (2022).
34. D. Benedikovic, C. Alonso-Ramos, D. Pérez-Galacho, S. Guerber, V. Vakarin, G. Marcaud, X. Le Roux, E. Cassan, D. Marris-Morini, P. Cheben, F. Boeuf, C. Baudot, and L. Vivien, "L-shaped fiber-chip grating couplers with high directionality and low reflectivity fabricated with deep-UV lithography," Opt. Lett. **42**, 3439–3442 (2017).
35. C. Alonso-Ramos, P. Cheben, A. Ortega-Moñux, J. Schmid, D.-X. Xu, and I. Molina-Fernández, "Fiber-chip grating coupler based on interleaved trenches with directionality exceeding 95%," Opt. Lett. **39**, 5351–5354 (2014).
36. D. Benedikovic, C. Alonso-Ramos, P. Cheben, J. H. Schmid, S. Wang, D.-X. Xu, J. Lapointe, S. Janz, R. Halir, A. Ortega-Moñux, J. G. Wangüemert-Pérez, Í. Molina-Fernández, J.-M. Fédéli, L. Vivien, and M. Dado, "High-directionality fiber-chip grating coupler with interleaved trenches and subwavelength index-matching structure," Opt. Lett. **40**, 4190–4193 (2015).

37. X. Chen, C. Li, C. K. Fung, S. M. Lo, and H. K. Tsang, "Apodized waveguide grating couplers for efficient coupling to optical fibers," IEEE Photonics Technol. Lett. **22**, 1156–1158 (2010).
38. D. Benedikovic, P. Cheben, J. H. Schmid, D.-X. Xu, B. Lamontagne, S. Wang, J. Lapointe, R. Halir, A. Ortega-Moñux, S. Janz, and M. Dado, "Subwavelength index engineered surface grating coupler with sub-decibel efficiency for 220-nm silicon-on-insulator waveguides," Opt. Express **23**, 22628–22635 (2015).
39. C. Littlejohns, D. Rowe, H. Du, K. Li, W. Zhang, W. Cao, T. Domínguez Bucio, X. Yan, M. Banakar, D. Tran, S. Liu, F. Meng, B. Chen, Y. Qi, X. Chen, M. Nedeljkovic, L. Mastronardi, R. Maharjan, S. Bohora, and G. Reed, "Cornerstone's silicon photonics rapid prototyping platforms: current status and future outlook," Appl. Sci. **10**, 8201 (2020).
40. A. Sánchez-Postigo, R. Halir, J. G. Wangüemert-Pérez, A. Ortega-Moñux, S. Wang, M. Vachon, J. H. Schmid, D.-X. Xu, P. Cheben, and Í. Molina-Fernández, "Breaking the coupling efficiency–bandwidth trade-off in surface grating couplers using zero-order radiation," Laser Photonics Rev. **15**, 2000542 (2021).
41. R. Guo, S. Zhang, H. Gao, G. S. Murugan, T. Liu, and Z. Cheng, "Blazed subwavelength grating coupler," Photonics Res. **11**, 189–195 (2023).
42. X. Zhou and H. K. Tsang, "Optimized shift-pattern overlay for high coupling efficiency waveguide grating couplers," Opt. Lett. **47**, 3968–3971 (2022).
43. J. Notaros, F. Pavanello, M. T. Wade, C. M. Gentry, A. Atabaki, L. Alloatti, R. J. Ram, and M. A. Popović, "Ultra-efficient CMOS fiber-to-chip grating couplers," in *Optical Fiber Communications Conference and Exhibition (OFC)* (IEEE, 2016), pp. 1–3.
44. B. Zhang, D. Gluhovic, A. Khilo, and M. A. Popović, "Sub-decibel efficiency, bi-layer, O-band fiber-to-chip grating coupler demonstrated in a 45 nm CMOS foundry platform," in *CLEO: Science and Innovations* (Optica Publishing Group, 2022), paper STu5G-4.
45. V. Vitali, C. Lacava, T. Domnguez Bucio, F. Y. Gardes, and P. Petropoulos, "Highly efficient dual-level grating couplers for silicon nitride photonics," Sci. Rep. **12**, 15436 (2022).
46. W. D. Sacher, Y. Huang, L. Ding, B. J. Taylor, H. Jayatilleka, G.-Q. Lo, and J. K. Poon, "Wide bandwidth and high coupling efficiency Si_3N_4-on-SOI dual-level grating coupler," Opt. Express **22**, 10938–10947 (2014).
47. J. C. Mak, Q. Wilmart, S. Olivier, S. Menezo, and J. K. Poon, "Silicon nitride-on-silicon bi-layer grating couplers designed by a global optimization method," Opt. Express **26**, 13656–13665 (2018).
48. T. Ang, G. Reed, A. Vonsovici, A. Evans, P. Routley, and M. Josey, "Highly efficient unibond silicon-on-insulator blazed grating couplers," Appl. Phys. Lett. **77**, 4214–4216 (2000).
49. V. Vitali, T. Domnguez Bucio, C. Lacava, R. Marchetti, L. Mastronardi, T. Rutirawut, G. Churchill, J. Faneca, J. C. Gates, F. Gardes, and P. Petropoulos, "High efficiency reflector-less dual-level silicon photonic grating coupler," 2023. https://doi.org/10.5258/SOTON/D2550 (Last accessed 27 April 2023).