

PHOTONICS Research

Foundry manufacturing of tight-confinement, dispersion-engineered, ultralow-loss silicon nitride photonic integrated circuits

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The foundry development of integrated photonics has revolutionized today's optical interconnect and datacenters. Over the last decade, we have witnessed the rising of silicon nitride (Si_3N_4) integrated photonics, which is currently transferring from laboratory research to foundry manufacturing. The development and transition are triggered by the ultimate need for low optical loss offered by Si_3N_4 , which is beyond the reach of silicon and III-V semiconductors. Combined with modest Kerr nonlinearity, tight optical confinement, and dispersion engineering, Si_3N_4 has today become the leading platform for linear and Kerr nonlinear photonics, and it has enabled chip-scale lasers featuring ultralow noise on par with table-top fiber lasers. However, so far all the reported fabrication processes of tight-confinement, dispersion-engineered Si_3N_4 photonic integrated circuits (PICs) with optical loss down to few dB/m have only been developed on 4-inch (100 mm diameter) or smaller wafers. Yet, to transfer these processes to established CMOS foundries that typically operate 6-inch or even larger wafers, challenges remain. In this work, we demonstrate the first foundry-standard fabrication process of Si_3N_4 PICs with only 2.6 dB/m loss, thickness above 800 nm, and near 100% fabrication yield on 6-inch (150 mm diameter) wafers. Such thick and ultralow-loss Si_3N_4 PIC enables low-threshold generation of soliton frequency combs. Merging with advanced heterogeneous integration, active ultralow-loss Si_3N_4 integrated photonics could pave an avenue to addressing future demands in our increasingly information-driven society. © 2023 Chinese Laser Press

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1. INTRODUCTION

Integrated photonics [1] enables the synthesis, processing, and detection of optical signals using the photonic integrated circuit (PIC). The successful translation from laboratory research to foundry development over the past decades has established integrated photonics as a standard technology [2] deployed in high-data-rate telecommunication and datacenters [3]. Foundry-level manufacturing of photonic chips allows fast prototyping or mass production with high yield, high throughput, low cost, and guaranteed performance.

Silicon (Si) and indium phosphide (InP) are two mainstream platforms of integrated photonics [4]. The development of heterogeneous integration [5,6] has married these two

platforms and created the first electrically pumped InP/Si lasers [7,8] that have today been used for optical interconnect. Despite that, Si and InP still have many limitations, particularly the high linear and nonlinear losses (e.g., two-photon absorption) that compromise their performance.

To address this challenge, silicon nitride (Si_3N_4) has emerged as a leading platform for low-loss integrated photonics [9–11]. The 5 eV bandgap of Si_3N_4 makes it transparent from ultraviolet to mid-infrared, and immune to two-photon absorption in the telecommunication band. Meanwhile, Si_3N_4 has a dominant Kerr nonlinearity but negligible Raman [12] and Brillouin nonlinearities [13]. In addition, with advanced CMOS fabrication techniques, linear optical loss down to

1 dB/m or even lower has been only achieved in Si_3N_4 [14–19] among all integrated platforms. All these advantages have triggered the rapid development of Si_3N_4 Kerr nonlinear photonics [9,10] and have enabled key advances such as optical frequency comb generation [20–22], supercontinuum generation [23–25], and quantum light sources [26–28]. In addition to ultralow loss, tight optical confinement with SiO_2 cladding is simultaneously required. Since the refractive index of Si_3N_4 ($n \approx 1.99$) is modestly higher than that of SiO_2 ($n \approx 1.45$), Si_3N_4 waveguides require sufficient thickness to achieve tight optical confinement for small mode volume and for bending radii down to 20 μm . In addition, while Si_3N_4 material has intrinsic normal group velocity dispersion (GVD) at telecommunication bands, Si_3N_4 waveguides with thickness above 600 nm can obtain net anomalous GVD that is required for phase matching in Kerr parametric processes [29,30].

While CMOS foundries have already developed standard Si_3N_4 processes [31] to fabricate PIC with typical thickness of 300 nm and loss on the order of 10 dB/m, there has not been a process to simultaneously achieve ultralow loss (e.g., below 3 dB/m) and large thickness (above 600 nm) without crack formation. So far, thin Si_3N_4 PIC with a width above 5 μm and thickness below 100 nm [17–19] can achieve optical loss below 0.1 dB/m. While this process has recently become an 8-inch (200 mm diameter) foundry process [32], the thin Si_3N_4 exhibits weak optical confinement and, thus, suffers from exaggerated bending loss with a small footprint. The optical mode also exhibits strong normal GVD due to the waveguide geometry. While coupled waveguide structures can be used to alter local GVD [33,34], they cannot offer anomalous GVD over a wide spectral range. In parallel, a thick Si_3N_4 PIC of ultralow loss and broadband anomalous GVD has been realized via the subtractive process [35–37] and the photonic Damascene process [14,38]. However, all these reported processes have been

developed only in laboratories and have issues with transferring to foundry manufacturing. While high-yield, wafer-scale fabrication of Si_3N_4 PIC has achieved 1 dB/m loss and anomalous GVD in Ref. [14], the photonic Damascene process has intrinsic limitations. For example, the use of chemical-mechanical planarization (CMP) to remove excess Si_3N_4 can cause a serious dishing effect in large-area structures (see Appendix C) and, thus, cannot be used to fabricate elements such as arrayed waveguide gratings (AWGs) and multimode interferometers (MMIs). Meanwhile, the aspect-ratio-dependent etch effect prevents the formation of narrow but deep channels [39]. In comparison, with the subtractive process [35–37], a thick Si_3N_4 PIC of ultralow loss and anomalous GVD has been only achieved with electron-beam lithography (EBL) on 3- or 4-inch wafers, which are not foundry-standard. Meanwhile, an 8-inch foundry process has been developed in Ref. [40], but this process has not yet achieved optical loss below 3 dB/m.

In this work, we overcome the above challenges and demonstrate a foundry-standard fabrication process of tight-confinement, dispersion-engineered, ultralow-loss Si_3N_4 PIC. The process is based on 6-inch (150 mm diameter) wafers and combines deep-ultraviolet (DUV) stepper lithography [14] and state-of-the-art subtractive process [37], i.e., a DUV subtractive process. We have achieved a linear optical loss of 2.6 dB/m in 810-nm-thick Si_3N_4 PIC. Finally, we generate single-soliton microcombs of 100.17 GHz and 19.975 GHz mode spacings using these devices.

2. FABRICATION

Figure 1(a) presents a photograph that shows dozens of Si_3N_4 chips on a 6-inch wafer, which contains microresonators of different free spectral ranges (FSRs) and meter-long spirals. Figure 1(b) presents an optical micrograph that shows a curved

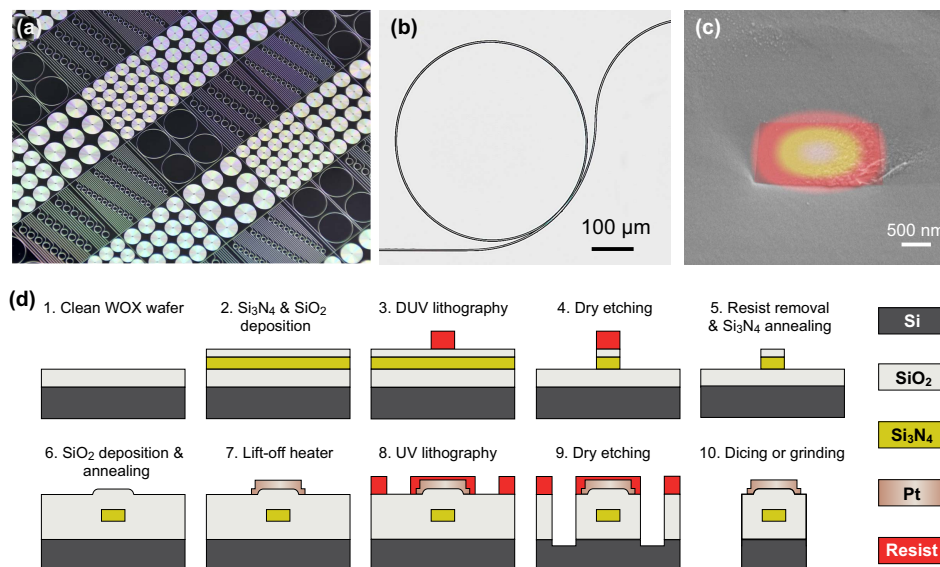


Fig. 1. Process flow and sample images of the 6-inch Si_3N_4 foundry fabrication process. (a) Photograph of dozens of Si_3N_4 chips on a 6-inch wafer, which contains microresonators of different FSR and meter-long spirals. (b) Optical micrograph showing a curved bus waveguide slowly approaching a 100-GHz-FSR microring resonator. (c) SEM image showing the Si_3N_4 waveguide core with SiO_2 cladding. The TE_{00} mode is plotted, showing tight confinement in the Si_3N_4 waveguide core. (d) DUV subtractive process flow. WOX, wet oxide (SiO_2).

bus waveguide slowly approaching a 100-GHz-FSR microring resonator for light coupling. This coupler design can increase coupling strength and ideality, which will be described later. Figure 1(c) presents a scanning electron microscopy (SEM) image that shows the actual Si_3N_4 waveguide cross section with 85° sidewall angle and overlaid fundamental transverse-electric (TE_{00}) mode. The optical mode is tightly confined in the Si_3N_4 waveguide core with SiO_2 cladding, enabling dispersion engineering and small bending radii.

The Si_3N_4 PIC is fabricated using the DUV subtractive process. Figure 1(d) shows the subtractive process flow widely used to fabricate PIC based on essentially any material, particularly Si_3N_4 [35–37,40–44]. First, a Si_3N_4 film is deposited on a clean thermal wet SiO_2 substrate via low-pressure chemical vapor deposition (LPCVD). It is well known that LPCVD Si_3N_4 films are prone to crack due to their intrinsic tensile stress (typically 1.1–1.4 GPa). The film stress can be relaxed via thermal cycling during Si_3N_4 deposition in multiple layers [40,41], yielding zero cracks during our fabrication. After SiO_2 deposition as an etch hardmask, DUV stepper photolithography is used to expose the waveguide pattern. Via dry etching, the pattern is subsequently transferred from the photoresist mask to the SiO_2 hardmask and then into the Si_3N_4 layer to form waveguides. For superior etch quality and smooth waveguide sidewall, the etchant we use is CHF_3 with added O_2 to remove fluoride-carbon polymers as etch byproducts.

The etched substrate is thermally annealed in nitrogen atmosphere at 1200°C to eliminate nitrogen-hydrogen bonds in Si_3N_4 , which cause absorption loss. Top SiO_2 cladding is then deposited on the wafer, which also requires high-temperature annealing to remove silicon-hydrogen bonds that also cause absorption loss. In specific cases where deuterated plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 [44,45] and SiO_2 [46] are used, thermal annealing may not be required as these films are intrinsically hydrogen-free.

Platinum heaters [22,47] are deposited on the substrate via an evaporator and patterned via a lift-off process. Due to the thick top SiO_2 cladding and tight optical confinement of the Si_3N_4 core, the presence of metallic heaters does not impact the optical loss of Si_3N_4 waveguides beneath. Afterward, UV photolithography and deep dry etching of SiO_2 and Si are used to define chip size and create smooth chip facets. Finally, the wafer is separated into chips using dicing or backside grinding.

3. CHARACTERIZATION

A. Microresonator Quality Factors and Loss Rates

We characterize the optical loss of Si_3N_4 PIC by measuring the resonance linewidth of Si_3N_4 microresonators. Light is coupled into and out of Si_3N_4 chips via lensed fibers and inverse tapers [39]. The fiber-chip edge coupling efficiency is about 60%. We use frequency-comb-assisted diode laser spectroscopy [48] to measure resonance frequency $\omega/2\pi$ and linewidth $\kappa/2\pi$, ranging from 1480 to 1640 nm wavelength. The resonance's quality factor is calculated as $Q = \omega/\kappa$. Here we study both the TE_{00} and TM_{00} (fundamental transverse-magnetic) modes of the 100-GHz-FSR microresonators of 810 nm thickness and 2.40 μm waveguide width. For each resonance fit [49], the

intrinsic loss $\kappa_0/2\pi$, external coupling strength $\kappa_{\text{ex}}/2\pi$, and total (loaded) linewidth $\kappa/2\pi = (\kappa_0 + \kappa_{\text{ex}})/2\pi$ are extracted.

Figure 2(a) shows a typical TE_{00} resonance with a Lorentzian fit. The resonance is under-coupled ($\kappa_0 > \kappa_{\text{ex}}$), with fitted $\kappa_0/2\pi = 13.8$ MHz. Figure 2(b) shows a histogram of $\kappa_0/2\pi$ for 11,741 fitted TE_{00} resonances from sixty 100-GHz-FSR microresonators. The most probable value is $\kappa_0/2\pi = 14$ MHz, corresponding to a statistical intrinsic quality factor of $Q_0 = 1.4 \times 10^7$. The microresonator Q_0 and linear optical loss α (dB/m physical length) are linked via

$$\alpha = 27.27 \frac{n_g}{\lambda Q_0}. \quad (1)$$

At telecommunication band $\lambda = 1550$ nm and with a group index $n_g = 2.09$ for the given waveguide geometry, $Q_0 = 1.4 \times 10^7$ corresponds to $\alpha = 2.6$ dB/m. In comparison, $\kappa_0/2\pi = 17$ MHz is found for the TM_{00} mode, corresponding to $Q_0 = 1.1 \times 10^7$ (see Appendix A). The wavelength-dependent loss of each TE_{00} resonance is studied in Appendix B, showing no prominent hydrogen-related absorption around 1520–1540 nm.

Next, we investigate wafer-scale fabrication yield. The right of Fig. 2(d) shows our design layout containing 16 chips on the DUV stepper reticle. Each chip has a 5 mm \times 5 mm size on the wafer and contains many microresonators. The DUV stepper exposes the reticle uniformly over the 6-inch wafer in discrete fields. The 100-GHz-FSR chips characterized above are labeled as the C11 chips. The most probable $\kappa_0/2\pi$ values for all C11 chips, as well as their GVD parameters $D_2/2\pi$ (described later), are plotted in each field, as shown in the left of Fig. 2(d). In all measured 20 fields, $\kappa_0/2\pi \leq 16$ MHz is found, demonstrating that our foundry process to manufacture ultralow-loss Si_3N_4 PIC is uniform and near 100% yield.

We also characterize $\kappa_0/2\pi$ of 100-GHz-FSR microresonators of 2.20, 2.00, and 1.80 μm waveguide width. Again, we create a $\kappa_0/2\pi$ histogram for each case and look for the most probable values. We plot and compare the most probable $\kappa_0/2\pi$ values for the three width values and observe a decreasing $\kappa_0/2\pi$ with increasing waveguide width, as shown in Fig. 2(c). This trend indicates that our optical loss is still dominated by the waveguide's $\text{Si}_3\text{N}_4/\text{SiO}_2$ interface roughness and can be further reduced by optimizing the dry etching process or using CMP to reduce top surface roughness [36].

B. Microresonator Dispersion

For most applications using Kerr nonlinearity of Si_3N_4 , anomalous GVD is required [29,30]. In addition, for the generation of dissipative Kerr solitons [20,50,51], avoided mode crossings (AMX) induced by spatial mode coupling [52] should be suppressed, as they prohibit soliton formation [53,54] or distort soliton spectra [55,56]. Therefore, next we quantitatively characterize the dispersion profile and investigate AMXs of the high- Q , 100-GHz-FSR microresonators. The microresonator's integrated dispersion is defined as

$$D_{\text{int}}(\mu) = \omega_\mu - \omega_0 - D_1\mu \\ = D_2\mu^2/2 + D_3\mu^3/6 + D_4\mu^4/24, \quad (2)$$

where $\omega_\mu/2\pi$ is the μ th resonance frequency relative to the reference resonance frequency $\omega_0/2\pi$, $D_1/2\pi$ is microresonator FSR, $D_2/2\pi$ describes GVD, and D_3 and D_4 are

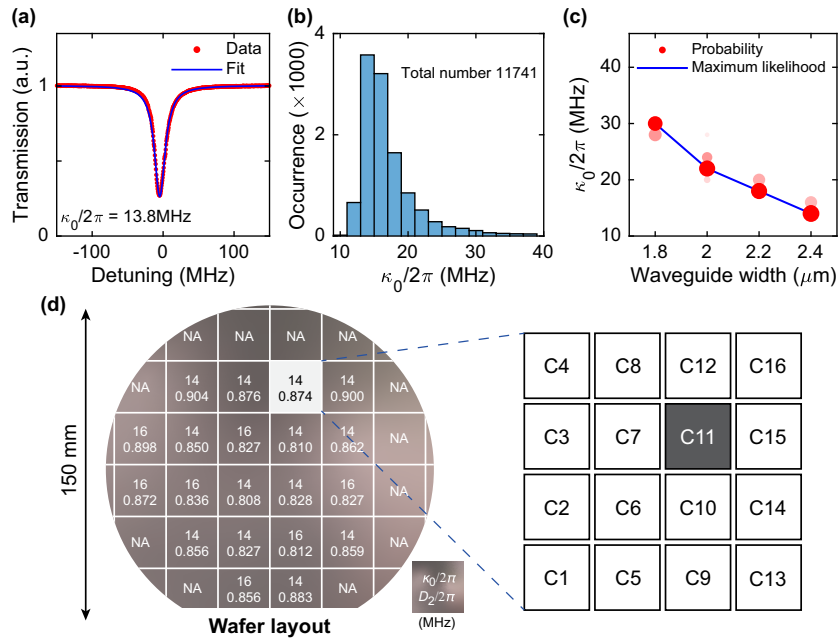


Fig. 2. Statistical loss characterization and yield analysis. (a) Typical TE_{00} resonance profile with a Lorentzian fit, showing $\kappa_0/2\pi = 13.8$ MHz and negligible mode split. (b) Histogram of 11,741 TE_{00} resonances from sixty 100-GHz-FSR microresonators of $2.40 \mu\text{m}$ waveguide width, showing the most probable value of $\kappa_0/2\pi = 14$ MHz and $Q_0 = 1.4 \times 10^7$. (c) Characterization of waveguide-width-dependent loss. Microresonators of 2.40 , 2.20 , 2.00 , and $1.80 \mu\text{m}$ waveguide widths are characterized and compared. A trend of lower κ_0 with a larger width is shown. The size and color tone of the circles indicate the probability of occurrence. (d) Uniformity and yield analysis over the 6-inch wafer scale. Right, the DUV stepper reticle layout contains 16 chips and is uniformly exposed in discrete fields over the 6-inch wafer. Left, the most probable values $\kappa_0/2\pi$ of the C11 chips, as well as the measured GVD parameters $D_2/2\pi$, are marked in each field over the wafer. NA: not applicable, due to visible defects or missing C11 chips near wafer edge.

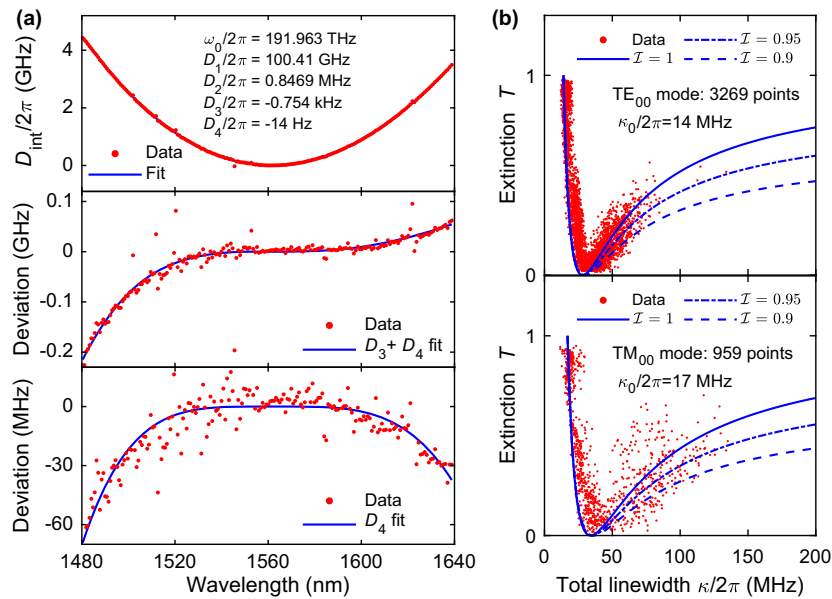


Fig. 3. Characterization of microresonator dispersion and coupling ideality. (a) Measured integrated dispersion of the microresonator that is fitted with $D_{\text{int}}(\mu) = D_2\mu^2/2 + D_3\mu^3/6 + D_4\mu^4/24$ (top), the resonance frequency deviations from $D_3\mu^3/6 + D_4\mu^4/24$ (middle), and the deviations from $D_4\mu^4/24$ (bottom). Avoided mode crossings are revealed in the bottom panel, however weak for the later soliton generation experiment. (b) Characterization of coupling ideality of the TE_{00} (top) and TM_{00} (bottom) modes. For the TE_{00}/TM_{00} modes, in total thirty-four/seventeen 100-GHz-FSR microresonators are characterized, providing 3269/959 data points in each plot. A clear trend from under-coupling to critical coupling and then to strong over-coupling is observed. The calculated curves of $\mathcal{I} = 0.9, 0.95, 1$ with $\kappa_0/2\pi = 14$ or 17 MHz are plotted for comparison, showing near-unity coupling ideality.

higher-order dispersion terms. The top of Figure 3(a) shows a typical D_{int} profile, with each parameter extracted from the fit Eq. (2). The positive sign of D_2 validates anomalous GVD. To reveal AMXs, we remove the D_2 term and fit the data with $D_3\mu^3/6 + D_4\mu^4/24$, as shown in the middle of Fig. 3(a). We further remove the D_2 and D_3 terms, and fit the data with $D_4\mu^4/24$, as shown in the bottom of Fig. 3(a). The observed AMXs are overall weak and only lead to megahertz-level resonance frequency deviation. It also shows that, with these weak AMXs, our spectroscopic method is sufficiently precise to extract the D_4 term.

C. Coupling Ideality

Furthermore, we experimentally characterize the coupling ideality [57] of our high- Q Si_3N_4 microresonators. In the current case, light in the bus waveguide's fundamental TE mode ($\text{TE}_{b,00}$) is coupled into the microresonator's fundamental TE mode ($\text{TE}_{r,00}$) and then coupled out of the microresonator and back into the bus waveguide. In this process, coupling ideality \mathcal{I} is defined as

$$\mathcal{I} = \frac{\kappa_{\text{ex}}}{\kappa_{\text{ex}} + \kappa_p}. \quad (3)$$

Here κ_{ex} is the external coupling rate between the $\text{TE}_{r,00}$ and $\text{TE}_{b,00}$ modes, and κ_p is the parasitic loss rate describing coupling strength to other bus waveguide modes as well as radiation modes into free space. The parasitic loss κ_p appears as another loss channel in addition to κ_0 and κ_{ex} . Thus, \mathcal{I} is a parameter describing how much power is recoupled in the $\text{TE}_{b,00}$ mode that is exactly the initial driving mode of the bus waveguide [57,58]. In the ideal case of single-mode bus waveguide and no radiation into free space, $\mathcal{I} = 1$ is obtained. In the present case, the bus waveguide is multimode, since it has the same waveguide cross section (thickness \times width) as the microresonator waveguide, to obtain phase matching between the $\text{TE}_{b,00}$ and $\text{TE}_{r,00}$ modes for maximum κ_{ex} . Thus, the $\text{TE}_{r,00}$ mode can couple to other bus waveguide modes (e.g., higher-order TE modes or any TM modes) or radiation modes, which ultimately compromises coupling ideality ($\mathcal{I} < 1$).

With a sufficient number of characterized resonances, coupling ideality is evaluated by analyzing the dependence of resonance transmission T and total linewidth $\kappa/2\pi$, as

$$T = \left| 1 - \frac{2}{K^{-1} + \mathcal{I}^{-1}} \right|^2, \quad (4)$$

where $K = \kappa_{\text{ex}}/\kappa_0$ describes the coupling regime ($K < 1$ for under-coupling, $K = 1$ for critical coupling, and $K > 1$ for over-coupling [59]). Previously, coupling ideality of integrated Si_3N_4 microresonators has been characterized [58], however, based on devices of $Q < 4 \times 10^6$. For state-of-the-art Si_3N_4 microresonators of $Q > 10^7$, coupling ideality has not been experimentally studied, and whether high coupling ideality is still maintained needs to be answered.

Here we perform extra measurement on over-coupled devices with smaller gap values down to 300 nm. The microresonators are identical, except that the gap varies from sample to sample to provide a varying κ_{ex} . Figure 3(b) shows the measured coupling ideality for the TE_{00} and TM_{00} modes from dozens of 100-GHz-FSR microresonators. The TE_{00} [top of

Fig. 3(b)] and TM_{00} [bottom of Fig. 3(b)] plots contain 3269 and 959 data points, respectively. The data are sufficient to uncover the global trend even in the presence of κ_0 variation due to fabrication and AMXs. Meanwhile, for comparison, we also plot the κ - T curves with $\mathcal{I} = 0.9, 0.95, 1$, calculated using Eq. (4). As can be seen, our microresonators coupled with curved bus waveguides can already provide near-unity \mathcal{I} and strong over-coupling (e.g., $K > 7$ for the TM_{00}), which are critical for microring-based phase modulation [60,61], wideband tunable delay lines [62], and the extraction of quantum light states generated in high- Q microresonators [27,63–65].

4. SOLITON MICROCOMB GENERATION

A key application area of our Si_3N_4 PIC is Kerr nonlinear photonics, where ultralow optical loss is central as it determines the threshold power P_{th} for Kerr parametric oscillation [29]. For example, for soliton microcomb generation [20,50,51], P_{th} scales with the microresonator Q factor as $P_{\text{th}} \propto Q^{-2}$. Therefore, with this quadratic dependence, a high Q enables significant reduction of P_{th} down to milliwatt level.

The experimental setup to generate single solitons in our Si_3N_4 chips is shown in Fig. 4(a). We note that, due to the high- Q and low thermal effects of our Si_3N_4 microresonators, single solitons can be generated via simple laser-piezo frequency tuning [50,66] or on-chip heaters [22,47]. This is in contrast to many soliton generation experiments that require sophisticated techniques to manage thermal effects [67], such as power kicking [68,69], single-sideband suppressed-carrier frequency shifters [70], dual-laser pump [71,72], pump modulation [73,74], pulse pumping [75], or laser self-cooling [76].

When the continuous-wave (CW) pump laser's frequency scans across a resonance from the blue-detuned side to the red-detuned side, a step feature (i.e., the "soliton step") is observed in the microresonator transmission spectrum [50], signaling soliton formation. Figure 4(b) shows a typical soliton step with sub-millisecond duration, sufficiently long for accessing the single-soliton state via simple laser-piezo frequency tuning [50,66]. To further confirm the soliton nature and measure the soliton detuning value, a system response measurement using an electro-optic modulator (EOM) and a vector network analyzer (VNA) is performed [66]. As shown in Fig. 4(c), the system response features double resonances corresponding to the cavity resonance of the CW pump ("C-resonance"), and the soliton-induced resonance ("S-resonance"). Physically, the "cold" cavity resonance is probed by the intracavity low-power CW as a background to the soliton pulse pattern; thus, the observed C-resonance frequency indicates the effective laser-cavity detuning (where thermal induced resonance shift is eliminated) [66]. The S-resonance is induced by the soliton pattern that has a high peak-power leading to nonlinear frequency shift of the cavity resonance.

As shown in Fig. 4(d), in a 100-GHz-FSR microresonator, a single soliton of 100.17 GHz mode spacing is generated with 19 mW power in the bus waveguide on-chip. The spectrum sech^2 fit shows 3 dB bandwidth of 17.99 nm, corresponding to a Fourier-limited pulse duration of 141.8 fs. Increasing the pump power to 126 mW and the pump laser detuning, the

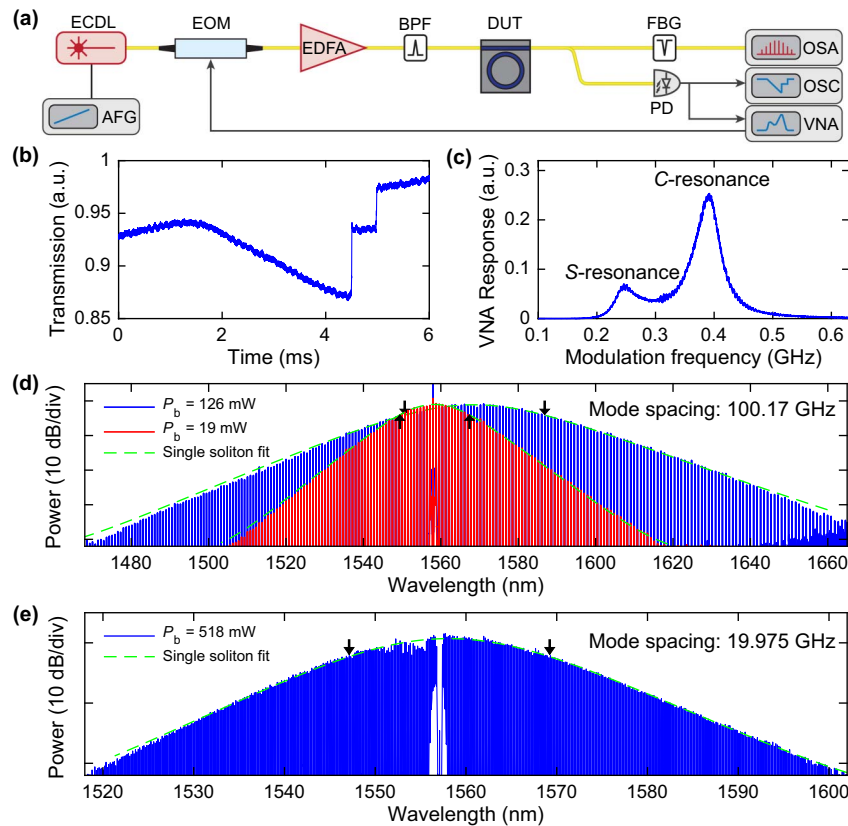


Fig. 4. Single-soliton generation in silicon nitride. (a) Experimental setup. AFG, arbitrary function generator; ECDL, external-cavity diode laser; EDFA, erbium-doped fiber amplifier; BPF, bandpass filter; EOM, electro-optic modulator; DUT, device under test; FBG, fiber Bragg grating; PD, photodiode; OSA, optical spectrum analyser; OSC, oscilloscope; VNA, vector network analyzer. (b) When the laser frequency is scanned from the blue-detuned to the red-detuned side of a resonance, a soliton step of sub-millisecond length appears, enabling direct access to soliton states via simple piezo tuning of laser frequency. (c) Cavity response measurement using the EOM and VNA. The appearance of S -resonance verifies soliton generation. (d) Single-soliton spectra of 100.17 GHz mode spacing, with 19 mW (red) and 126 mW (blue) CW pump power on the chip, and their spectral fit (green). With 19/126 mW power, the arrows mark the 3 dB bandwidth of 17.99/35.68 nm. A prominent Raman self-frequency shift of 10.4 nm is observed with 126 mW power. (e) Single-soliton spectrum of 19.975 GHz mode spacing with 518 mW (blue) CW pump power on the chip and its spectral fit (green). The arrows mark the 3 dB bandwidth of 21.96 nm, containing 137 comb lines. In both (d) and (e), the EDFA's amplified spontaneous emission (ASE) noise is filtered out by the BPF, and the pump laser in the soliton spectra is filtered out by the FBG.

soliton's 3 dB spectrum bandwidth is increased to 35.68 nm (pulse duration of 71.47 fs). We also observe a strong Raman-induced self-frequency shift [77,78] of 10.4 nm. Moreover, we generate a single soliton in a 20-GHz-FSR microresonator from the same wafer. Figure 4(e) shows the single-soliton spectrum of 19.975 GHz mode spacing with 518 mW power in the bus waveguide. The 3 dB bandwidth of 21.96 nm, corresponding to a pulse duration of 115.4 fs, covers 117 comb lines. This coherent soliton microcomb with a microwave K-band repetition rate is advantageous for applications such as high-spectral-efficiency telecommunications [79,80], photonic microwave generation [81–83], and astronomical spectrometer calibration [84,85]. Previously, among all CMOS-compatible high-index materials, single-soliton microcombs of repetition rates below microwave K-band (<20 GHz) have only been realized in Si_3N_4 , using either the 4-inch photonic Damascene process [82], or the 3-inch EBL-written subtractive process [86]. Our work represents the first foundry-based, 6-inch subtractive process with DUV stepper lithography to reach this goal.

5. CONCLUSION AND OUTLOOK

In conclusion, we have reported a 6-inch foundry fabrication process of tight-confinement, dispersion-engineered Si_3N_4 PIC of optical loss down to 2.6 dB/m and near 100% yield. We have demonstrated its application in soliton microcomb generation with low power threshold and dense channel spacings. While currently our process is based on 6-inch wafers due to our dry etcher, essentially our process can be scaled up to an 8-inch (200 mm diameter) process, which can offer even better uniformity and higher throughput. Merging our ultralow-loss Si_3N_4 process with established heterogeneous integration [87,88] can introduce a variety of active functions to the passive Si_3N_4 PIC, such as narrow-linewidth lasers in the UV and visible bands [89,90], broadband EOMs [91,92], fast photodetectors [93,94], and programmable MEMS-controlled networks [95,96]. Together, foundry development of heterogeneous, ultralow-loss Si_3N_4 integrated photonics could revolutionize next-generation applications for frequency metrology [97,98], photonic neural networks [99,100], and quantum information processing [101,102].

APPENDIX A: CHARACTERIZATION OF THE MICRORESONATOR TM_{00}

Figure 5(a) shows a TM_{00} resonance with a Lorentzian fit. The resonance is critically coupled ($\kappa_0 \approx \kappa_{ex}$), with fitted $\kappa_0/2\pi = 15.6$ MHz. Figure 5(b) shows a histogram of $\kappa_0/2\pi$ for 7944 fitted TM_{00} resonances from forty 100-GHz-FSR microresonators. The most probable value is $\kappa_0/2\pi = 17$ MHz, corresponding to $Q_0 = 1.1 \times 10^7$. Figure 5(c) shows the most probable $\kappa_0/2\pi$ values for all C11 chips plotted in each field of the 6-inch wafer, as well as their GVD parameters $D_2/2\pi$. In all measured 20 fields, $\kappa_0/2\pi \leq 19$ MHz is found.

APPENDIX B: LOSS VERSUS WAVELENGTH

We use frequency-comb-assisted diode laser spectroscopy [48] to measure resonance frequency $\omega/2\pi$ and linewidth $\kappa/2\pi$, ranging from 1480 to 1640 nm wavelength. Figure 6 shows the measured and fitted intrinsic loss $\kappa_0/2\pi$, the external coupling strength $\kappa_{ex}/2\pi$, and the total (loaded) linewidth $\kappa/2\pi = (\kappa_0 + \kappa_{ex})/2\pi$ of each resonance of a typical 100-GHz-FSR microresonator. Since the bus waveguide and the microresonator are coupled via evanescent field, $\kappa_{ex}/2\pi$ is wavelength-dependent with a given geometry. Therefore, the alignment of $\kappa_{ex}/2\pi$ values on a line indicates correct resonance fit with reasonable precision. Local $\kappa_0/2\pi$ increase is observed at multiple wavelengths; however, such narrowband features are likely caused by AMXs. In addition, no prominent

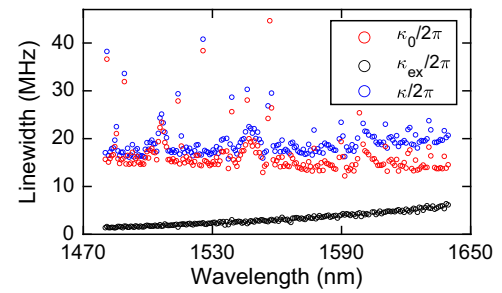


Fig. 6. Broadband measurement of resonance linewidth. Measured and fitted $\kappa_0/2\pi$, $\kappa_{ex}/2\pi$, and $\kappa/2\pi = (\kappa_0 + \kappa_{ex})/2\pi$ of each resonance from 1480 to 1640 nm. The alignment of $\kappa_{ex}/2\pi$ values on a line indicates correct resonance fit with reasonable precision. Local $\kappa_0/2\pi$ increase at multiple wavelengths is likely caused by AMXs. No prominent hydrogen-related absorption around 1520–1540 nm is observed.

hydrogen-related absorption around 1520–1540 nm is observed, indicating low photo-thermal absorption.

APPENDIX C: CMP DISHING EFFECT

Our reported process is based on the subtractive process that is a top-down process where Si_3N_4 waveguides are formed by dry etching. There is another process widely used for the fabrication of ultralow-loss Si_3N_4 PIC, i.e., the photonic Damascene process [14,38]. This process is an “additive” process. As illustrated

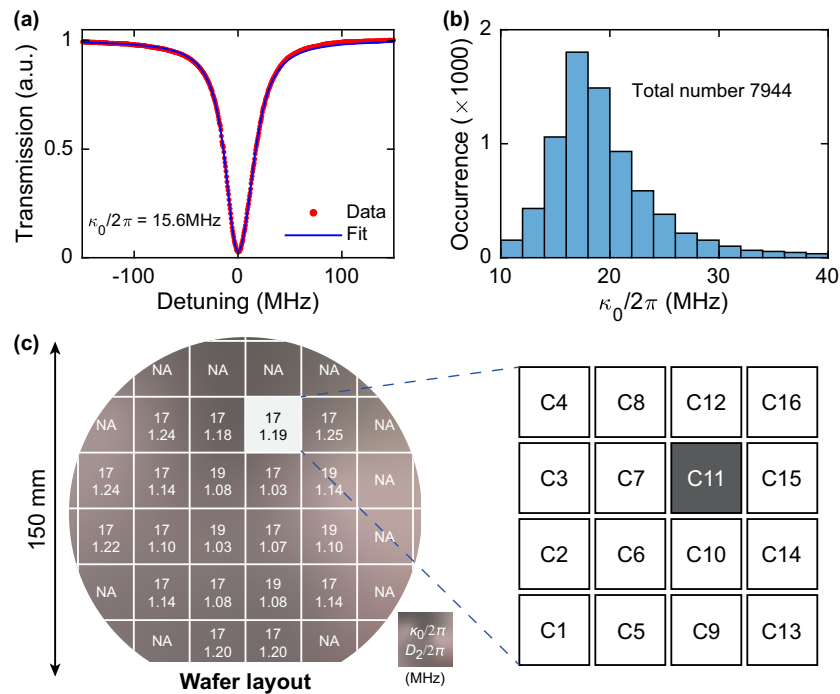


Fig. 5. Characterization of the microresonator TM_{00} mode. (a) Typical TM_{00} resonance profile with a Lorentzian fit, showing $\kappa_0/2\pi = 15.6$ MHz. (b) Histogram of 7944 TM_{00} resonances from forty 100-GHz-FSR microresonators of $2.40 \mu\text{m}$ waveguide width, showing the most probable value of $\kappa_0/2\pi = 17$ MHz and $Q_0 = 1.1 \times 10^7$. (c) Uniformity and yield analysis over the 6-inch wafer scale. Right, the DUV stepper reticle layout contains 16 chips and is uniformly exposed in discrete fields over the 6-inch wafer. Left, the most probable values $\kappa_0/2\pi$ of the C11 chips, as well as the measured GVD parameters $D_2/2\pi$, are marked in each field over the wafer. NA: not applicable, due to visible defects or missing C11 chips near wafer edge.

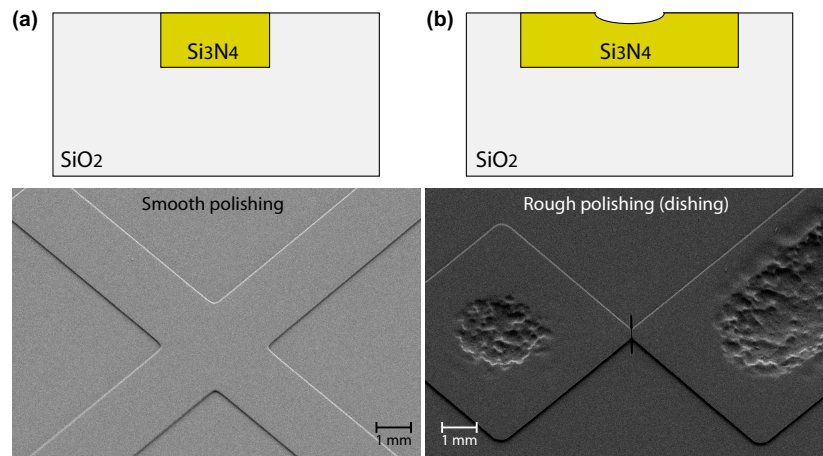


Fig. 7. Illustration of the CMP dishing effect observed during fabrication. (a) SEM images showing smooth top surface after CMP for waveguides with smaller critical dimension (e.g., below 3 μm). (b) SEM images showing rough top surface due to the CMP dishing effect for waveguides with larger critical dimension (above 3 μm).

in Ref. [14], the patterns are transferred from the photoresist mask to the SiO₂ substrate to create waveguide preforms. Then, an LPCVD Si₃N₄ film is deposited on the patterned substrate, filling the preform trenches and forming the waveguides. CMP is used to remove excess Si₃N₄ and create a flat and smooth wafer top surface. The rest steps are the same as the subtractive process.

It should be noted that the dishing effect, illustrated in Fig. 7, is commonly presented if the CMP polishing rates for the waveguide material and cladding are different (which is true for Si₃N₄ and SiO₂). In the Damascene case, the CMP slurry containing SiO₂ nano-particles makes the polishing rate of Si₃N₄ higher than that of thermal wet SiO₂, which induces the dishing effect in large-area patterns (e.g., critical dimension larger than 3 μm). The dishing effect leads to significant structure distortion and top surface roughness.

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the soliton generation experiment. L. G. took the photos of the sample. Y.-H. L., B. S., and J. Liu analyzed the data and prepared the paper with input from others. J. Liu supervised the project and managed the collaboration.

Disclosures. Z. Y., H. J., Z. H., and J. Liu are co-founders of Qaleido Photonics, a start-up that is developing heterogeneous silicon nitride integrated photonics technologies. Others declare no conflicts of interest.

Data Availability. The original data and data used to produce the plots within this work are available on Zenodo [103]. All other data used in this study are available from the corresponding author upon reasonable request.

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