

Silicon photonics for high-capacity data communications

YAOCHENG SHI,^{1,*} YONG ZHANG,² YATING WAN,^{3,4} YU YU,⁵ YUGUANG ZHANG,^{6,7} XIAO HU,^{6,7} XI XIAO,^{6,7} HONGNAN XU,^{1,8} LONG ZHANG,¹ AND BINGCHENG PAN¹

¹Centre for Optical and Electromagnetic Research, State Key Laboratory for Modern Optical Instrumentation, College of Optical Science and Engineering, Zhejiang University, Zijingang Campus, Hangzhou 310058, China

²State Key Laboratory of Advanced Optical Communication Systems and Networks, Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China

³Institute for Energy Efficiency, University of California Santa Barbara, Santa Barbara, California 93106, USA

⁴Electrical and Computer Engineering Department, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia

⁵Wuhan National Laboratory for Optoelectronics & School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China

⁶National Information Optoelectronics Innovation Center, China Information and Communication Technologies Group Corporation (CICT), Wuhan 430074, China

⁷State Key Laboratory of Optical Communication Technologies and Networks, China Information and Communication Technologies Group Corporation (CICT), Wuhan 430074, China

⁸Department of Electronic Engineering, The Chinese University of Hong Kong, Shatin, New Territories, Hong Kong, China

*Corresponding author: yaocheng@zju.edu.cn

Received 25 February 2022; revised 15 May 2022; accepted 2 June 2022; posted 3 June 2022 (Doc. ID 456772); published 19 August 2022

In recent years, optical modulators, photodetectors, (de)multiplexers, and heterogeneously integrated lasers based on silicon optical platforms have been verified. The performance of some devices even surpasses the traditional III-V and photonic integrated circuit (PIC) platforms, laying the foundation for large-scale photonic integration. Silicon photonic technology can overcome the limitations of traditional transceiver technology in high-speed transmission networks to support faster interconnection between data centers. In this article, we will review recent progress for silicon PICs. The first part gives an overview of recent achievements in silicon PICs. The second part introduces the silicon photonic building blocks, including low-loss waveguides, passive devices, modulators, photodetectors, heterogeneously integrated lasers, and so on. In the third part, the recent progress on high-capacity silicon photonic transceivers is discussed. In the fourth part, we give a review of high-capacity silicon photonic networks on chip. © 2022 Chinese Laser Press

<https://doi.org/10.1364/PRJ.456772>

1. INTRODUCTION

With the development of big data and Internet of Things, the demand for data centers and high-performance computing (HPC) is increasing. An extremely large link capacity for high-speed datacom interconnects between multi-cores or local/distant caches is strongly required. However, it is becoming increasingly difficult for the conventional electrical interconnects to meet the ever-growing capacity requirement since they severely suffer from limited bandwidth and significant power consumption. The demand of high-capacity, reliable, and low-cost optical data links has led to the development of photonic integrated circuits (PICs) to improve the power efficiency, latency, and capacity. The single wavelength channel capacity for the conventional transceiver modules composed of discrete optical components is usually 50–100 Gb/s. Next-generation

high-capacity data communication systems will require dramatically increased complexity that cannot be obtained by simply increasing the number of channels using discrete optical components. Silicon-based optoelectronic technology can significantly increase the integration density and reduce the cost and energy consumption, which has great potential in the future. The key driving force behind silicon photonics is the ability to use complementary metal-oxide-semiconductor (CMOS)-compatible fabrication resulting in high-volume production at low cost. The high-confinement silicon waveguides make them ideal for medium- to high-density integration with compact silicon photonic devices. Silicon based PICs provide a promising solution to resolve the dilemma of scaling system complexity while reducing the size, energy, and cost [1,2]. In the case of silicon-based PICs, the optical circuit can be built up on a large-diameter silicon-on-insulator (SOI) substrate

with almost all the required components, including the modulators [3], multiplexers [4], and photodetectors [5], realized by the CMOS-compatible processes. The lack of a reliable silicon laser has been the major impediment due to the fundamental indirect bandgap limit of silicon material. Heterogeneous integration of III–V material to the silicon platform using the wafer bonding technology has been demonstrated to achieve on-chip lasers [6].

In this paper, the key components for high-speed optical communication and high-capacity data communication systems, including wavelength multiplexing devices, polarization management devices, mode multiplexing devices, heterogeneously integrated lasers, modulators, and optical functional devices realized on silicon photonics platforms are explained. The integration of III–V lasers, modulators, and other functional devices to form transceiver modules is also reviewed. This review on silicon photonics delves into the different technologies of the field, giving an insight into the state of the art as well as current and future challenges.

2. SILICON PHOTONIC BUILDING BLOCKS

A. Passive Devices

Silicon passive devices are fundamental elements in silicon photonics, which are defined as integrated devices without supplying electrical signals. Edge couplers, grating couplers, crossings, bends, couplers, and splitters are essential components of passive devices, which have been reviewed by some excellent papers [7,8]. These silicon passive devices are included in the process design kit (PDK) library provided by the foundries [9,10]. Functional silicon integrated chips can be assembled by these basic elements. Therefore, the development routine of integrated chips is simplified for the users. To meet the demand for high-capacity data communications, multiple physical dimensions of an optical carrier can be exploited for multiplexing on an SOI platform, including wavelength, polarization, and mode. Silicon passive devices that can operate in one or more of the three dimensions have been developed. In this section, we review the passive devices for the three dimensions, including wavelength multiplexing, polarization handling, and mode multiplexing devices.

1. Wavelength Multiplexing Devices

On-chip wavelength-division multiplexing (WDM) devices are utilized to multiplex a number of optical signals with different wavelengths into a single waveguide. Many basic structures have been used to realize on-chip WDM devices, such as microring resonators (MRRs), Mach–Zehnder interferometers (MZIs), arrayed waveguide gratings (AWGs), and Bragg gratings.

Silicon MRR attracts much attention due to its easy design and compact footprint. An add-drop type MRR can be utilized as a wavelength multiplexing or filtering device, which consists of a looped waveguide with two side-coupled straight waveguides. The light with on-resonance wavelength is selected and coupled to the Drop port, while the signal with off-resonance wavelength output from the Thru port. Correspondingly, the light with on-resonance wavelength from the Drop port and the signal with off-resonance wavelength from the Thru port can be multiplexed in the Input port, i.e., the multiplexing function is achieved. The operation bandwidth of the MRR-based WDM

system is limited by the relatively small free spectral ranges (FSRs) of the rings, which is inversely proportional to the total length of the ring. An ultrasharp waveguide bend can be introduced to achieve a small radius ring with a large FSR. A large FSR of 93 nm is obtained in an add-drop multimode MRR with a radius of 0.8 μm [11]. The Vernier effect in cascading MRRs with different FSRs [12,13] or coherent interference method [14,15] can be also used to achieve larger FSRs. The spectral response of a single MRR is expressed by Lorentzian function, while a box-like spectral response is desired in the WDM system. The combinations of multiple MRRs are utilized to improve the spectral response, such as series coupling, parallel coupling, and cascaded topology. Quadruple Vernier racetrack resonators on an SOI platform are demonstrated with a ripple of 0.2 dB, an adjacent channel isolation of 37.2 dB, and an FSR of 37.52 nm [16]. Second- and fifth-order ring filters are reported with a bandwidth of 1–2 GHz, FSRs of 50 GHz, and out-of-band extinction ratios of 50 dB [17]. More recently, the second-, third-, and fourth-order adiabatic elliptical-MRRs are proposed to achieve box-like spectral responses with a large FSR of 37 nm as shown in Fig. 1(a). Based on the high-order MRRs, an optical filter is demonstrated with eight channels, a channel spacing of 3.2 nm, and cross talk of < -30 dB [18]. An important issue of the MRRs is the wavelength misalignment, which may be induced by the fabrication imperfections or temperature fluctuations. Thermal tuning is generally used to align the wavelengths, which introduces extra power consumption and increases the management complexity [19].

MZIs with different arm lengths can be used to realize wavelength multiplexing or filtering. Unlike the unwanted nonlinear effect induced by the field enhancement in the looped waveguide of the MRR, MZIs without field enhancement can work for optical signals with higher power. As shown in Fig. 1(b), a 1-to-8 wavelength (de)multiplexer based on a binary tree of cascaded MZI lattice filters is demonstrated with a low

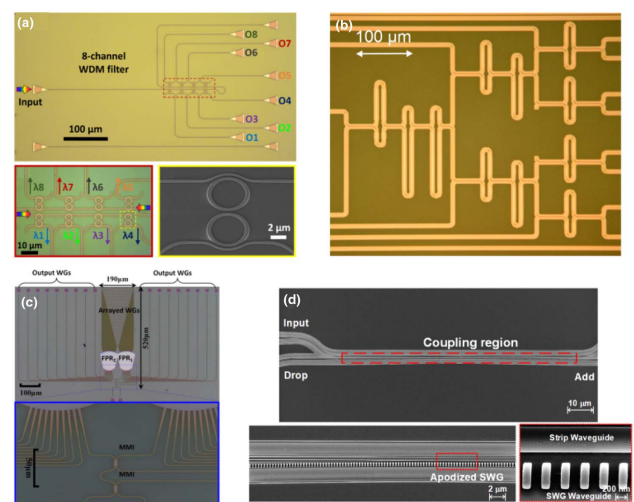


Fig. 1. (a) Optical microscope and scanning electron microscope (SEM) photos of an eight-channel add-drop filter based on second-adiabatic elliptical-MRRs [18]; (b) micrograph of a cascaded MZI (de)multiplexer [20]; (c) optical micrographs of a bidirectional A WG and an MZI-based interleaver [4]; (d) SEM photos of a contra-directional coupler based on an apodized SWG [21].

insertion loss of <1.6 dB and flat-topped responses [20]. Athermalization is another main requirement for a silicon filter. A hybrid strip-slot waveguide is introduced into one arm of the MZI structure to achieve athermalization. The temperature-dependent wavelength shift is -5 pm/K, and the insertion loss is 0.4 dB with a device footprint of $170 \mu\text{m} \times 580 \mu\text{m}$ [22]. Furthermore, a multifunctional optical filter is proposed, employing a self-coupled MRR assisted MZI structure, which exhibits flexible reconfigurability and tenability for reconfigurable optical signal processing and microwave photonics systems [23].

As the most well-known structure for dense wavelength division multiplexing (DWDM) applications, AWG is used to combine or split closely spaced wavelength channels of optical signal, which consists of two free propagation regions connected with arrayed waveguides [24]. High-performance AWGs have been realized on various material platforms, including silica [25] and silicon nitride [26]. The high index contrast offered by the SOI platform enables the realization of ultracompact AWGs. A compact 12-channel, 400 GHz silicon AWG is demonstrated with an insertion loss of 3.29 dB, cross talk of -17 dB, nonuniformity of 1.55 dB, and device size of $560 \mu\text{m} \times 350 \mu\text{m}$ [27]. An 8×8 silicon nanowire AWG with a channel spacing of 400 GHz and cross talk of -20.5 dB is fabricated by 130 nm CMOS processing [28]. However, for the silicon AWGs with smaller channel spacing, the insertion loss and the cross talk degrade significantly. 4×100 GHz, 8×250 GHz, and 12×400 GHz AWGs are demonstrated with insertion losses of 2.45, 1.32, and 0.53 dB and device footprints of $1180 \mu\text{m} \times 285 \mu\text{m}$, $540 \mu\text{m} \times 320 \mu\text{m}$, and $380 \mu\text{m} \times 330 \mu\text{m}$, respectively [29]. A 512×512 AWG with a channel spacing of 25 GHz is realized based on silicon rib waveguides with cross talk of -4 dB and a size of $16 \text{ mm} \times 11 \text{ mm}$ [30]. Combining a bidirectional AWG and an MZI optical interleaver is an approach to achieve doubled channel number and halved channel spacing. As depicted in Fig. 1(c), an 18-channel wavelength (de)multiplexer with a channel spacing of 200 GHz is fabricated with insertion losses of 8 dB and cross talk of -15 dB [4]. More recently, a 32-channel wavelength multiplexer with 100 GHz spacing is realized using two 16-channel AWGs with 200 GHz spacing and an MZI with 200 GHz FSR [31].

Bragg gratings with the advantages of the flat-topped spectral responses and large FSRs are utilized to realize wavelength multiplexing devices for coarse wavelength-division multiplexing (CWDM) applications. It is complemented by the periodic index perturbations on silicon waveguides. A typical two-port Bragg grating operates in reflection mode; thus, an optical isolator or circulator is required, which increases the device complexity. Many methods have been proposed to develop add-drop structures based on Bragg gratings, such as grating-assisted contradirectional couplers, multimode waveguide gratings, and subwavelength gratings (SWG). A wavelength multiplexer based on the asymmetric contradirectional coupler is reported with a channel spacing of ~ 3 nm and insertion losses of <0.58 dB [32]. A silicon triplexer is proposed based on cascaded multimode waveguide gratings, which is used to (de)multiplex three wavelength channels of 1310/1490/1550 nm. Box-like spectral responses are achieved with insertion losses of <0.9 dB and cross talk of <-27 dB. Furthermore, the cascaded multimode waveguide gratings are utilized to realize an on-chip quadplexer for four-wavelength multiplexing of 1270, 1310, 1490, and 1577 nm [33]. An apodized SWG coupler can be also utilized to realize a silicon add-drop filter with a high sidelobe suppression ratio of 27 dB and a 3 dB bandwidth of 8.8 nm as plotted in Fig. 1(d) [21].

Table 1 shows the state-of-the-art wavelength multiplexing devices.

2. Polarization Management Devices

Due to the large structural birefringence in the high-index-contrast silicon nanowire waveguides, polarization sensitivity is a major problem in silicon photonics. For a silicon waveguide with typical dimensions of $220 \text{ nm} \times 500 \text{ nm}$, the calculated effective refractive indices of the TE and TM polarization are 2.45 and 1.78, respectively. On-chip polarization-division multiplexing (PDM) devices are utilized to multiplex the optical signals with two orthogonal polarizations into a single waveguide channel. PDM devices have found many applications, such as integrated coherent transceivers, which have become critical components for high-capacity long-haul optical communications. Polarization beam splitters and rotators are essential components in the PDM system.

Table 1. State-of-the-Art Wavelength Multiplexing Devices^a

Reference	Type	Loss (dB)	ER (dB)	BW (nm)	FSR/Spacing (nm)	Channels
[11]	Submicrometer MRR	1.8	>17	0.8	93	2×2
[16]	Vernier racetrack	/	10.2	/	37.52	2×2
[17]	High-order MRR	2	50	0.008	0.4	1×2
[18]	Elliptical MRR	1.5	45	1.4	3.2	1×8
[20]	Cascaded MZI	1.6	15	/	2.4	1×8
[22]	Two-stage MZI	0.4	13.6	5	14.7	1×2
[27]	400 GHz AWG	3.29	17	/	3.2	1×12
[28]	400 GHz AWG	2.32	20.5	/	3.2	8×8
[29]	100 GHz AWG	2.45	17.1	/	0.8	4×4
[30]	25 GHz AWG	/	4	/	0.2	512×512
[31]	MZI + AWG	5	15	/	0.8	1×32
[32]	Asymmetric grating	0.58	10	/	3	3×3
[33]	Multimode grating	0.5	24	6	>40	1×4

^aER, extinction ratio; BW, bandwidth.

Polarization beam splitters (PBSs) are utilized to split or combine the orthogonal TE and TM polarizations in silicon nanowire waveguides. Many structures have been proposed to realize compact silicon PBSs, including directional couplers, multimode interferometers (MMIs), Y junctions, subwavelength structures, slot waveguides, and plasmonic waveguides. High extinction ratio (ER) is an important evaluation parameter of the PBS. Benefitting from the different coupling strength of the two polarizations in a directional coupler, a silicon PBS is demonstrated with an ER of 15 dB based on a symmetrical directional coupler (DC) with two identical silicon nanowire waveguides [34]. An asymmetrical directional coupler (ADC) is a good structure to obtain higher ER, since coupling only exists for one polarization in the structure with strong birefringence. A PBS based on an ADC consisting of a strip waveguide and a periodic waveguide is demonstrated with an ER of >30 dB and a loss of <1 dB [35]. An asymmetrical grating-assisted contradirectional coupler is employed to achieve a PBS with an ER of >30 dB in a wavelength range of 20 nm as shown in Fig. 2(a). A cascaded bent directional coupler is another option to increase the ER [40]. The measured ER is >35 dB, and the loss is <0.35 dB for the fabricated PBS. Broad operation bandwidth is another primary parameter to evaluate the PBSs. The working bandwidths of directional-coupler-based PBSs are limited due to the waveguide dispersion. Anisotropic metamaterials are exploited to realize an ultrabroadband silicon PBS [41]. The bandwidth is >200 nm with a low loss of <1 dB and an ER of >20 dB. Ultracompact device size is a goal for the on-chip PBSs. Many methods have been proposed to further reduce the length of the PBS, such as subwavelength structures and counter-tapered couplers. A PBS using a pixelated directional coupler is demonstrated with a

coupling length of 6 μm , a loss of <1.5 dB, and an ER of >14 dB [42]. A particle-swarm-optimized counter-tapered directional coupler is utilized to achieve a 5 μm long silicon PBS [43]. Furthermore, an SWG waveguide is introduced to shrink the length of the PBS to be only 2 μm [44].

The two orthogonal polarizations are maintained in a typical silicon nanowire waveguide with a rectangle cross section. The symmetry of the rectangle waveguide needs to be broken to excite the hybridized modes, which enable efficient polarization conversion. Adiabatic tapers are utilized to achieve mode-evolution-based polarization rotators [45]. Si_3N_4 -assisted adiabatic mode evolution is employed to realize a silicon polarization rotator with a length of 420 μm and a loss of 1 dB [46]. The length of the polarization rotator is long enough to guarantee the low loss and adiabatic conversion [47,48]. The cut-cornered structures are commonly used to break the symmetry of the waveguide for polarization conversion as shown in Fig. 2(b). Polarization rotators based on the cut-cornered structure are theoretically proposed with a conversion length of 10 μm [49] and experimentally demonstrated with a length of 25 μm using 193 nm deep ultraviolet lithography [50], respectively. Furthermore, a 23 μm long polarization rotator exhibits an ER of >17 dB based on double-stair waveguide dimension [51]. In addition, subwavelength structures [52,53] and digital metamaterials [54,55] can be also employed to realize compact and ultrabroadband polarization rotators.

Polarization splitters and rotators (PSRs) combine the functions of polarization splitting and rotating simultaneously. Mode evolution and mode coupling methods can be used to achieve PSRs [45]. For mode-evolution PSRs, adiabatic couplers are used to convert the TM polarization to TE high-order mode; then, mode converters or (de)multiplexers are utilized to couple TE high-order mode to the TE fundamental mode [56,57]. Highly efficient $\text{TM}_0 - \text{TE}_1$ conversion is enabled by the mode hybridization region in the multimode waveguide. Then the TE_1 mode is converted to the TE_0 mode by ADC structure as depicted in Fig. 2(c). The fabricated PSR exhibits an ER of >30 dB and a loss of <0.57 dB. For mode coupling PSRs, the vertical and horizontal symmetries of the waveguides are broken; thus, the coupling exists between two orthogonal polarizations with equal effective indices. One method to break the vertical symmetry is to use air as a top-cladding material. ADC structure with air cladding is utilized to achieve a PSR with a loss of <0.6 dB and a coupling length of 36.8 μm [58]. Tapered ADC with a length of 140 μm is used to achieve a fabrication-tolerant PSR [59]. Furthermore, bent ADC with stronger birefringence is employed as a PSR with a much shorter length of 8.77 μm [60]. Asymmetrical waveguide cross section by multistep etch is another option to break the vertical symmetry. A double-etched ADC is employed to realize a silicon PSR with a length of 27 μm and an ER of 20 dB [61]. A fabrication-tolerant and broadband PSR is demonstrated using a linearly tapered ADC with a length of 700 μm [62]. To shrink the device size, a nonlinearly tapered double-etched ADC is utilized to realize a PSR with a length of 129 μm and high fabrication tolerance as shown in Fig. 2(d). Other structures can be also used to achieve silicon PSRs, such as MZI [63], Y branch [57], and S-bend [64].

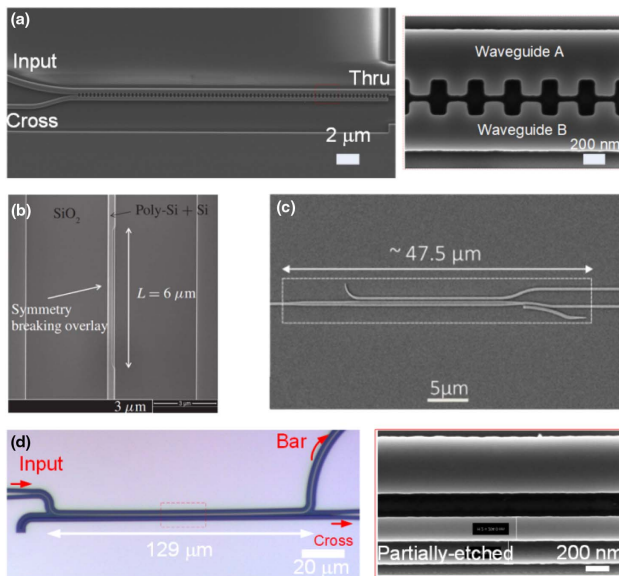


Fig. 2. (a) SEM photos of a PBS based on grating-assisted contradirectional couplers [36]; (b) SEM photo of a cut-cornered polarization rotator [37]; (c) SEM photo of a PSR based on multimode waveguide and mode converter [38]; (d) micrographs of a PSR employing a nonlinearly tapered double-etched ADC structure [39].

Table 2. State-of-the-Art Polarization Management Devices

Reference	Type	Loss (dB)	XT (dB)	BW (nm)
[36]	Grating-assisted contra directional couplers	1	30	20 (XT > 30 dB)
[38]	Multimode waveguide	0.57	30.82	85 (XT > 20 dB)
[34]	Symmetrical DC	<0.5	15	C-band (XT > 15 dB)
[35]	Asymmetric DC	<1	30	100 (XT > 25 dB)
[40]	Cascaded bent DC	<0.35	35	70 (XT > 30 dB)
[41]	Hetero-anisotropic metamaterials	<1	>20	200 (XT > 20 dB)
[42]	Pixelated DC	1.53	14.22	53 (XT > 14 dB)
[46]	Si ₃ N ₄ -assisted mode evolution	1	30	60 (XT > 30 dB)
[51]	Mode-hybridization	2	17	40 (XT > 17 dB)
[58]	ADC	0.6	12	C-band (XT > 12 dB)
[60]	Bent DC	<1	18	70 (XT > 18 dB)
[61]	Double-etched DC	0.5	20	30 (XT > 20 dB)

Table 2 shows the performance of reported polarization management devices.

3. Mode Multiplexing Devices

Orthogonal modes supported by silicon multimode waveguides can carry different optical signals and propagate independently in the waveguides, which offer another dimension to increase the multiplexing channel numbers and the total communication capacity. Mode (de)multiplexers are one critical building block in mode-division multiplexing (MDM) system, and they are capable of multiplexing the optical signals into different orthogonal waveguide modes. Lots of structures have been proposed to realize silicon mode multiplexers, such as MMIs [65,66], Y junctions [67,68], ADCs [69,70], plasmonic waveguides [71], and inverse design waveguides [72].

A silicon two-mode (de)multiplexer is proposed based on two MMIs and a butterfly-shape tapered phase shifter in theory [73]. An MMI-based mode (de)multiplexer is experimentally demonstrated with a loss of <0.36 dB, cross talk of <-24.4 dB, and a size of 3.8 μm \times 160 μm for TE₀ and TE₁ mode multiplexing [74]. Good fabrication tolerances are verified for MMI-based devices, while the devices exhibit relatively large footprint and poor scalability. Recently, a silicon three-mode multiplexer based on a shallow-etched MMI is presented based on the two-step mode conversion process in the MMI region as shown in Fig. 3(a) [75]. Higher-order mode multiplexers can be further scaled using a multistep mode conversion in the MMI structure.

Asymmetric few-mode and multimode weakly guiding Y junctions have been proposed to be suitable for mode sorting [77]. A silicon two-mode multiplexer is experimentally reported with a loss of <1.5 dB and a length of 1.2 mm based on asymmetric Y junctions as shown in Fig. 3(b) [68]. Furthermore, an MDM on-chip link with bit rate of 20 Gb/s is demonstrated using the devices [78]. Small branching angle is needed to satisfy adiabatic evolution, leading to very long length (hundreds of micrometers) of the Y junctions. A short and broadband asymmetric Y-junction-based two-mode multiplexer is theoretically proposed using fast quasi-adiabatic dynamics. A mode multiplexer is obtained with a length of 16 μm and cross talk of <-34 dB [79].

ADC is the most popular structure to realize on-chip mode multiplexing due to the advantages of compact footprint, good scalability, and easy design. The fundamental mode in an access

waveguide is coupled into a bus waveguide as a high-order mode; 4-channel [69], 8-channel [80,81], and 10-channel [70] mode (de)multiplexers are implemented using this structure as shown in Fig. 3(c). Due to the strong waveguide dispersion, the bandwidth of the ADC-based mode multiplexers is limited. Tapered ADCs can be utilized to broaden the bandwidth. A three-mode multiplexer is demonstrated with a 1 dB bandwidth of 180 nm using counter-tapered couplers [82]. The fundamental mode in the access waveguide and the high-order mode in the bus waveguide exhibit significantly different dependences of the effective indices on the waveguide widths, leading to a fragile phase-matching condition for mode coupling. SWG waveguides are utilized to tailor the dispersion curves of the waveguide modes, resulting in robust high-order mode multiplexers. 11-mode multiplexing on a TE-polarized light (TE₀ - TE₁₀) is experimentally demonstrated with losses of <2.6 dB and cross talk of -15.4 dB. More recently, a 16-channel mode (de)multiplexer (TE₀ - TE₁₅) was reported using gradient-duty-cycle SWGs as shown in Fig. 3(d) [76]. The device is characterized with 16-channel 112 Gb/s 16-ary quadrature amplitude modulation (16-QAM) signals to achieve a 1.51 Tb/s/polarization/wavelength capacity at 1550 nm.

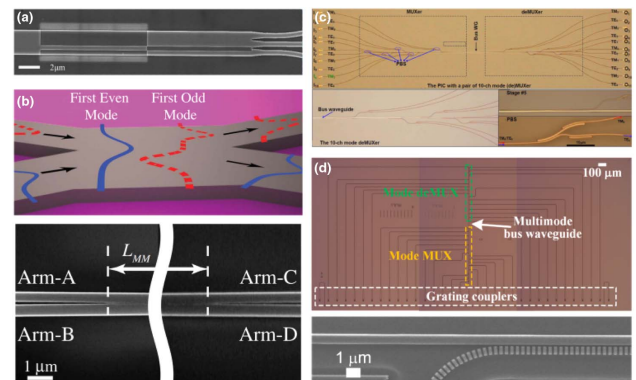


Fig. 3. (a) SEM photo of a three-mode multiplexer based on a shallow-etched MMI [75]; (b) illustration of mode multiplexer using asymmetric Y junctions [68]; (c) micrographs of a 10-channel mode multiplexer based on ADC structures [70]; (d) photos of a 16-channel mode (de)multiplexer (TE₀ - TE₁₅) using gradient-duty-cycle SWGs [76].

The inverse design method is applied to further minimize the size of the mode multiplexing devices [83]. Ultracompact three-mode multiplexers, multimode bending, and crossings are implemented based on the optimized discretized metastructure [72]. 112 Gb/s signals encoded on each mode are successfully transmitted on the devices.

Table 3 compares various state-of-the-art silicon mode multiplexing devices.

In terms of insertion loss, cross talk, footprint, and multiplexing channels, significant progress has been made for on-chip multiplexing devices, including wavelength-, polarization-, and mode-multiplexing devices. Multiple physical dimensions can be combined to further increase the capacity. Many interesting works have been reported to build on-chip multidimensional multiplexing and switching devices [84–86]. The relatively large cross talk between channels is an important issue, especially for multidimensional multiplexing with lots of channels. A low-coherence matched detection method may be a possible approach to ease the cross talk requirement [87]. The capacity of an optical communication system depends on the number of available orthogonal channels in the physical dimensions. A larger capacity can be enabled by more wavelength/mode channels. Wavelength-division multiplexing can provide tens of data channels employing AWG or cascaded MRR structures. High cross talk is challenging in silicon AWG ($XT > -4$ dB in a 25-GHz AWG) due to the phase errors in the silicon nanowire waveguide introduced in the fabrication. Since the MRR resonance is sensitive to fabrication errors and temperature variations, wavelength misalignment between channels is a critical issue for the cascaded MRR scheme. The wavelength locking method can be utilized to align the wavelengths, at the cost of the device complexity. Current state-of-the-art mode-division multiplexing technologies have achieved 16 single-polarization modes on silicon chips, enabling a 1.51 Tb/s/polarization/wavelength capacity at 1550 nm. Since the coupling between high-order modes is sensitive to the waveguide dimensions, suppressing the modal cross talk is a vital task in the future.

Another concerning is high-efficiency coupling between the high-order modes of the rectangle waveguides and the LP modes of the few-mode fibers [88]. Due to the large phase mismatch between the waveguide modes and the LP modes, the implementation of the multimode coupler is challenging. Many efforts have been made to achieve a multimode coupler

employing grating couplers [89] or edge couplers [90]. Edge couplers for few-mode fiber coupling are theoretically proposed to couple four silicon waveguide modes of TE_0 , TM_0 , TE_1 , TM_1 [91] and six waveguide modes of TE_{11} , TE_{21} , TE_{31} , TE_{41} , TM_{11} , TM_{12} [90] to linearly polarized (LP) modes in the few-mode fiber, respectively. Direct coupling between higher-order modes in a few-mode fiber and modes in a silicon waveguide is demonstrated experimentally using nonlinear 3D adiabatic tapering to ensure one-to-one modal coupling [92]. The nonlinear tapering enables conversion between four silicon TE modes to larger rectangular modes in an SU-8 polymer waveguide, followed by the conversion between the larger modes in the rectangular waveguide to the circular modes in the few-mode fiber. A silicon edge coupler consisting of a 1×3 symmetrical MMI and a triple-tip inverse taper is demonstrated to achieve dual-mode fiber-to-chip coupling [93]. LP_{01} and LP_{11} modes are launched by the edge coupler with low loss and low cross talk over 90 nm bandwidth. 2×100 Gb/s/wavelength four-pulse amplitude modulation (PAM-4) mode-division multiplexing transmission is also demonstrated over 40 m dual-mode fiber. A subwavelength waveguide grating coupler is proposed and demonstrated for two polarizations of the LP_{01} mode and the LP_{11} mode with coupling efficiencies of -4.9 dB and -6.1 dB, which are optimized using the genetic optimization algorithm [89]. Table 4 compares various state-of-the-art couplers for few-mode fiber coupling. Higher coupling efficiency and good scalability to support more mode channels are the issues that need to be addressed.

B. Modulators

As one of the most essential components, high-performance optical modulators converting electrical signal to optical signal are highly desired. For the unique characters of high integration, low cost, and CMOS ability, silicon photonics is considered to be one of the best candidates to achieve high-performance optical devices, and the topic has been intensively researched [2]. However, due to its centrosymmetric crystal lattice, silicon has almost no linear electro-optic effect (i.e., Pockels effect) [94]. To realize modulation based on silicon, the thermal effect and the plasma dispersion effect are investigated [9]. Since the large response time of thermal effect [limiting the response frequency smaller than megahertz (MHz)] [95], most high-speed silicon modulators are demonstrated based on the plasma dispersion effect. Plasma dispersion

Table 3. State-of-the-Art Mode Multiplexing Devices

Reference	Type	Loss (dB)	XT (dB)	BW (nm)	Channels
[65]	MMIs	<1	28	C-band ($XT > 28$ dB)	3
[68]	Y junctions	1.5	30	C-band ($XT > 30$ dB)	2
[70]	ADCs	1.8	15	90 ($XT > 15$ dB)	10
[71]	Plasmonic waveguide	0.35	17	100 ($XT > 17$ dB)	2
[72]	Inverse design waveguide	8	20	80 ($XT > 20$ dB)	3
[73]	MMIs and tapered phase shifter	1	37	60 ($XT > 37$ dB)	3
[74]	MMIs	0.36	24.4	60 ($XT > 20$ dB)	3
[75]	Shallow-etched MMI	2.4	10	70 ($XT > 10$ dB)	3
[76]	SWGs	0.8–5.2	9.2–24	/	16
[79]	Asymmetric Y junction	/	34	300 ($XT > 34$ dB)	2
[82]	Counter-tapered couplers	<0.74	10	100 ($XT > 10$ dB)	2

Table 4. State-of-the-Art Couplers for Few-Mode Fiber Coupling

Reference	Type	Loss (dB)	XT (dB)	Channels
[90]	SiN-waveguide-assisted edge coupler ^a	<0.5	-23	6
[93]	Triple-tip inverse taper	13.2	-7.3	2
[91]	Mode-evolution counter-tapers ^a	5.1	-25	4
[92]	SU8-waveguide-assisted edge coupler	5	/	4
[89]	Subwavelength grating coupler	6.1	/	4

^aSimulation results; XT, cross talk.

is an electro-refractive effect, depending on the change of free carrier concentration in the region occupied by the optical mode of the waveguide. There are three mechanisms to introduce change of the free carrier concentration in the silicon modulator: (a) carrier injection; (b) carrier accumulation; (c) carrier depletion [96].

Silicon modulators based on carrier injection provide a largest change of the free carrier concentration with the same driving voltage [97–99]. However, suffering from the long free-carrier recombination time and the large resistance, the bandwidth of carrier injection modulators is limited to be about gigahertz (GHz) [100]. To extend the bandwidth of the carrier injection modulator, the passive RC equalizer is utilized by inserting an $R_E C_E$ filter [101,102]. Through this approach, a high-bandwidth carrier injection modulator is demonstrated with the EO bandwidth of 42.6 GHz, supporting 70 Gbaud PAM-4 operation [103]. For the carrier accumulation modulators, a thin insulating oxide gate [several nanometers (nm)] should be inserted between the n-type and the p-type silicon. Generally, due to the fabrication difficulty of the lateral carrier accumulation phase shifter, the vertical carrier accumulation phase shifters are more attractive [104,105]. The high carrier concentration on each side of the oxide gate provides the high modulation efficiency. A 28 Gb/s vertical carrier accumulation modulator is proposed with the $V_\pi \cdot L$ of $<0.2 \text{ V} \cdot \text{cm}$, allowing the phase shifter to be directly driven by CMOS driver circuit [106,107]. Recently, with the improvement of fabrication process, horizontal carrier accumulation modulators are fabricated by depositing amorphous Si into silicon trenches [108,109]. The EO bandwidth of 35 GHz and $V_\pi \cdot L$ of $1.8 \text{ V} \cdot \text{cm}$ (due to the large oxide gate of 40 nm) are demonstrated, enabling 72 Gb/s modulation [110].

Carrier depletion modulators featuring low optical loss, ease of fabrication, and large EO bandwidth are the most widely adopted scheme [111,112]. However, they exhibit a low modulation efficiency due to the limited capacitance [113]. In order to improve the modulation efficiency and optimize modulator speed, various configurations of PN junctions, including vertical PN junction [114], L-shaped PN junction [115], U-shaped PN junction [116], and interleaved PN junction [117], are proposed to enhance the interaction between the electrical field and the optical mode field as shown in Fig. 4. Vertical PN junction has advantages in providing high overlap between the optical mode and the depletion region, and the high modulation efficiency of 30 GHz/V has been demonstrated with the data rate of 25 Gb/s [118]. Reducing optical loss is another important orientation. Lateral PN junction with doping compensation is utilized to decrease the optical loss

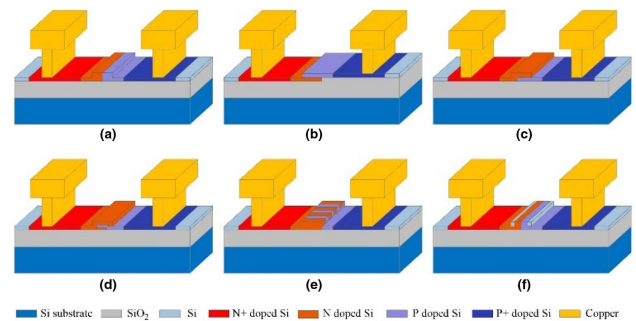


Fig. 4. Various configurations of carrier depletion PN junctions. (a) Lateral PN junction, (b) vertical PN junction, (c) L-shaped PN junction, (d) U-shaped PN junction, (e) interleaved PN junction, and (f) lateral PN junction with doping compensation.

while maintaining the modulation efficiency, and the measured bandwidth can be improved from 10 to 17 GHz [119].

To translate phase modulation into intensity modulation, modulators are usually designed based on MZIs and resonant cavities (MRR, microdisk, photonic crystal cavity) as shown in Fig. 5.

Figure 5(a) shows the schematic of the Mach-Zehnder modulator (MZM). Since the low modulation efficiency of the carrier depletion effect, to achieve sufficient modulation depth, the length of the modulator should be about several millimeters (mm). To reduce the size of the modulator, the literature reports some smart design strategies. For example, a slow-light waveguide [120–122] enables us to increase the electrical-optical interaction time, resulting in high modulation efficiency. With slow-light waveguide length of $500 \mu\text{m}$, a silicon modulator with EO bandwidth of 30 GHz, $V_\pi \cdot L$ of $0.85 \text{ V} \cdot \text{cm}$, and 112 Gb/s PAM-4 modulation is demonstrated [120]. On the other hand, the EO bandwidth can be much extended by reducing the short modulation length. EO

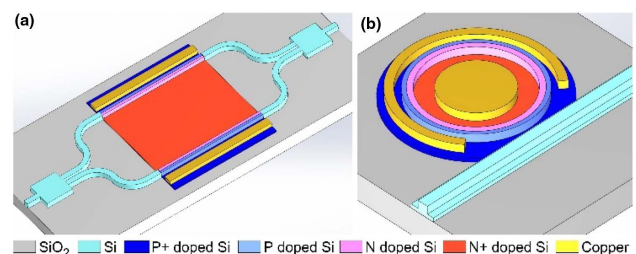


Fig. 5. Schematic of silicon modulator. (a) MZM, (b) MRR modulator.

bandwidth of 110 GHz is demonstrated based on an ultracompact silicon slow light modulator with modulation length of 124 μm [122]. The input light can be modulated twice in the Michelson interferometer modulators [123–125] and doubles the effective modulation length. High modulation efficiency with the $V_\pi \cdot L$ of 0.72 V · cm is provided by a Michelson interferometer modulator with the modulation data rate of 40 Gb/s [123]. However, the EO bandwidth for slow-light waveguide modulators and Michelson interferometer modulators is limited due to the velocity mismatch between the optical signal and the electrical signal.

To improve the EO bandwidth, the traveling-wave electrode (TWE) is commonly utilized to drive the carrier depletion modulator. The EO bandwidth of the TWE modulators is affected by (i) the velocity mismatch between the propagation speed of the optical signal in the waveguide and the electrical signal in the TWE; (ii) the impedance mismatch of the TWE to the impedance of the driver and the terminator; and (iii) the microwave attenuation resulting from the TWE and the PN junction. Researchers have made many efforts to investigate the electrical model of the TWE modulator to improve the EO bandwidth [126–128]. By introducing the optical delay loops, or slow-wave electrode, the velocity matching can be achieved. An open eye diagram is observed up to bitrate of 70 Gb/s with a slow-wave series TWE modulator [129]. The impedance matching is realized by carefully designing the structure of the TWE, and the modulation speed even at 2 μm wave band can reach 80 Gb/s with PAM-4 formats [130]. A small resistance of the terminator is beneficial for improving the EO bandwidth of the MZM, by suppressing the modulation depth at low frequency instead of enhancing that at high frequency [127]. A high EO bandwidth of approximately 47 GHz is experimentally demonstrated by peaking the frequency response through implementing a 35 Ω on-chip terminator to the TWE with the characteristic impedance of 50 Ω , allowing 220 Gb/s/ λ net rate operation [131].

The microwave attenuation is partly coming from the capacitance of the PN junction, which means that the EO bandwidth of the MZM can be improved by lowering the doping concentration [132], reducing the cross section of the PN junction, or utilizing push-pull structure [133]. Lowering the doping concentration or reducing the cross section of the PN junction will decrease the modulation efficiency, so the designers should trade off these two conflicts. Since the two PN junctions are connected in series, the loaded capacitance will be half of single PN junction capacitance for push-pull modulators [134]. From another perspective, the substrate silicon of the device will also introduce microwave loss, and it can be reduced by substrate removal [135] as shown in Fig. 6(a). Through this method, the modulator with the EO bandwidth of beyond 50 GHz is achieved, enabling 90 Gbaud on-off keying (OOK) and 128 Gb/s PAM-4 signal transmission [136]. The synergistically designed electrical CMOS driver is utilized to solve the bandwidth limitation of silicon modulators, and 100 Gb/s OOK is experimentally demonstrated without using any equalization with the power consumption of 2.03 pJ/bit for the driver [137] as shown in Fig. 6(b).

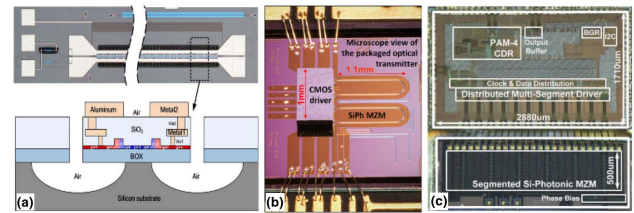


Fig. 6. (a) High-bandwidth MZM with substrate removed [135], (b) electronic–photonic synergistically designed silicon photonics transmitters [137], (c) lump-segmented silicon transmitter with six lumped phase shifters [138].

By carefully controlling the propagation delay difference between the optical and electrical path and lowering the power consumption of each driver, modulators based on segmented electrodes [139] will be another efficient approach to reduce the microwave attenuation due to the long TWE. The driving voltage is maintained all the same along the segmented electrode, which can be modeled as a lumped model [139]. A lump-segmented silicon transmitter with the data rate of 50 Gb/s PAM-4 is proposed by integrating six lumped phase shifters driven by six drivers [138] as shown in Fig. 6(c).

Silicon modulators based on resonant cavity have the advantages of low optical loss, low driving voltage, and small footprint, which are crucial for high-density optical interconnect, particularly co-packaged optics (CPO) [140]. For the simple structure, microring modulators (MRMs) are widely investigated for resonant cavity modulators [141–143] as shown in Fig. 5(b).

To extend the EO bandwidth further, the optical peaking enhancement (OPE) [144] caused by the intrinsic time dynamics is investigated. Assisted with OPE, the MRM with the EO bandwidth of 50 GHz is achieved with $V_\pi \cdot L$ of 0.52 V · cm, supporting 128 Gb/s PAM-4 modulation [112]. With the similar design, the transmission speed is doubled through a polarization demultiplexer to 260 Gb/s/ λ [145]. By optimizing the doping concentration of the PN junction, the MRM with the EO bandwidth larger than 67 GHz is demonstrated, enabling 120 Gb/s none return to zero (NRZ) and 200 Gb/s PAM-4 transmission [146]. The highest baud rate of 128 Gbaud NRZ is proposed based on the MRM with the EO bandwidth of 77 GHz and $V_\pi \cdot L$ of 0.53 V · cm [147] as shown in Fig. 7(a). The smallest MRM based on carrier accumulation with the radius of 1.5 μm , the modulation efficiency of 30 GHz/V, and

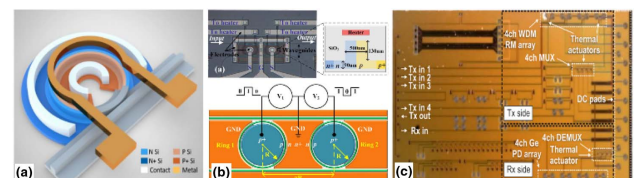


Fig. 7. (a) High speed MRM for next generation energy-efficient optical networks beyond 100 Gbaud [147], (b) push-pull silicon dual-ring modulator with enhanced optical modulation amplitude [148], (c) 4 × 40 Gb/s O-band WDM silicon photonic transmitter based on MRMs [149].

10 Gb/s NRZ modulation is fabricated in a 45 nm monolithic CMOS electronic-photonic process [150]. The MRM can also be utilized for advanced modulation formats [151,152], and 56 Gb/s QPSK modulation is demonstrated [153].

The cascaded MRMs either in series [148,154] or in parallel [155] operating with push-pull configuration are also proposed to enhance the modulation depth and suppress the frequency chirp. Based on the push-pull dual-ring modulator, the maximum optical modulation amplitude (OMA) is improved about 100% @ 10 Gb/s and 81% @ 20 Gb/s compared to that of the single MRM [148]. A low-chirp high-speed push-pull dual-ring modulator has been experimentally demonstrated with the EO bandwidth of 42 GHz and 144 Gb/s PAM-4 data transmission [154]. Due to the natural advantage of the MRMs, only modulating the particular wavelength, they are quite suitable for WDM systems [156]. An all-silicon MRM-based WDM transceiver is proposed with 50 Gb/s/λ at low BER ($<10^{-12}$) [157].

For their ultracompact footprint, photonic crystal cavity modulators are studied and experimentally demonstrated. Due to the small active region, the modulation depth for photonic crystal cavity modulator is limited. Thus, the early demonstrations of photonic crystal cavity modulators are proposed based on carrier injection with high modulation efficiency [158]. The PIN photonic crystal cavity modulator with the EO bandwidth of 1.3 GHz is demonstrated, operating at 3 Gb/s NRZ modulation with the charging energy less than 1 aJ/bit [159]. Recently, to extend the EO bandwidth, photonic crystal cavity modulators relying on carrier depletion are proposed. A side-coupled photonic crystal cavity modulator with the EO bandwidth of 2.8 GHz (limited by the large resistance) and 5 Gb/s modulation is presented [160]. The highest speed photonic crystal cavity modulator is experimentally demonstrated with the EO bandwidth of 38.6 GHz and modulation data rate of 70 Gb/s [161].

The resonant wavelength of the resonant cavity modulators is sensitive to the fabrication error or temperature variation. To solve this problem, integrated heater and thermal control circuit should be implemented, which will increase the design difficulty and power consumption [162]. Passive temperature compensating maintains the resonant wavelength with

temperature variation [163], while the mode field distribution should be carefully designed.

Nowadays, digital signal processing (DSP) is extensively studied to realize high-speed modulation. With post-filter and maximum likelihood sequence detection (MLSD), single-lane bit rate of 200 Gb/s (80 Gbaud) PAM-6 is achieved based on the MZM with EO bandwidth of 22.5 GHz [164]. By optical pre-emphasis filter and nonlinear digital pre-compensation, modulation data rate up to 1 Tb/s with dual-polarization higher-order 32-QAM is demonstrated [165]. Just utilizing linear digital compensation in both the transmitter and the receiver sides, 120 Gbaud QPSK and 100 Gbaud 32-QAM operations are experimentally demonstrated based on a silicon in-phase and quadrature (IQ) modulator [166]. The highest modulation with the net rate of 305 Gb/s is demonstrated, based on the TWE modulator with the EO bandwidth of 47 GHz [167]. For MRM, through compensating the nonlinearity, 302 Gb/s optical interconnection [168] is experimentally demonstrated, which is the highest data rate ever reported for MRM. Table 5 shows the state-of-the-art silicon modulators, including MZMs and MRMs.

Over recent year, many efforts have been made to improve the overall performance of silicon modulators, including the PN junction optimization [114–119] and the design of the TWE [126–131]. The performance of silicon modulator itself is well explored. For high-capacity data communications, reducing the size of the silicon modulators is of great importance, which means that silicon MRMs [141–152] will be one of the best approaches. The resonant wavelength control of the MRMs will be the research focus. On the other hand, the electronic-photonic co-design [137] can combine the advantages of electronics and photonics, and it will be an efficient approach to solve the bandwidth limitation of the silicon modulators and to reduce the power consumption. DSP [164–168, 170] is a promising solution to enhance the system performance and to enable the high-capacity data communications.

Recently, lithium niobate thin film on insulator (LNOI) has emerged as a promising platform to form waveguide devices with good confinement [171], and LNOI modulators with a low drive voltage and ultrahigh bandwidth have been demon-

Table 5. State-of-the-Art Silicon Modulators

Reference	Type	BW (GHz)	$V_{\pi} \cdot L$ (V · cm)	IL (dB)	Length (mm)	Data Rate (Gb/s)
[103]	MZM	42.6	2.09	/	0.5	140
[131]	MZM	47	1.35	5.4	2.5	225
[136]	MZM	>50	1.4	5.4	2	128
[137]	MZM	/	1.5	6.9	2.47	100
[167]	MZM	47	1.4	5.4	2.5	305
[166]	IQ-MZM	28	1.2	5.6	2	500
[112]	MRM	50	0.52	/	0.01 ^b	128
[146]	MRM	>67	0.8	/	0.008 ^b	200
[147]	MRM	77	0.53	/	0.006 ^b	192
[154]	Push-pull MRM	42	/	14 ^a	0.015 ^b	144
[168]	MRM	>67	0.8	/	0.008 ^b	302
[169]	PDM-MRM	/	/	/	0.005 ^b	256
[145]	PDM-MRM	/	/	1	0.01 ^b	260
[161]	PhC modulator	38.6	/	/	0.016	70

^aTotal loss, including ~8 dB for grating couplers.

^bThe radius of the MRM.

strated [172–174]. An alternative approach, hybrid integration of LN film onto silicon, has also attracted considerable interest. The hybrid LN/Si material system is able to combine the scalability of silicon photonics with the excellent modulation performance of LN. A few demonstrations of hybrid Si/LN optical modulators have been reported [175,176], which rely on a supermode waveguide structure consisting of an unpatterned LN film on top of a silicon waveguide. This structure is designed to support a distributed optical mode that resides in both the LN and the underlying silicon waveguide, which means only part of the modal power overlaps with the LN region, which compromises the modulation efficiency. As the hybrid LN/Si modulators are based on the electro-optic (Pockels) effect of LN material itself, they can achieve lower insertion loss and higher linearity compared to silicon modulators with P/N doping or other highly absorptive materials. However, the electro-optic coefficient of LN is relatively low ($\gamma_{33} \approx 30$ pm/V), and thus the phase shifter length or $V_{\pi} \cdot L$ is quite a bit larger.

Hybrid LN/Si MZMs that employ two layers of hybrid integrated waveguides and vertical adiabatic couplers (VACs) have been reported (Fig. 8) [177], in which the VACs transfer the optical power fully between the silicon waveguide and LN film waveguide. The integration of LN with silicon is carried out with benzocyclobutene (BCB) bonding. The presented device exhibits an insertion loss of 2.5 dB, voltage–length product $V_{\pi} \cdot L$ of 2.2 V · cm in single-drive push–pull operation, high linearity, electro-optic bandwidth of at least 70 GHz, and modulation rates up to 112 Gb/s.

C. Hybrid Integrated Lasers

Heterogeneous integration uses a non-Si, unprocessed thin film material bonded onto a Si substrate with a coarse alignment and

then defines devices lithographically on the Si wafer scale. By eliminating the requirements of active alignments between integrated elements, the alignment tolerances are significantly reduced. In addition to the efficient volume scaling and reduced cost due to economy of scale, this technique also accommodates different materials and thus different functionalities to different areas of a Si chip, including not only III–V materials that provide gain, detection, and modulation, but also more exotic materials such as LiNbO₃ [176] and Ce:YIG [178], which promise high performance modulation, nonlinearities, and magnetic properties.

There has been a lot of progress of heterogeneous Si photonic devices and integrated circuits recently. The complexity of heterogeneous devices has rapidly grown to rival that of PICs on native substrates, with over 5000 components on a single waveguide in recent results [179]. Since the first commercial products announced in 2016, Intel's market share of Si photonics had increased to more than 50% within just two years [180]. A 23,500 h reliability test at 80°C shows that less than 10% drift of the bias current was required to maintain a constant 10 mW output power for 30 randomly chosen lasers stressed at twice the specified product operation currents [181]. Parallel to the tremendous success in commercialization, primarily in data centers and high-performance computing, R&D continues to thrive on expanding the application scenarios to quantum information processing [182], photonic neural networks [183], and sensors for life sciences, gyroscopes, LiDAR, and so on [184]. Comprehensive reviews of the state-of-the-art industrial development, scientific achievements, and future perspectives can be found in Refs. [185–191]. In what follows, we will be interested primarily in recent progress in lasers, where the synergistic relationship between the III–V and Si through heterogeneous integration gives rise to performance far exceeding what is achievable purely with III–V and Si. This will be analyzed from the perspective of the laser passive cavities and the gain materials, respectively.

In terms of the laser passive cavities, heterogeneous integration offers almost a complete suite of passive photonic devices with a versatile selection of waveguides, including not only Si and its oxide, which forms high index contrast, high-confinement waveguides ideally suited for medium to high-integration, but also extended versions of platforms based on SiN, SiON, and so on. Compared to >1 dB/cm waveguide loss in III–V waveguides, Si waveguide loss is in the decibel per centimeter (dB/cm) scale and can be reduced to as low as 0.05 dB/cm through photoresist reflow treatment, shallow etched geometry, optimized etch chemistry, and so on [192]. SiN-based waveguides have even lower waveguide loss, down to 0.001 dB/cm [193], with added benefits of a wide transparency from the visible to the infrared, a low thermo-optic coefficient, and the absence of nonlinear absorption loss.

These ultralow-loss waveguides can form high-*Q* passive cavity architectures, which not only facilitates tunable, narrow-band filtering, but also enables significant reduction in the quantum-limited white frequency noise that pushes narrowlinewidth device performance well beyond the abilities of their monolithic counterparts. For a solitary distributed feedback (DFB) laser design with an embedded spacer layer for

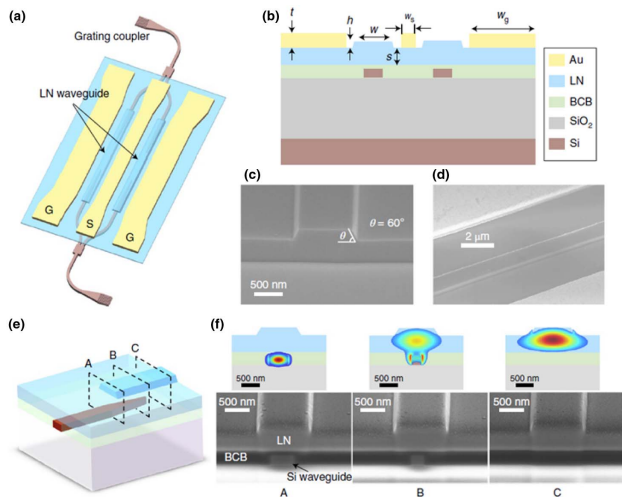


Fig. 8. Structure of the hybrid Si/LN MZM. (a) Schematic of the structure of the whole circuit; (b) schematic of the cross section of the hybrid waveguide; (c) SEM image of the cross section of the LN waveguide; (d) SEM image of the metal electrodes and the optical waveguide; (e) schematic of the VAC; (f) SEM images of the cross sections of the VAC at different positions (A, B, C) and calculated mode distributions associated with the cross sections.

spontaneous emission control [Fig. 9(a)], and a Lorentzian linewidth of ~ 1.1 kHz has been demonstrated [194]. For a coupled-triple ring structure as the back mirror [Fig. 9(b)], Lorentzian linewidth of 220 Hz was achieved with a 110 nm wide wavelength tuning [195]. For a 20 mm long on-chip SiN spiral-shaped distributed Bragg reflector (DBR) as the back mirror [Fig. 9(c)], a Lorentzian linewidth of 4 kHz was measured, with a highly thermally stable wavelength of 10.46 pm/ $^{\circ}\text{C}$, which is more than 7 times smaller than that of a typical one with Si-based mirrors [196]. Besides laser linewidth, operating wavelengths, and reliability, the output power is also a critical issue when a large number of channels are employed to boost the data capacity. For these applications, grating-based III-V/Si lasers offer excellent performance. By engineering the grating structure on the Si rib waveguide, the grating κ can be kept small to lower the grating κLg value and consequently a narrow filter bandwidth for single-mode selectivity. A maximum output power of over 20 mW can thus be obtained in a 1.2 mm long InP/Si DFB laser [186] and a maximum output power of over 30 mW can be achieved in an InP/Si extended DBR laser [197]. These versatile external cavities provided by heterogeneous integration offer different laser operations and more potential for laser performance engineering.

In terms of the gain materials, heterogeneous integration allows the versatile selection of III-V thin films with different bandgap/epitaxial structure tailored for different spectral coverage beyond the 1310 and 1550 nm telecom windows [Fig. 10(a)]. Combined with the appropriate transparent passive waveguiding materials, the shortest wavelength (900 nm) heterogeneous lasers using GaAs-based gain medium have been coupled to SiN waveguides with very high device uniformity in a wafer-scale process [198], and the longest wavelength (4.8 μm) heterogeneous lasers were demonstrated by combining a quantum cascade laser (QCL) gain medium with a special Si-on-nitride-on-insulator substrate [199]. These

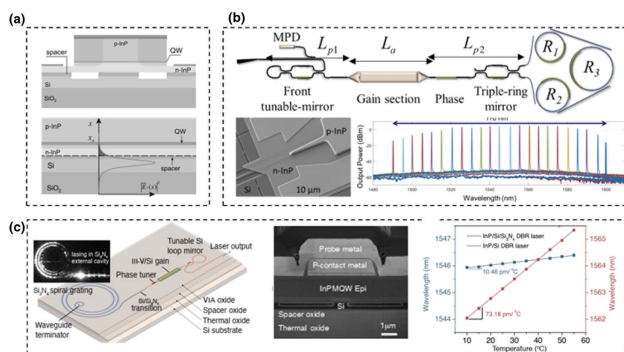


Fig. 9. (a) Cross section (upper) and transverse field profile (lower) of a heterogeneous DFB laser design with an embedded spacer layer [194]. (b) Triple-ring mirror based tunable laser [195]: schematic illustration, SEM image of a Si/III-V taper, coarse tuning spectra showing the tuning range of 110 nm. (c) III-V/Si/SiN₄ laser with SiN-based spiral [196]: schematic illustration, cross-section SEM image of the InP/Si gain, comparison of temperature-dependent wavelength shift of the III-V/Si/SiN laser and of a typical one with Si-based mirror.

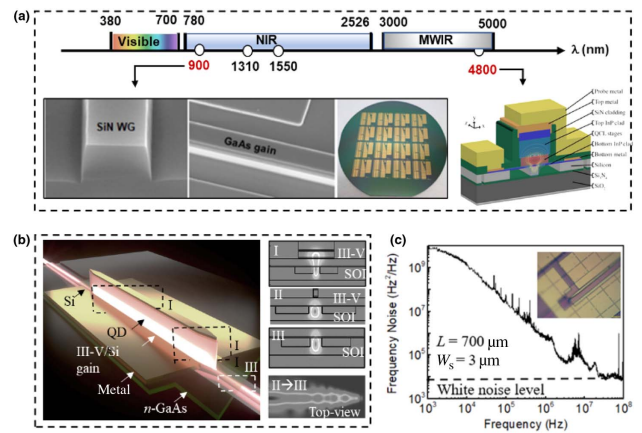


Fig. 10. (a) Heterogeneous integration allows spectral coverage beyond the 1310 and 1550 nm telecom windows, with the shortest wavelength being 900 nm [198] and the longest wavelength being 4800 nm [199]. (b) Heterogeneous QD laser: schematic image (left) and simulated cross-sectional fundamental transverse-electric (TE) mode electrical field distributions (right). (c) Frequency noise spectrum of a heterogeneous QD laser showing that Lorentzian linewidth of 26 kHz is achieved [200].

demonstrations prove that with a similar optical refractive index between the gain materials and waveguide materials, efficient evanescent coupling between the active and passive sections can be an exercise in engineering, and lessons can be leveraged for other spectrum applications. For example, InGaN-based gain materials can be integrated with TiO₂ or SiN waveguides on Si for visible applications [201], and GaSb-based interband cascade lasers (ICLs) can be combined with Ge-on-Si waveguides for mid-IR applications [202].

The versatile selection of gain materials also allows the flexible selection of optical materials for the best achievable on-chip performance. Quantum dot (QD) gain medium has multiple favorable material properties including large tolerance to material defects, reduced reflection sensitivity, nearly zero linewidth enhancement factor, low transparency current density, and high temperature operation [203–207]. Recent advances in monolithic QD lasers have spurred intense interest in transitioning the active material from quantum wells (QWs) to QDs in heterogeneous lasers as well. Device design and process optimization have been actively conducted to replace InP-based QW epitaxial material with GaAs-based QD epitaxial material [Fig. 10(b)]. Since the first demonstration in 2016 [208], great strides have been made in heterogeneous QD lasers within a short timeframe. Up to 100°C lasing in the CW mode [209], a threshold current density down to 134 A/cm² [210], a side-mode suppression ratio (SMSR) of up to 61 dB [210], a Lorentzian linewidth of 26 kHz [200], a 3 dB modulation bandwidth of 13 GHz [200], and a tuning range of 52 nm [211] have been demonstrated. It is foreseeable that heterogeneous QD lasers could quickly challenge the state-of-the-art heterogeneous QW lasers as the field matures, analogue to the evolution in monolithic lasers.

This would not only benefit the thermoelectric cooling and laser drive currents that alone themselves can make a substantial

impact on the overall energy efficiency. One particular source of interest in using QDs in the heterogeneous integration is the reduced linewidth enhancement factor (α -factor), which is a key to spectral linewidth, the modulation-induced chirp, and the sensitivity to optical injection or optical feedback [212]. With an α -factor in the range of 2–6, traditional QW DFB or DBR lasers typically have linewidths on the order of a few MHz. While this value could be narrowed down by utilizing an external cavity, which could take the form of extended grating-based external cavities, ring-resonator-based external cavities and self-injection locking with ultrahigh Q , etc., as discussed previously. The small α -factor could further lower the laser linewidth to a next level, even without the complexity of accessory device design.

By simply engineering the Si grating designs in heterogeneously integrated QD DFB lasers, a Lorentzian linewidth of 211 kHz is achieved based on a shallow etched first-order grating [210], and a Lorentzian linewidth of 26 kHz is achieved based on a first-order side-hole grating [Fig. 10(c)] [200]. These values not only surpass typical solitary QW laser linewidth of several MHz, but also significantly outperform QD DFB lasers without a Si waveguide, i.e., 480 kHz in Ref. [213] and 1.275 MHz in Ref. [214]. Since linewidth determining parameters of the loaded (external) quality factor and the α -factor can be separately optimized in heterogeneous integration, it is anticipated that a sub-100 Hz linewidth can be achieved when QD materials are coupled with a design of distributed cavity loss of 0.1 dB/cm [185]. In terms of the feedback tolerance, QD lasers exhibit over 100,000 increases in the critical feedback level compared to that of QWs, such that coherence collapse does not occur even with 90% of the light reflected back to the laser [215]. As a proof of demonstration, 25 Gb/s data-links isolator-free modulation with a metal-oxide semiconductor capacitor MRM has been achieved [210]. This isolator-free laser source eliminates the co-packaged/integrated optical isolator while still maintaining the required feedback tolerance, significantly reducing the packaging complexities and enhancing the integration density for future PIC.

Parallel to the success of heterogeneous integration, monolithic integration through direct growth of the III–V gain material onto Si substrates has been considered as a more economical favorable solution if challenges of the heteroepitaxial growth can be properly managed [203]. In addition to the continuous progress to reduce the dislocation densities as low as 10^6 cm^{-2} [216], switching from the QW active region to QDs provides an even lower barrier to entry for Si photonics through the reduced sensitivity to defects inherent in QD devices [217]. Great strides have been made in individual QD devices grown on Si with various embodiments, compact photonic crystal lasers [218], sub-millamp threshold MRR lasers [219], coupled cavity tunable lasers [213], high-channel-count mode-locked lasers [220], ultralow dark current photodetectors [221], high-gain and high-saturation output power semiconductor optical amplifiers [222], and so on. Record long lifetime has been achieved at 80°C with minimum degradation after more than 1200 h of constant current stress and an extrapolated lifetime of over 22 years [207]. Several paths have also been explored for active-passive coupling and co-integration of QD lasers to the

remaining parts of Si photonics. Using the as-grown III–V layers for the entirety of the PIC with Si serving only as a low-cost substrate is a straightforward approach. Following this direction, regrown QD DFB lasers prove a process-compatible path to spatially combine different bandgaps [223]. Alternatively, growing the III–V gain materials in pockets in a butt-coupled configuration is actively pursued by several groups and could provide the best economy of scale [224,225]. With robust on-chip laser operation and efficient low-loss light coupling to Si photonic circuits, monolithic integration on Si will be very promising for future low-cost mass production.

D. Silicon-Germanium Photodetectors

As one of the indispensable components in silicon (Si) photonics, silicon-germanium (Si-Ge) photodetectors (PDs) convert the optical signals to electrical forms. The large optical absorptivity, high carrier mobility, and the potential of low-cost and high-density integration render the Si-Ge PDs promising for large-capacity optical communications and interconnects.

High-performance Si-Ge PDs can be divided into normal-incidence and waveguide-integrated structures. The former is conducive to optical fiber or free-space optical coupling as shown in Fig. 11(a). However, the input direction of light is parallel to the carrier transit direction, making it difficult to enhance the light absorption and reduce the carrier transition at the same time, as the absorption is proportional to the Ge thickness, while the carrier transition is inversely proportional to it. Thus, waveguide-integrated PDs are introduced to break through the trade-off by uncoupling the light propagation and the photogenerated carrier collection. Two main schemes are adopted to couple the light from the Si waveguide into the Ge absorption region, including butt coupling [Fig. 11(b)] [226] and evanescent coupling [227–229]. The butt coupling directly connects the Ge region at the end of the Si waveguide. However, Si corrosion and Ge chemical mechanical polish are required with complex fabrication [230]. The evanescent coupling, with only epitaxial Ge on Si, can be distinguished as (i) bottom-up coupling [227], (ii) top-down coupling [228], and (iii) side-coupling schemes [229], as shown in Figs. 11(c)–11(e), according to the relative location of the Si and Ge. This coupling scheme is more robust by manipulating the light field distribution in the absorption region, and potential better performance can be expected.

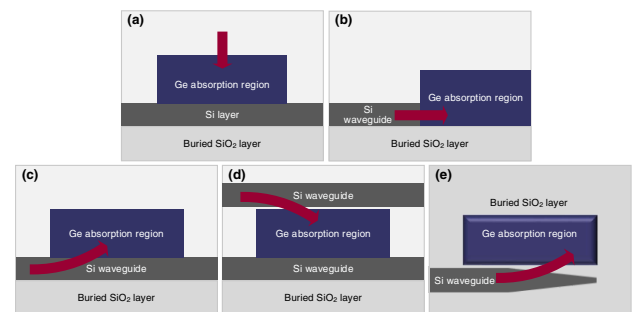


Fig. 11. (a) Normal-incidence structure; waveguide-integrated structures: (b) butt-coupling, (c) bottom-up coupling, (d) top-down coupling, (e) side-coupling (top view) schemes.

The positive-intrinsic-negative (PIN) structure is often utilized for waveguide Si-Ge PDs, consisting of an intrinsic Ge absorption region sandwiched between highly doped p-type and n-type regions. According to different doped forms, the PIN PDs can be classified into three types: (i) lateral homojunction [231], (ii) lateral heterojunction [232], and (iii) vertical heterojunction [233] as shown in Fig. 12. The homojunction PD enables bias-free operation without power consumption thanks to the continuous bandgap and strong electric field to collect most of the photogenerated carriers. However, it suffers from poor optical confinement and low responsivity, due to the weak refractive index contrast between the intrinsic and doped regions. The heterogeneous counterparts can better confine the light into the intrinsic region and enhance optical absorption.

The waveguide Si-Ge PDs with high responsivity, large bandwidth, and low dark current are highly desired. Yet this is not easy to achieve, limited by the inherent mechanism associated with material defects, structural contradictions, and fabrication complexity. For years, great efforts have been made to solve these issues comprehensively.

1. Dark Current

A low dark current is required to reduce the shot noise and improve the sensitivity for the waveguide Si-Ge PDs. Typically, it includes bulk- and surface-leakage components. The former originates from the generation of minority carriers in the depletion region and is enhanced by the threading dislocations due to the well-known 4.2% Ge/Si lattice mismatch, while the latter derives from the generation of the minority carriers in the poor passivated Ge sidewalls [234].

The bulk-leakage current is proportional to the area of the device. Pioneer works focus on the growth of high-quality Ge epitaxial films on Si to reduce the dislocation and bulk-leakage current density (BLCD), including the schemes of optimized Ge or Si-Ge buffer layer [235], thin buffer layer [236], and direct Ge growth [237]. The typical BLCDs with these methods are in the range of 1–10 mA/cm². Subsequently, selective Ge growth for filling submicrometer narrow trenches demonstrated a BLCD of 0.1 mA/cm² [238]. Osmond *et al.* achieved a record BLCD of 0.04 mA/cm² by the low-energy plasma-enhanced chemical vapor deposition (CVD) [239], approaching the BLCD limit of ~0.01 mA/cm² at room temperature.

For waveguide PDs with a small area with the order of 10 μm × 10 μm, the surface-leakage current becomes dominant. High-quality Ge interface passivation is effective to improve it, using silicon dioxide (SiO₂) [240] or amorphous Si [241] as the passivation material. Owing to the advanced fabrication and small size, the dark currents of high-performance waveguide Si-Ge PDs have been below 10 nA [242–244]. Byrd

et al. demonstrated a Si-Ge PD with a best-in-class dark current of 1.6 nA, a responsivity of 1 A/W, and a bandwidth of 40 GHz [242]. When the dark current is near nanoampere (nA) level, the main limitation of the sensitivity of a receiver becomes the noise of the transimpedance amplifier (TIA) with a typical input noise current close to 1 μA [245].

2. Responsivity

The responsivity is an indicator to evaluate the photoelectric conversion efficiency of the PD. It is related to the material footprint used to absorb the light. Typically, an order of 10 μm length is needed for sufficient absorption above 90%, realizing a high responsivity above 0.8 A/W and a large bandwidth above 20 GHz [231,246]. The deviation between the practical responsivity and the theoretical limit is mainly due to the undesired optical absorption of the metal contact [247] and the imperfect optical mode confinement in the Ge section [248]. Considering the evanescent wave coupling between Si and Ge, the optical intensity is periodically distributed at the center of the Ge along the light propagation direction. The responsivity can be enhanced by the optimized metal contact location to offset the optical intensity peaks. In this way, Frad *et al.* demonstrated a responsivity improved from 0.86 to 1.09 A/W at 1550 nm [247]. Yu *et al.* realized more uniform light distributions in the absorption region [249,250] and demonstrated 50% higher responsivity under high-power illumination [251,252]. In addition, the lateral Si-Ge-Si heterojunction was introduced to enhance the mode field confinement in Ge to achieve a high responsivity of 1.16 A/W [248]. Subsequently, this result was improved to 1.2 A/W [253]. More recently, a sufficiently wide lateral Ge PIN junction and four-port incident structure achieved a responsivity of 1.23 A/W, corresponding to a quantum efficiency of 98% [254]. However, a 17 GHz bandwidth was limited by the longer carrier transit time.

A shorter Ge length assisted by additional optical resonant structures is further used to improve the responsivity-bandwidth margin. A 5 μm long PD with an optimized distributed Bragg reflector (DBR) showed an improved responsivity from 0.61 to 0.72 A/W and an improved bandwidth from 24.8 to 31.7 GHz [255]. The DBR was also used in an avalanche photodiode (APD) to achieve a record primary responsivity of 1.25 A/W (almost 100% quantum efficiency) without compromising the bandwidth [256]. On the other hand, the waveguide loop reflector [257] and MRRs [258] have been utilized to realize the similar effect, and Chang *et al.* proposed a simple corner reflector at the edge of the Ge film instead of resonant structures on Si [259].

3. Bandwidth

The bandwidth of the PIN PD is mainly determined by the equivalent resistance-capacitance (RC) parasitic parameters and the time for the carrier transiting the depletion region. Some previous works focus on reducing the equivalent RC parameters, and the Ge area has been shrunk to reduce the junction capacitance, achieving a bandwidth of 40–50 GHz [244]. However, the responsivity degrades to 0.4–0.8 A/W. Choi *et al.* reduced the series resistance by increasing the intrinsic silicon doping concentration, thereby increasing the bandwidth from 27 to 40 GHz [260]. In addition, a peaking

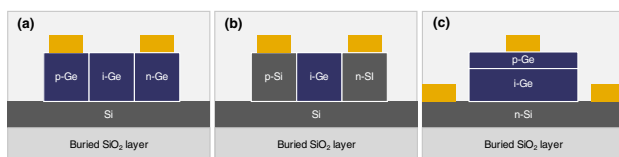


Fig. 12. (a) Lateral homojunction, (b) lateral heterojunction, (c) vertical heterojunction PIN PDs.

Table 6. State-of-the-Art Waveguide Si-Ge PIN Photodiodes^a

Reference	Type	λ (μm)	V_r (V)	I_d (nA)	R (A/W)	BW (GHz)
[242]	VPIN	1.55	1	1.6	1.0	40
[244]	VPIN	1.53	1	3	0.8	45
[231]	LPIN	1.55	1	4000	0.8	120
[262]	LPIN	1.55	1	100	1.0	70
[243]	LPIN	1.55	1	4	0.74	67
[263]	LPIN	1.55	2	200	0.3	265
				100	0.45	240
[233]	VPIN	1.55	2	3000	0.75	60
[246]	VPIN	1.55	3	61	0.85	60
[261]	VPIN	1.55	3	6.4	0.89	80
[248]	LPIN	1.55	2	8	1.16	>50
[254]	LPIN	1.55	1	4	1.23	17
[253]	LPIN	1.55	1	100	1.2	7

^a λ , wavelength; V_r , operation voltage; R , responsivity; I_d , dark current; BW, bandwidth; VPIN, vertical PIN; LPIN, lateral PIN.

inductor is introduced in the electrode to reform the RC to the RLC equivalent circuit of the detector and partly offsets the total capacitance to extend bandwidth without compromising the optical responsivity. Novack *et al.* designed the on-chip spiral inductor, extending the bandwidth from 30 to 60 GHz [233], and Yu *et al.* utilized the wire bonding to achieve an off-chip inductor with simplified design complexity and the same function [246]. Recently, the two-dimensional engineering of the parasitic parameters from both the diode and electrodes has been demonstrated to boost the bandwidth from 27 to 80 GHz [261]. In addition, a very high detectivity is achieved thanks to the high responsivity and low dark current.

Another way to increase bandwidth is to reduce the carrier transit time. Chen *et al.* enhanced the electric field of the lateral junction to eliminate the slow carrier diffusion [243]. The bandwidth increased from 20 to 67 GHz. A novel, low-loss contact scheme reduced the negative effect of diffusion to achieve a high bandwidth of 70 GHz at -1 V [262]. Vivien *et al.* reduced the intrinsic Ge width after thermal annealing for dopant drift, achieving a very high bandwidth up to 120 GHz [231]. Very recently, Lischke *et al.* demonstrated

waveguide-coupled Ge PDs with record bandwidths of 265 and 240 GHz by using 100 and 150 nm ultrathin Ge fins sandwiched between *in situ*-doped Si layers [263]. The responsivities inevitably decreased to 0.3 and 0.45 A/W, even though this work proves that the conventional Si technology can match or even outperform indium phosphide (InP) technology in terms of high-speed performance, without the need of III-V material transfer approaches. The state-of-the-art waveguide Si-Ge PIN PDs with large bandwidths, high responsivities, and low dark currents are summarized and shown in Table 6.

4. Avalanche Photodiode

APDs are used when high sensitivity is needed. The inherent gain, owing to the impact ionization effect, can break through the quantum efficiency limit of 100%. Thus, the APD has higher sensitivity compared with PIN. The Si-Ge APD combines the Ge material with a high absorption coefficient in the communication waveband and the Si material with perfect multiplication characteristics.

Typically, a vertical separate absorption charge multiplication (SACM) structure is utilized to eliminate Ge multiplication and thus reduce the effective carrier impact ionization ratio (k factor) and improve the sensitivity. However, a multiplication layer with Si epitaxy and a charge layer need to be adopted and carefully designed. Recently, the lateral SACM structure has been proposed to omit epitaxial Si [264,265], being compatible with the fabrication of conventional PIN PDs. The three-terminal structure is used to directly and independently manipulate the electric fields in the absorption and multiplication regions, without the need for a charge layer [266]. In addition, the SACM APDs usually operate at high voltages above 25 V with high power consumption. Other structures including the metal-semiconductor-metal (MSM) [267] and PIN [268] are adopted to achieve operations at 1.5–10 V.

The Si-Ge APDs with outstanding gain-bandwidth product (GBP) and sensitivities have been investigated for high-speed optical communications as shown in Table 7. In 2008, Kang *et al.* demonstrated a Si-Ge APD with a GBP of 340 GHz and a sensitivity of -28 dBm at 10^{-12} and 10 Gb/s, and it was comparable to the InP-based counterparts [269]. Subsequently, they improved this result to a record sensitivity of -30.4 dBm

Table 7. State-of-the-Art Si-Ge APDs for High-Speed Optical Communications^a

Reference	Type	λ (μm)	V_b (V)	R_p (A/W)	I_d (nA)	BW (GHz)	GBP (GHz)	BR (Gb/s)	S at BER (dBm)
[269]	VSACM	1.31	25	0.55	1.24	11.5	340	10	-28 at 10^{-12}
[267]	MSM	1.31	3.5	0.4	—	39.5	300	10	-13.9 at 10^{-9}
[270]	VSACM	1.55	23	0.81	3	29.5	—	10	-30.4 at 10^{-12}
[268]	LPIN	1.55	7	0.4	20	11	190	10	-26 at 10^{-7}
[271]	VSACM	1.55	10	0.75	0.44	23	276	25	-16 at 10^{-12}
[272]	VSACM	1.31	18	0.7	0.4	26	—	25	-22.5 at 10^{-12}
[273]	VSACM	1.55	26.5	0.35	1	30	460	40	-13.9 at 10^{-12}
[266]	VSAM	1.55	6	0.48	1	18.9	284	25	-11.4 at 10^{-4}
[274]	VSACM	1.31	12	0.21	2	26	150	50	-16 at 10^{-4}
[275]	VPIN	—	4.2	—	—	40	—	112	-8 at 10^{-4}
[264]	LSACM	1.31	12	0.65	30	27	300	50	-18.6 at 10^{-4}
[5]	LPIN	1.55	12.5	0.95	10	33	240	64	-9.2 at 10^{-6}
[276]	VSACM	1.31	19.6	0.55	0.5	28	180	106	-16.8 at 10^{-4}

^a λ , wavelength; V_b , breakdown voltage; R_p , primary responsivity; I_d , dark current; BW, bandwidth; GBP, gain-bandwidth product; BR, bit rate; S, sensitivity; BER, bit error rate; VSACM, vertical SACM; MSM, metal-semiconductor-metal; LPIN, lateral PIN; VPIN, vertical PIN; LSACM, lateral SACM.

[270]. The sensitivity of a 25 Gb/s APD reached -23.5 dBm at 1310 nm [245]. Kim *et al.* demonstrated a receiver with vertically illuminated Si-Ge APD, assisted by a negative conductance effect for high-speed operation with high gain [273]. The GBP of the device reached 460 GHz, and the device sensitivities varied from -19 to -14 dBm at 10^{-12} for 28 and 40 Gb/s signal reception, respectively. A lateral SACM APD with a GBP of 300 GHz supports 56 Gb/s signal, with a sensitivity of -18.6 dBm at 10^{-4} [264]. Recently, the Si-Ge APDs have been investigated by using four-level pulse amplitude modulation (PAM-4) to achieve 100 Gb/s [275,276]. Pan *et al.* achieved a 106 Gb/s (53 Gbaud PAM-4) Si-Ge APD with a record sensitivity of -16.8 dBm [276].

3. HIGH-CAPACITY SILICON PHOTONIC TRANSCIVERS

Silicon PICs can manipulate the light in silicon, which contains the generation, modulation, routing, processing, and detection. As an enabling technology, the application of silicon photonics in transceiver datacom and telecom is very successful [277,278].

In short distance data center communications, the requirements to silicon photonics module are low cost, high volume, energy efficiency, and frequency upgrading. The research and development of 100G (4×25 Gb/s) pluggable transceivers have been initiated at Intel since 2010. After about six years' efforts, Intel paves the way for silicon photonics with first in the world shipping products [279], which are the 100G parallel single mode fiber 4-lane (PSM-4) and 100G coarse wavelength division multiplexing 4-lane (CWDM-4)}. The 100G CWDM-4 QFSP28 transceiver offers a solution up to 10 km as shown in Fig. 13. It includes two independent blocks, and each one has several dies. At transmitter (Tx) side, by bonding on silicon photonics die in a flip-chip configuration, it integrates four InP-based lasers and CMOS die chiplets. The key silicon photonics die is an MZM that encodes high-speed optical signals. And the data are processed by employing a four-channel 25G optical clock and data recovery (CDR) component from MACOM. At the receiver (Rx) side, it is realized by four high-performance germanium (Ge)-based photodetector dies and a TIA. The 100G silicon photonics module shows Intel's huge potential in terms of packaging and photonics.

In 2017, the IEEE standardized the 400GBase (4×100 Gb/s) Ethernet specifications where PAM-4 has been selected as the modulation format for the single-mode fiber (SMF) optical links. Two years later, the 400 Gb/s O-band silicon photonic chip for intra-data-center optical interconnects was demonstrated by Plant and co-authors [280]. Four parallel silicon photonic traveling wave MZMs are employed at the Tx

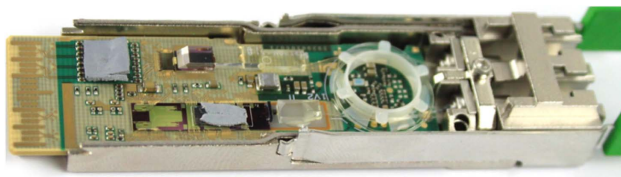


Fig. 13. 100G CWDM-4 QFSP28 transceiver module of Intel.

side with 53 Gbaud PAM-4 for each lane. However, the silicon photonic chip is not integrated or packaged with laser and driver and so on.

At the *Optical Fiber Communications Conference (OFC 2020)*, a 400G DR4 silicon photonics Tx integrated with four heterogeneously integrated DFB lasers was demonstrated by Intel [281] as shown in Fig. 14. The module fulfills the lifetime and reliability requirements for 400G DR4 data center 2 km applications over a temperature range of 0°C – 70°C . There is also another 400G silicon photonic transmitter for specific applications [282–285]. For the next generation of data center applications, the 800G interface is a feasible and competitive solution. By using a silicon photonic transmitter in which the four-channel traveling wave MZM chip is co-packaged with a four-channel driver chip [286], an 800G (4×200 G) PAM-4 optical signal transmission over 1 km SMF is demonstrated with DSP as shown in Fig. 15.

A 1.6 Tb/s silicon photonics fully integrated Tx that contains on-die all the spot size converters (SSCs), V-grooves, monitor photodetectors, MRMs, and lasers is demonstrated. To enable 800G photonic engine (PE), the fully integrated Tx is combined with discrete silicon photonics Rx. Though well designed, the PE can support 16 modules to be co-packaged around a high-bandwidth switch ASIC [287] as shown in

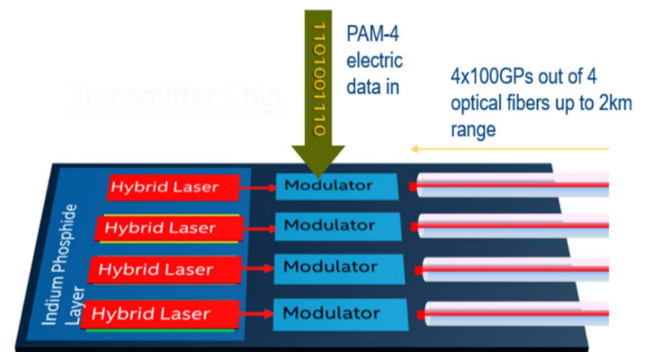


Fig. 14. 400G DR4 transmitter with 4×100 Gb/s data paths of Intel.

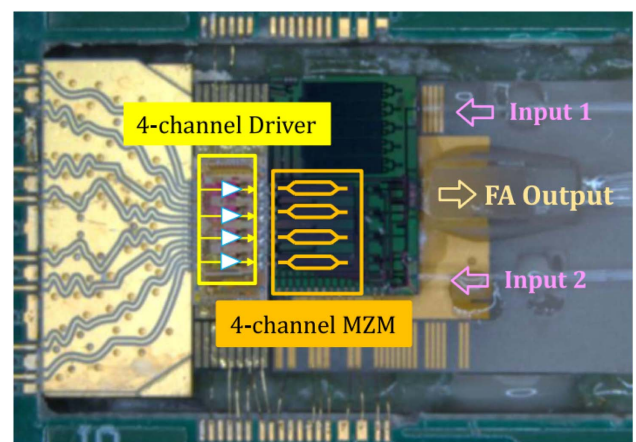


Fig. 15. Chip-on-board 800G silicon photonics transmitter.

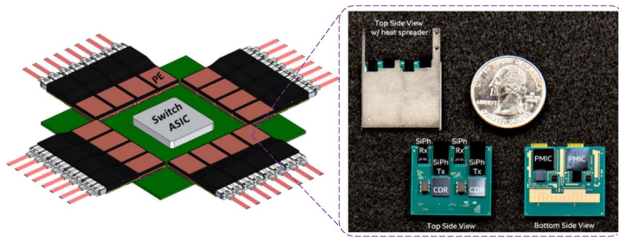


Fig. 16. Integrated copackaged optical IO switch package with 16 photonic engines (PEs).

Fig. 16. Ayar Labs reported an error-free 1 Tb/s WDM optical I/O chiplet that features 4.96–5.56 pJ/bit (Tx + Rx) optical energy efficiency [288].

In metro, long-haul, and subsea communications, the requirements for silicon photonics modules are low volume, high performance, and long life span. In 2021, Acacia Communications unveiled the industry's first 1.2T faceplate pluggable coherent solution, which is called coherent interconnect module 8 (CIM 8) [289]. The CIM 8 combines the 5 nm CMOS Jannu DSP with advanced 3D siliconization packaging technology that contains the silicon photonics integrated circuit, driver, and TIA in a single opto-electronic package. Based on a silicon photonics IQ modulator, a dual-polarization 100 Gbaud 32QAM (1 Tb/s) is achieved [165]. It is the highest reported net rate of 833 Gb/s in a silicon photonics IQ modulator. Further, with the segmented design of the silicon photonics IQ modulator, it can operate beyond 100 Gbaud [166,170,290–292]. A line rate of 600 Gb/s (net 480 Gb/s) on a single polarization is also realized [290]. The NTT Corporation presented a silicon photonics coherent optical sub-assembly with EO and OE bandwidths of over 50 GHz for digital coherent optical systems [293,294]. It supports dual-polarization 96 Gbaud 16QAM (768 Gb/s) signal generation and detection.

The monolithic integration of photonic and electronic circuits could enable the scalability and complexity simultaneously for electronic-photonic systems and accelerate the realization of overall “systems on a chip.” In 2015, a system-on-a-chip integrating over 70 million electronic transistors and 850 photonic components that work together to provide logic, memory, and interconnect functions was first reported by Sun and co-authors [295]. The realized microprocessor system on chip utilizes the photonic devices to directly communicate with other chips by light. The chips are fabricated in IBM's commercial 45 nm thin buried-oxide SOI process with “zero change.” In 2018, the group from US Massachusetts Institute of Technology (MIT) and cooperators demonstrated a large-scale monolithic electronic-photonic system based on a 65 nm transistor bulk CMOS process technology [296] as shown in Fig. 17. It integrated fully functional (except laser) photonic components such as optical waveguides, microring modulators, grating couplers, and APDs into a CMOS chip containing analog and digital electronics through the addition of a few extra processing steps in a 300 mm diameter wafer microelectronics foundry. There were two biggest challenges for this electronic-photonic integration chip: the first is to find

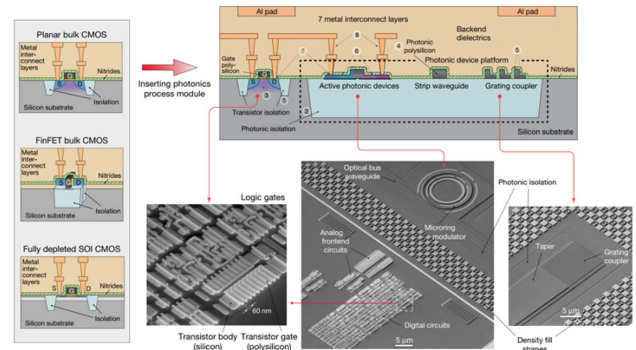


Fig. 17. Monolithic electronic-photonic systems based on a 65 nm transistor bulk CMOS process technology [296].

a processing recipe for the polysilicon film (220 nm) so that it had both good optical and electrical properties, and the second is to incur minimum changes to the CMOS process to avoid any degradation to the nanoscale transistors on the chips. Overall, the advances in silicon photonics integrated circuits are delivering chips that can densely pack photonics and electronics together.

A silicon photonics module has been successfully applied in transceiver datacom and telecom with high capacity. To further increase the bandwidth and speed and decrease power consumption and cost, the advanced packaging is strongly demanded. It is important to develop a cost-effective PIC and electronic IC (EIC) packaging platform to realize high-data-rate transmission. As the density and speed of optical links have increased dramatically, the paradigm of front panel pluggables has shown to have many drawbacks. The integration and packaging technology must support the scaling of the number of the optical channel and provide a high-speed electrical interconnect between the PIC and EIC of each channel. Thus, PICs are evolving from pluggable transceivers at the periphery of the board to co-packaged optics and electronics. The “3D integration” methods, which are widely employed in CMOS processes, enable new optoelectronic integration architectures and better signal transmission [179]. The monolithic integration of silicon-based photonic (including the laser) and electronic circuits will allow for the scalability and complexity simultaneously for electronic-photonic systems and accelerate the realization of overall “systems on a chip.” The key of monolithic integration is the process’ “sweet-spot” for photonic and electronic circuits.

4. HIGH-CAPACITY SILICON PHOTONIC NETWORKS ON CHIP

The photonic network on chip (NoC) has drawn tremendous attention due to its potential to route signals and allocate light paths with substantial flexibility and scalability, which makes it possible to meet the harsh bandwidth and power-efficiency requirements for on-chip and inter-chip communications [297]. In general, the network fabric can be organized by assembling a large number of switching units as an array, and thereby it is vital to ensure compact footprints, high tuning efficiencies, and fast switching responses in each switching unit. The

SOI waveguide can provide subwavelength modal areas, strong thermo-optical (TO) tunability, and sub-nanosecond electro-optical (EO) responses with free-carrier plasma-dispersion effect [2]. These outstanding characteristics have triggered a blooming proliferation of NoCs on silicon. Nevertheless, it still remains a prime issue as how to further expand the network capacity given that the scaling up of the switch array will exponentially increase the total power consumption and difficulties in controlling each switching unit. Besides, it is also challenging to make NoCs compatible with signals carried by different wavelengths or eigenmodes in order to multiply the capacity by utilizing wavelength/mode-division multiplexing technologies (i.e., WDM and MDM). Moreover, the efficient traffic of dense data streams in NoCs relies on the advanced topology of switch fabric, and thus it is essential to develop a new generation of NoCs on the basis of a smarter and multifunctional infrastructure. In this section, we will briefly review three typical classes of networks, i.e., single-mode, multimode, and ring-bus NoCs, and discuss how the capacity conundrum can be properly addressed for these schemes.

A. Single-Mode NoCs

The most commonly used NoCs are operated at a single-mode state, which can be attained by employing tunable MRR or MZS arrays as shown in the first column of Fig. 18. For MRR, the resonant wavelength can be thermally or electrically detuned from the incident one, which results in the low-power switching from bar state to cross state [298]. Thus, the crossbar fabric can be formed by arraying MRR in a rectangular grid as shown in Fig. 18(a), where each input signal can be routed toward any dropping port by selecting the corresponding MRR

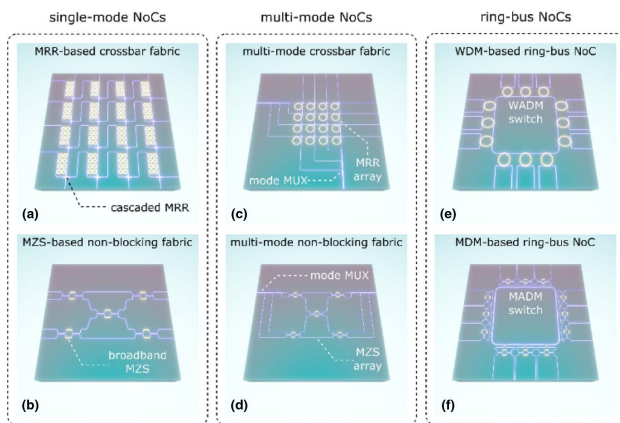


Fig. 18. Schematic configurations for single-mode networks (first column), multimode networks (second column), and ring-bus networks (third column). (a), (b) The single-mode carriers can be arbitrarily routed by leveraging MRR or Mach-Zehnder switch (MZS) arrays. (c), (d) For multimode operations, the fabrics can be constructed by assembling mode MUXs and a single-mode NoC. (e), (f) The ring-bus NoCs support multiple carriers transferring in a single ring-like bus waveguide, which can be realized by utilizing WDM or MDM technologies. NoC, network on chip; MRR, micro-ring resonator; MZS, Mach-Zehnder switch; MUX, (de)multiplexer; WDM, wavelength-division multiplexing; MDM, mode-division multiplexing; WADM, wavelength add-drop (de)multiplexer; MADM, mode add-drop (de)multiplexer.

element. The MRR array can also be organized based on a more complex configuration (e.g., serpentine fabric) to achieve the spatial non-blocking with a higher level of flexibility. The first demonstration of MRR-based silicon NoC was reported by the joint team from Columbia and Cornell [299] as shown in Fig. 19(a). The hitless routing of multiple light paths was implemented via harnessing eight MRRs arranged in a serpentine manner, whereby 4×4 input/output ports were interfaced with low cross talk (< -20 dB). Over the past years, great effort has been put into improving the performances of MRR-based NoCs [301,302] and also merging them into larger-scale networks [303,304]. Despite being compact and power efficient, MRRs suffer from two major drawbacks. First, the resonant wavelength of MRR is highly sensitive to fabrication errors (e.g., width and height deviations). Such inevitable wavelength drifts lead to the poor yielding in wafer-scale productions, which hampers the practical use of MRR-based NoCs. To tackle this problem, one approach is to lock the resonant wavelength by introducing the feedback mechanism [305–307]. As an alternative, the nonuniformity can also be depressed by exploiting the higher-order MRR filters with box-like transmission responses [308–311]. Secondly, the narrow bandwidth of MRR can contain only few wavelength channels, thereby hindering the link capacity in WDM systems. This obstacle can be solved by sequentially cascading several MRRs at the crossbar node [see also Fig. 18(a)], where each MRR is able to handle a single wavelength carrier. Such a WDM-compatible scheme can be found in some early studies that lack of experimental or systematic demonstrations [312,313]. Recently, Khope *et al.* reported the first practical wavelength-selective NoC that supports 111 Gb/s data streams with four wavelength channels over 4×4 MRR-based crossbar nodes [314,315], showcasing a large capacity and significant scalability.

The MZS is another promising candidate for building high-performance NoCs. Over the recent years, the integrative performance of on-chip silicon MZS has been pushed to an unprecedented level in terms of its bandwidth, extinction ratio, and error tolerance. In contrast to MRR, the working bandwidth of MZS is intrinsically large yet is still restricted by the coupling-ratio dispersion of 3 dB couplers. The MMI coupler is capable of working over a large wavelength range [316], but its relatively high insertion loss will be overwhelmingly accumulated in an array. One possible solution was proposed in Ref. [317]. In this work, the dispersion-engineered bent directional couplers (BDCs) were utilized to eliminate the wavelength dependence of MZS, leading to an ultrabroad

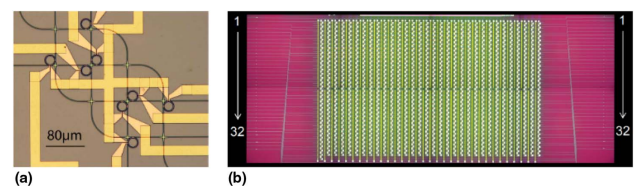


Fig. 19. (a) The single-mode NoC based on MRR array [299], under Creative Commons license CC BY. (b) The single-mode NoC based on MZS array [300], under Creative Commons license CC BY. NoC, network on chip; MRR, micro-ring resonator; MZS, Mach-Zehnder switch.

working bandwidth (>140 nm). The high extinction ratio is another desired attribute in MZS. In theory, the extinction ratio can be infinite if the coupling ratio is precisely 50:50 as the phase tuning of π is perfectly reached. However, the inevitable coupling-ratio deviations will impair the interference and degrade the extinction ratio. This hurdle can be overcome by introducing the two-stage scheme [318–320]. The idea is to use a pair of successive phase-shifting stages to tailor the wavefront, so that the perfect switching operation with ultrahigh extinction ratios (>50 dB) can be promised even with imperfect 3 dB couplers [318]. Another concern is that the fabrication nonuniformity of phase-shifting arms will induce a slight phase drift that deteriorates the constructive interference at the off state. As a result, it is necessary to apply a phase bias onto each MZS element to compensate for the phase drift, which gives rise to the power consumption. This issue can be addressed by exploiting multimode waveguides instead of single-mode waveguides as phase shifters since the width sensitivity can be dramatically relaxed with a larger waveguide dimension [321]. The nonblocking routing can be then achieved by deploying an array of MZSs with crossbar, Clos, Spanke, Beneš, and Spanke-Beneš configurations [see also Fig. 18(b)]. Detailed discussions about these architectures can be found in previous studies on fiber-optical networks [322]. The rapid progress of silicon photonic foundry enables the monolithic integration of a great number of MZS elements and the cointegration of photonic devices with electric-driving circuits. In 2010, Yang *et al.* reported the first MZS-based silicon NoC using a 4×4 serpentine fabric [323] as shown in Fig. 19(b). The first demonstration of large-scale nonblocking routing in MZS-based silicon NoC can be found in Ref. [251]. Totally, 1024 TO MZSs were integrated on a single die within a small area ($11 \text{ mm} \times 25 \text{ mm}$). The NoC chip was packaged with a printed circuit board (PCB) through a land grid array (LGA) interposer. Thus, 32×32 reconfigurable light paths can be arbitrarily built up with low cross talk (<-20 dB). Some other studies also focus on improving the power efficiency and response time by introducing the direct-heating [324] and EO-driven [325] phase shifters into MZSs.

B. Multimode NoCs

From the above discussions, we stress the importance of NoCs working at single-mode for nonblocking routing purposes since they are footstones for advanced NoCs working with a higher degree of freedom and more sophisticated functionalities. The drive toward power- and cost-efficient optical communications has led to the emerging of MDM technology for expanding the link capacity within a single-wavelength carrier [326,327]. It should be noted that MDM signals also need to be routed, added, and dropped directly in the optical domain. Therefore, the situation has arisen where the multimode NoC is required to dynamically manipulate mode carriers. The difference between single- and multimode NoCs is that, for single-mode NoCs, the routing operation happens between distinct input/output waveguides, whereas for multimode NoCs, the signal is usually reloaded onto a different mode carrier to regenerate the signal-carrier mapping. Over the recent years, there has been a wide scope of reported devices targeting reconfigurable multimode handling, including the ones based

on Y branches [328–330], MRRs [84,331–333], and MZSs [334–337]. However, most of them can only be used to realize simple mode exchange or add-drop, and thereby it is more reasonable to categorize this class of devices as “multimode switches” rather than “multimode NoCs”. Basically, a multimode NoC can be created by assembling mode (de)multiplexers (MUXs) with a single-mode NoC, as shown in the second column of Fig. 18. Based on this scheme, higher-order modes can be extracted into a series of single-mode waveguides and processed in the single-mode realm, and then multiplexed into another multimode bus waveguide with signal-carrier relation updated. One widely applied configuration is a combination of mode MUXs with an MRR-based crossbar fabric as shown in Fig. 18(c). This type of multimode NoC was first demonstrated by Sun *et al.* in 2018 [338] as shown in Fig. 20(a). Afterward, a very similar design was also reported by the same team [340]. In these works, 2×2 inter-path routing and inter-modal exchange were present as a proof of concept, showcasing the potential for multipurpose mode handling. Moreover, it is also feasible to realize the simultaneous routing of WDM and MDM signals by inserting more MRRs into the crossbar node [341]. Another mainstream use is to use MZS to build multimode NoCs [see Fig. 18(d)], taking advantage of its broadband property and compatibility with WDM. In 2018, Yang *et al.* proposed and demonstrated the general architecture for MZS-based multimode NoC, which consists of two groups of mode MUXs connected to a nonblocking MZS array in between [339,342] as shown in Fig. 20(b). The experimental results show that the 2×4 inter-path and inter-modal routing can be obtained with low cross talk (<-15.3 dB) over a broad wavelength span (>40 nm). Furthermore, recent research also shows that both wavelength and mode selectivity can be achieved in a single NoC by merging MRRs into the MZS array as a full system [343,344].

C. Ring-Bus NoCs

For the majority of the reported NoCs, the switch array is organized in a rectangular grid or a layered infrastructure as discussed above. However, functionalities provided by these conventional fabrics are basically limited to routing and add-drop. For a practical NoC, a lot more features (e.g., self-configuring, broadcasting, hubbed connection, and duplex link) are demanded to manage light paths and ensure survivability over a large capacity. This bottleneck can be broken only by introducing a more advanced infrastructure beyond conventional fabrics. One emerging trend is to use the ring-bus NoC, which is composed of numerous nodes that are bridged by a

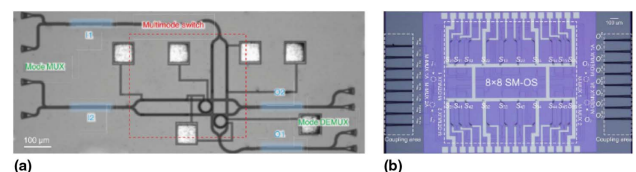


Fig. 20. (a) The multimode NoC based on MRR array [338], under Creative Commons license CC BY. (b) The multimode NoC based on MZS array [339], under Creative Commons license CC BY. NoC, network on chip; MRR, micro-ring resonator; MZS, Mach-Zehnder switch.

feeding ring, as shown in the third column of Fig. 18. For such a scheme, all the light paths run parallel within a single ring-like bus, and thus the data-transmission topology can be vastly diversified since signals can be arbitrarily accessed and controlled by all the nodes. Additionally, each pair of nodes is linked by two semi-rings, thereby enabling duplex communications without circulators. It should be noted that all the light paths in a ring-bus NoC are inevitably overlapped, since there is only one available bus. Consequently, it is essential to use multiplexing technologies (i.e., WDM and MDM) to ensure the parallelism for each independent light path. As a result, each node is actually a wavelength or mode add-drop multiplexing switch (i.e., WADM or MADM switch) as shown in the third column of Fig. 18, which raises the technical difficulty in building a practical ring-bus NoC. In 2016, Zhang *et al.* reported the first breakthrough in this field [345] as shown in Fig. 21(a). The broadband MZS was adopted to add-drop eight-channel WDM signals that propagate in the bus, while the wavelength (de)multiplexing was implemented at eight nodes by leveraging AWGs. An extra node was also inserted into the bus to enable chip-fiber interconnections. Moreover, low-threshold DFB lasers, high-speed electro-absorption modulators (EAMs), semiconductor optical amplifiers (SOAs), and PDs were all packed on the same chip through heterogeneous integrations. In this way, an aggregate link capacity up to $8 \times 8 \times 40$ Gb/s was realized for both intra- and inter-chip communications. Nevertheless, this WDM-based scheme requires quite a number of laser diodes, each working at a different wavelength. A more cost-effective approach is to use MDM to substitute WDM, so that light paths can be conveyed by different eigenmodes within a shared wavelength channel. The first demonstration of MDM-based ring-bus NoC was reported very recently [346] as shown in Fig. 21(b). The “direct-access” MADM was proposed to realize the hitless add-drop of any selected eigenmode without demultiplexing other idle carriers. One hub node and three accessing nodes were connected by a multimode waveguide in order to realize a multi-point-to-point (MP2P) data traffic, based on which, several different network states were present with a large link capacity of $3 \times 3 \times 10$ Gb/s in a duplex manner. In this work, the wavelength/mode-hybrid add-drop was also demonstrated by combining an MRR array with MADM switches. Hence, it is possible to further boost the link capacity by introducing the WDM-MDM hybrid mechanism.

Several key improvements could facilitate the practical use of large-capacity NoCs. First, the power efficiency of switching

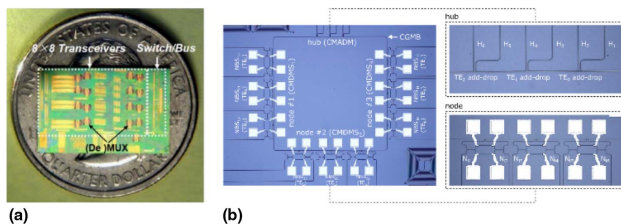


Fig. 21. (a) The ring-bus NoC based on WDM [345], under Creative Commons license CC BY. (b) The bus-ring NoC based on MDM [346], under Creative Commons license CC BY. NoC, network on chip; WDM, wavelength-division multiplexing; MDM, mode-division multiplexing.

unit in NoCs needs to be minimized. One possible solution is to seek alternative mechanisms beyond the conventional TO or EO switching. Micro-electro-mechanical systems (MEMS) could offer opportunities for power-efficient NoCs. The switching operation for MEMS switch is realized by moving waveguides via electrostatic actuations, whose power consumption can be nearly zero. Some recent works have proven that MEMS switches can provide ultrahigh extinction ratios (>70 dB), fast switching responses (<50 ns), broad bandwidths (>100 nm), low actuation voltages (<2 V), and an ultralarge integration scale ($>240 \times 240$) [347–353]. Second, the further scaling up of the switch array is constrained by the maximum die size and propagation losses over a long routing path. This issue can be addressed by using the multimode waveguide since it is able to reduce the scattering losses induced by sidewall roughness and misalignment between adjacent rectangles [354], ensuring the wafer-scale seamless integration. Third, it is still a big challenge to manipulate multimode carriers in an NoC. So far, most reported multimode NoCs can only process signals in the single-mode realm, and thus it is necessary to cascade mode MUXs at two ends, which increases the device size and system complexity. The system can be significantly simplified if higher-order modes can be directly handled without demultiplexing. This scheme could be realized by using phase-change materials due to the ultralarge index variation range [355–360].

5. CONCLUSION

Silicon photonics provides an excellent platform to scale the complexity of integrated transceiver systems. All the required components including the laser source, modulators, photodetectors, and the passive devices [e.g., wavelength and mode (de)multiplexers, splitters/combiners, couplers, polarization manipulating devices] can be integrated on silicon chips, either monolithically or in a hybrid manner. The transmission capacity can be scaled in various dimensions. The single channel transmission rate can be improved by using large-bandwidth modulators and photodetectors. Furthermore, coherent detection with higher-order modulation formats, such as quadrature phase-shift keying (QPSK) and higher-order quadrature amplitude modulation (QAM) can be utilized to improve the single carrier transmission rate. More channels can be achieved by extending the wavelength-division multiplexing band from the traditional C band (1530–1565 nm) to C + L bands (1530–1625 nm). New multiplexing technologies such as mode division multiplexing and polarization-division multiplexing have been introduced to further improve the transmission capacity. Large-scale integration of photonic functions on a silicon platform provides a promising solution to resolve the dilemma of scaling system complexity while reducing the size, energy, and cost.

Funding. National Key Research and Development Program of China (2019YFB2203603); “Pioneer” and “Leading Goose” R & D Program of Zhejiang (2022C01103); National Natural Science Foundation of China (61922070, 6213000026); Fundamental Research Funds for the Central Universities.

Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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