

Ultralow-loss compact silicon photonic waveguide spirals and delay lines

SHIHAN HONG,¹  LONG ZHANG,¹ YI WANG,¹ MING ZHANG,¹ YIWEI XIE,¹ AND DAOXIN DAI^{1,2,*}

¹State Key Laboratory for Modern Optical Instrumentation, Center for Optical & Electromagnetic Research, College of Optical Science and Engineering, International Research Center for Advanced Photonics, Zhejiang University, Zijingang Campus, Hangzhou 310058, China

²Ningbo Research Institute, Zhejiang University, Ningbo 315100, China

*Corresponding author: dx dai@zju.edu.cn

Received 15 July 2021; revised 22 October 2021; accepted 25 October 2021; posted 26 October 2021 (Doc. ID 437726); published 9 December 2021

Low-loss and compact optical waveguides are key for realizing various photonic integrated circuits with long on-chip delay lines, such as tunable optical delay lines, optical coherence tomography, and optical gyroscopes. In this paper, a low-loss and compact silicon photonic waveguide spiral is proposed by introducing broadened Archimedean spiral waveguides with a tapered Euler S-bend. A 100-cm-long waveguide spiral is realized with a minimal bending radius as small as 10 μm by using a standard 220-nm-thick silicon-on-insulator foundry process, and the measured propagation loss is as low as 0.28 dB/cm. Furthermore, the present waveguide spirals are used to realize a 10-bit tunable optical delay line, which has a footprint as small as 2.2 mm \times 5.9 mm and a dynamic range of 5120 ps with a fine resolution of 10 ps. © 2021 Chinese Laser Press

<https://doi.org/10.1364/PRJ.437726>

1. INTRODUCTION

Loss reduction is considered as the most fundamental and critical priority in the development of on-chip photonic integrated circuits (PICs), and tremendous efforts have been made to develop ultralow-loss optical waveguides in the past decades. Many PICs used for true-time-delay lines [1–6], optical gyroscopes [7,8], optical coherence tomography [9,10], and microwave photonics beam-forming [11,12] often require very long on-chip waveguides, and hence various low-loss optical waveguides have been demonstrated on different platforms such as Si_3N_4 [2,10], SiO_2 [13,14], and silicon [4,15–20]. Though Si_3N_4 and SiO_2 optical waveguides exhibit low losses down to ~ 1 dB/m [2] and ~ 0.1 dB/m [14], their bending radii usually have to be as large as hundreds of micrometers or even millimeters, which prevents the realization of on-chip high integration density. In contrast, by taking advantage of the complementary metal–oxide semiconductor (CMOS) compatibility as well as high index-contrast Δn between the silicon core and silica cladding, silicon-on-insulator (SOI) nanophotonic waveguides have very strong optical field confinement to have microscale bending radii, which is gaining intensive interest for enabling ultra-compact photonic integrated devices and circuits [21–23]. On the other hand, however, the enhancement of light confinement strongly increases the interaction between the optical modal field and the rough etched sidewalls [24]. This might introduce a high scattering loss, which is proportional to $(\Delta n)^3$ [15,25].

Basically speaking, currently there are two typical methods to reduce the scattering losses in optical waveguides. One is to smoothen the waveguide sidewalls (characterized by the mean square deviation σ^2 of the sidewall roughness) by improving the fabrication processes or introducing some specific processes, such as an oxidation-based etchless process [16], chemical oxidation [17], anisotropic etching [15], and post-processing [18,19]. For instance, an etchless process based on selective thermal oxidation was developed to fabricate a silicon photonic waveguide with a low loss of 0.3 dB/cm [16]. However, these specific processes are usually incompatible with the multi-project-wafer (MPW) foundry for silicon photonics, and thus they are not easy to use for further photonic integration. The other one is to decrease the interaction of the optical modal field with the rough sidewalls by introducing a shallowly etched ridge or ultrathin core region [4,20]. For example, a shallowly etched SOI ridge waveguide with a cross section of 0.25 $\mu\text{m} \times 2 \mu\text{m}$ and an etching depth of 50 nm was employed, and the propagation loss was about 0.274 dB/cm [20]. Later, an ultrathin silicon photonic waveguide with a 60-nm-thick core region was also demonstrated with a reduced propagation loss of 0.61 dB/cm [4]. As it might be noticed, these silicon photonic waveguides are not compatible with standard 220-nm-thick silicon strip waveguides. Furthermore, since their mode confinement becomes very weak, the bending radii are required to be as large as several tens [4] or hundreds [20] of micrometers, while the decoupling separation between adjacent

waveguides is also pretty large. The large bending radius requires a sufficient footprint, and as a result, the compactness of the delay lines is realized with difficulty [2,10,13,14,20]. To minimize the footprints of waveguide spirals, one should reduce the gap W_g between adjacent waveguides as well as the radius of the S-bend in the middle. As a result, it is still challenging to achieve long delay lines with low losses, high compactness, and broad bandwidths by using 220-nm-thick silicon strip waveguides.

In this paper, we propose and realize an ultralow-loss and ultra-compact 220-nm-thick silicon strip waveguide spiral fabricated with standard MPW processes. Here the silicon strip waveguide is designed with a broadened core region beyond the single-mode regime. In this way, the field amplitude at the sidewalls can be reduced significantly, and thus the scattering loss is reduced greatly. Particularly, to be compact with negligible losses as well as high-order mode excitation, a tapered Euler-curve S-bend is introduced for the waveguide spiral. With such low-loss and compact waveguide spirals, a 10-bit tunable optical true-time-delay line on silicon is realized with a time delay as long as 5120 ps for the first time.

2. STRUCTURE AND DESIGN

Figure 1(a) shows the configuration of the proposed silicon photonic waveguide spiral, which consists of single-mode input/output waveguides, two bent waveguide tapers, two multimode Archimedean spiral waveguides, and a tapered Euler-curve S-bend in the middle. The bent waveguide tapers should be long enough to adiabatically connect the narrow input/output waveguide and the broadened Archimedean spiral waveguide, so that the fundamental-mode loss and the higher-order mode excitation ratio is negligible. Usually, the length of the bent waveguide tapers is chosen as $R\pi/2$, where R is the maximal bending radius of the Archimedean spiral. The Archimedean spiral presents a gradually varied bend radius and uniform gap widths. This makes the Archimedean spiral very attractive to achieve adiabatic light propagation of the fundamental mode in a multimode waveguide without any higher-order mode excitation even when the radius is gradually reduced to be small. In contrast, waveguide spirals with normal circular bend usually require large bending radii to overcome the mode mismatch at the junction between the circular bends with different radii. For this tapered Euler-curve S-bend, the curvature radius is varied gradually from the maximum R_{\max} to the minimum R_{\min} and back to R_{\max} , while the core width

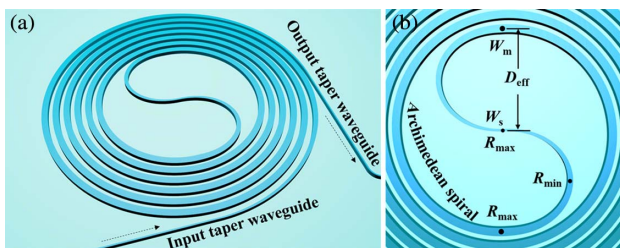


Fig. 1. (a) 3D view of the proposed ultralow-loss and compact silicon photonic waveguide spiral. (b) Enlarged view of tapered Euler-curve S-bend in the middle.

is varied gradually from the maximum W_m to the minimum W_s , as shown in Fig. 1(b). In this way, the transition loss and the intermode cross talk introduced by the junction in the middle of the S-bend can be minimized possibly even when the maximal bending radius R_{\max} is not very large.

To evaluate the loss due to the scattering at the waveguide interfaces, which is the major loss source, a three-dimensional volume current method was used for modeling [26–28]. In this way, the scattering is modeled as an equivalent polarization volume current density. Figures 2(a)–2(c) show the calculated losses due to the top/bottom surface scattering and sidewall scattering, as well as the total scattering loss, respectively. Apparently, the scattering loss decreases greatly as the roughness σ is reduced. One should note that the sidewall roughness is limited by the fabrication processes, while the top/bottom surface roughness is determined by the SOI wafer quality.

For standard MPW processes, the sidewall roughness σ_{sidewall} due to an optimized dry etching of the core is typically around 1–10 nm [26–31], while the top/bottom surface roughness σ_{surface} resulting from polished/deposited thin films is usually ~ 0.3 nm [28,29], and their correlation lengths usually are around 50 nm and 30 nm [26–31], respectively. For the popular 450-nm-wide silicon photonic waveguide, the top/bottom surface scattering loss is usually about ~ 0.1 dB/cm, while the sidewall scattering loss is usually about several dB/cm. In this case, it is no doubt that the scattering at the sidewalls is the major loss source. As shown in Fig. 2(a), the loss due to the scattering at the top/bottom surfaces first increases to a maximum (around $W_{\text{co}} = 1 \mu\text{m}$) and then decreases slightly when the core width increases from 0.45 to $3 \mu\text{m}$. This can be explained as follows. When the core width increases, the areas of the top/bottom surfaces increase, which tends to introduce an increase of the scattering loss. Meanwhile, the mode confinement in the core region becomes enhanced, and thus the field amplitudes at the top/bottom surfaces decrease, which tends to decrease the scattering loss. The core-width dependence of the top/bottom surface scattering loss shown in Fig. 2(a) results

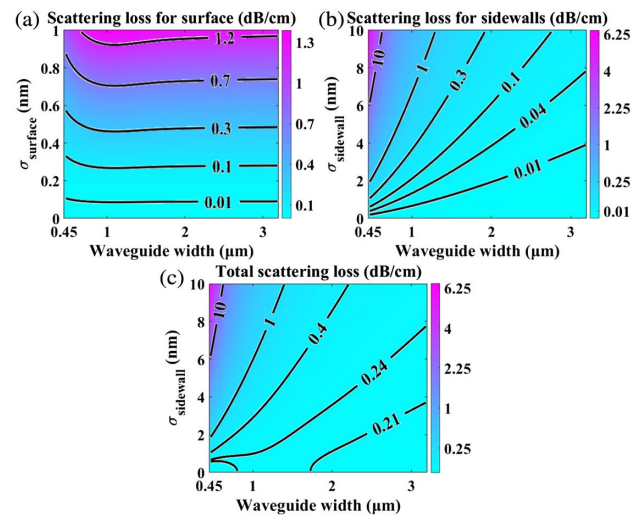


Fig. 2. Calculated losses due to the (a) top/bottom surface scattering (here $\sigma_{\text{sidewall}} = 0$ nm) and (b) sidewall scattering (here $\sigma_{\text{surface}} = 0$ nm). (c) Total scattering loss (here $\sigma_{\text{surface}} = 0.4$ nm).

from the balance of these two factors. In contrast, the loss due to the scattering at the sidewalls can be reduced exponentially as the core width increases, which is due to the significant decrease in field amplitudes at the sidewalls, as shown in Fig. 2(b). For example, the scattering loss is reduced from 4.2 to 0.042 dB/cm in theory when the core width is increased from 0.45 to 2 μm when $\sigma_{\text{sidewall}} = 4$ nm. As a result, the scattering losses from the top/bottom surfaces might become the major factor when the core width is sufficiently large. Figure 2(c) shows the calculated total scattering loss when assuming the top/bottom surface roughness $\sigma_{\text{surface}} = 0.4$ nm. It can be seen that the total scattering loss becomes insensitive to the core width when $W_{\text{co}} > 2$ μm . On the other hand, it is usually not desired to have a very wide core region to avoid the difficulty of mode manipulation (such as higher-mode excitation). Therefore, in this paper, we choose $W_m = 2$ μm in the design of the present waveguide spirals. Correspondingly, the total scattering loss for such a waveguide is about ~ 0.25 dB/cm, which is 10 times less than that for a 450-nm-wide silicon photonic waveguide.

As another key factor to minimize the footprint of the waveguide spiral, the gap width W_{gap} between two adjacent waveguides should be as small as possible without evanescent coupling. As it is well known, the coupling length L_c is calculated by using the following equation [32]:

$$L_c = \frac{\lambda}{2(n_{\text{eff,TE}_0} - n_{\text{eff,TE}_1})}, \quad (1)$$

where λ is the wavelength, and $n_{\text{eff,TE}_0}$ and $n_{\text{eff,TE}_1}$ are the effective indices of the TE_0 and TE_1 supermodes. Here the effective indices are calculated using the finite element method (FEM) mode solver. The coupling length calculated from Eq. (1) is demonstrated as a function of the gap width of the spiral waveguides, as shown in Fig. 3. Since the waveguide spiral is long in our case, the waveguide gap is chosen as $W_{\text{gap}} = 1.5$ μm , and the corresponding coupling length is up to 2400 m, which is sufficient to avoid the cross talk from the adjacent waveguide.

As is well known, the design of a broadened waveguide bend should be careful to avoid excitation of the higher-order mode when light carried by the fundamental mode propagates along the multimode waveguide spiral. Notice that the S-bend in the middle is one of the keys for the waveguide spiral design because there is an abrupt change of the bending radii from R to

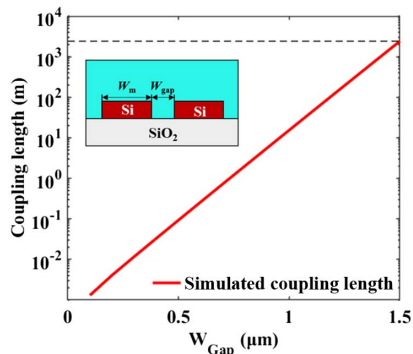


Fig. 3. Calculated coupling length L_c as the gap width W_{gap} in the Archimedean spiral varies.

$-R$. To guarantee ultralow bending losses and negligible higher-order-mode excitation, here we propose a tapered Euler-curve S-bend defined as [33–35]

$$\frac{d\theta}{dL} = \frac{1}{R} = \frac{L}{A^2} + \frac{1}{R_{\text{max}}}, \quad (2)$$

where L is the curve length, A is a constant given by $A = [L_{\text{max}}/(1/R_{\text{min}} - 1/R_{\text{max}})]^{1/2}$, and L_{max} is the total length of the waveguide bend. In general, the maximal radius R_{max} and the minimal radius R_{min} should be as small as possible to shrink the S-bend footprint. As the core width W_m is fixed as 2 μm , the radii ($R_{\text{max}}, R_{\text{min}}$) and the width W_s should comply with the design rule as follows: (1) the maximal radius R_{max} should be equal to the minimal radius of the designed Archimedean spiral waveguide; (2) the maximal radius R_{max} and the width W_s should be optimized to void any notable mode mismatch at the abrupt junction in the middle; (3) the minimal radius R_{min} should be chosen to make the effective diameter D_{eff} [as defined in Fig. 1(b)] of the 180° Euler-curve bend equal to the radius of the inner circle of the Archimedean spiral waveguide.

Figures 4(a) and 4(b) show the calculated excess loss and intermode cross talk as the radius R_{max} and the core width W_s vary. As it can be seen, one can achieve low excess losses and low cross talk by choosing a sufficiently large radius R_{max} and a narrow width W_s . For example, the excess loss is less than 0.01 dB, and the intermode cross talk is negligibly low (< -30 dB) when $W_s < 0.6$ μm and $R_{\text{max}} > 20$ μm (as shown in the marked area). As an example, we choose $R_{\text{max}} = 25$ μm and $W_s = 0.6$ μm by making a trade-off between the loss and the footprint compactness. Accordingly, the total loss is less than 0.01 dB, and the intermode cross talk is less than -30 dB. The radius R_{min} is chosen as 10 μm so that one has $D_{\text{eff}} = R_{\text{max}}$. The footprint of this designed S-bend is as small as 52 $\mu\text{m} \times 32$ μm . In addition, the bend radii of the Archimedean spiral and Euler bend are elaborately designed to be the same at the junction connecting them. Therefore, there is no transition loss and no intermode cross talk when light goes through the junction.

Figures 4(c) and 4(e) show the simulated light propagation in the designed tapered Euler-curve S-bend and the calculated mode-excitation ratios monitored at the output port. Here a three-dimensional finite-difference time-domain (3D-FDTD) method was used in the simulation. From Fig. 4(c), it can be seen that the launched TE_0 mode propagates smoothly along the present tapered Euler-curve S-bend, and no multimode interference is observed, indicating that the excess losses and the intermode cross talk are low. From Fig. 4(e), it can be seen that the estimated excess loss is < 0.016 dB, and the intermode cross talk is < -26 dB in the wavelength band from 1500 to 1600 nm. In contrast, for a regular arc S-bend with the same footprint of 52 $\mu\text{m} \times 32$ μm , significant multimode interference occurs when the TE_0 mode is launched, as shown in Fig. 4(d). From Fig. 4(f), which shows the calculated mode excitation ratios monitored at the output port, the estimated intermode cross talk is as high as -2.3 dB. Therefore, it can be seen that the present tapered Euler-curve S-bend works very well with low-loss and low-cross-talk light propagation of the fundamental mode even when the footprint is compact.

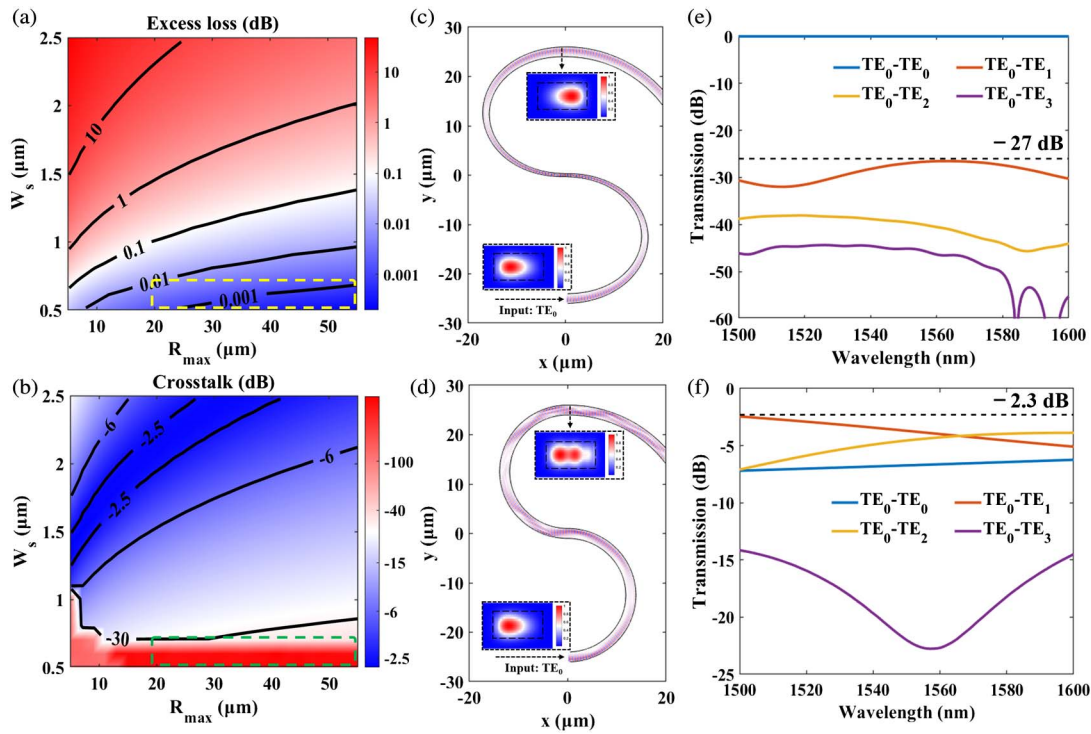


Fig. 4. (a) Calculated excess loss and (b) intermode cross talk as a function of the core width W_s and the bending radius R_{\max} . Simulated light propagation of the TE_0 mode in the (c) tapered Euler-curve S-bend and (d) regular arc S-bend. Calculated excess loss and intermode cross talk at the output port of the (e) tapered Euler S-bend and (f) regular arc S-bend.

3. FABRICATION AND CHARACTERIZATION

The designed silicon photonic waveguide spirals were fabricated by the MPW foundry (Institute of Microelectronics, China) with the standard processes of deep UV lithography and inductively coupled plasma dry-etching. A 1- μm -thick silica thin film was deposited on the top as the upper-cladding. There are seven samples of chips, and each has five waveguide spirals with different lengths of $L = 5, 10, 20, 50,$ and 100 cm for the design with $W_m = 2$ μm . For the present 5-cm-long waveguide spiral, the maximal bending radius is about 240 μm . For any waveguide spiral longer than 5 cm (e.g., $L = 10, 20, 50,$ and 100 cm here), the additional part has a bending radius of >240 μm , in which case, the bend behaves like a straight waveguide with the same core width according to the theoretical analysis. As a result, it is expected that the total propagation losses of these waveguide spirals increase linearly as the total length increases from 5 to 100 cm. In this way, one can estimate the propagation loss by using the cutback method [2,20]. The waveguide spirals with different core widths of $W_m = 0.45$ and 1.6 μm are also fabricated on the same chip to give a comparison.

Figure 5(a) shows the microscope image of the fabricated 50-cm-long silicon photonic waveguide spiral. The setup with an amplified spontaneous emission (ASE) source and an optical spectrum analyzer (OSA) was used for measuring the transmissions of these waveguide spirals. Here grating couplers were used for efficient chip–fiber coupling. The measured transmissions in the wavelength range of 1530 – 1580 nm are shown in Fig. 5(b). It can be seen that the waveguide loss is almost

wavelength insensitive in the C-band, which indicates that there is no multimode interference occurring in the waveguide spirals. The measured waveguide losses at 1550 nm for seven chips are given in Fig. 5(c). It can be seen that the waveguide

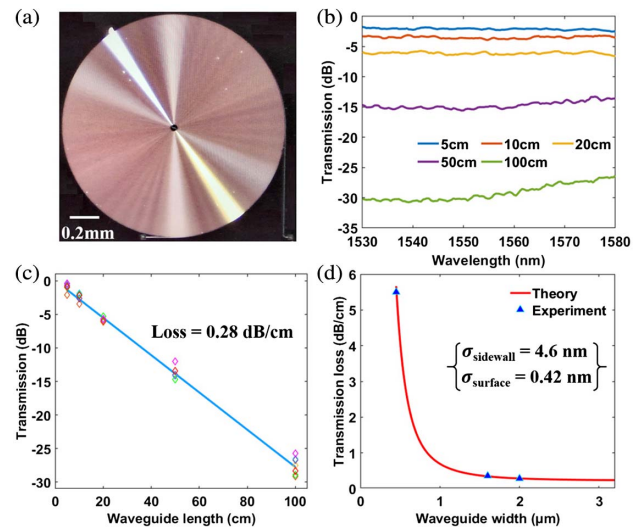


Fig. 5. (a) Microscope image of the fabricated 50-cm-long waveguide spiral. (b) Measured transmissions of the waveguide spirals with different lengths $L = 5, 10, 20, 50,$ and 100 cm. (c) Measured transmissions of the waveguide spirals on seven chips (rhombus) and linear fit (blue curve). (d) Fitting of theoretical scattering losses (red curve) and measured results (dots).

loss increases linearly with propagation distance. The data fitting shows the measured waveguide loss is about ~ 0.28 dB/cm for the case with $W_m = 2$ μm . In contrast, the measured losses for the waveguide spirals with $W_m = 0.45$ and 1.6 μm on the same chips are 5.5 and 0.38 dB/cm, respectively. Figure 5(d) shows the data fitting for the measured waveguide loss by the theoretical results from the three-dimensional volume current method [28] as the core width varies. It can be seen that the estimated roughness values of σ_{sidewall} and σ_{surface} are about 4.6 and 0.42 nm, respectively, which is consistent with the characterization result for the wafer surfaces and waveguide sidewalls.

The present waveguide spirals are further used to develop an n -bit tunable optical true-time-delay line on silicon, as shown in Figs. 6(a) and 6(b). Here the present 10 binary-delay stages

are realized by integrating 11 2×2 Mach-Zehnder (MZ) silicon-photonics switches and 10 waveguide spirals with the time delays of $\Delta\tau, 2\Delta\tau, 4\Delta\tau, \dots,$ and $2^9\Delta\tau$, where the time delay $\Delta\tau$ is about 10 ps. The lengths of the spirals for time delays of $\Delta\tau$ and $2^9\Delta\tau$ are 820 μm and 0.417 m, respectively. Their footprints are, respectively, 0.006 mm^2 and 2.14 mm^2 . Here we used the 2×2 thermo-optic MZ switch reported in our previous work [36]. In particular, these MZ switches have broadened phase shifters with lowered random phase errors, improved fabrication tolerance, and reduced power consumption for phase compensation. In the experiment, a pulse generated by a femtosecond laser (EFLA0222, Langyan) at 1550 nm is launched to the delay line system and received by a wide-bandwidth oscilloscope (Infiniium DCA-X 86100D, Keysight Technologies). The MZ switches are switched

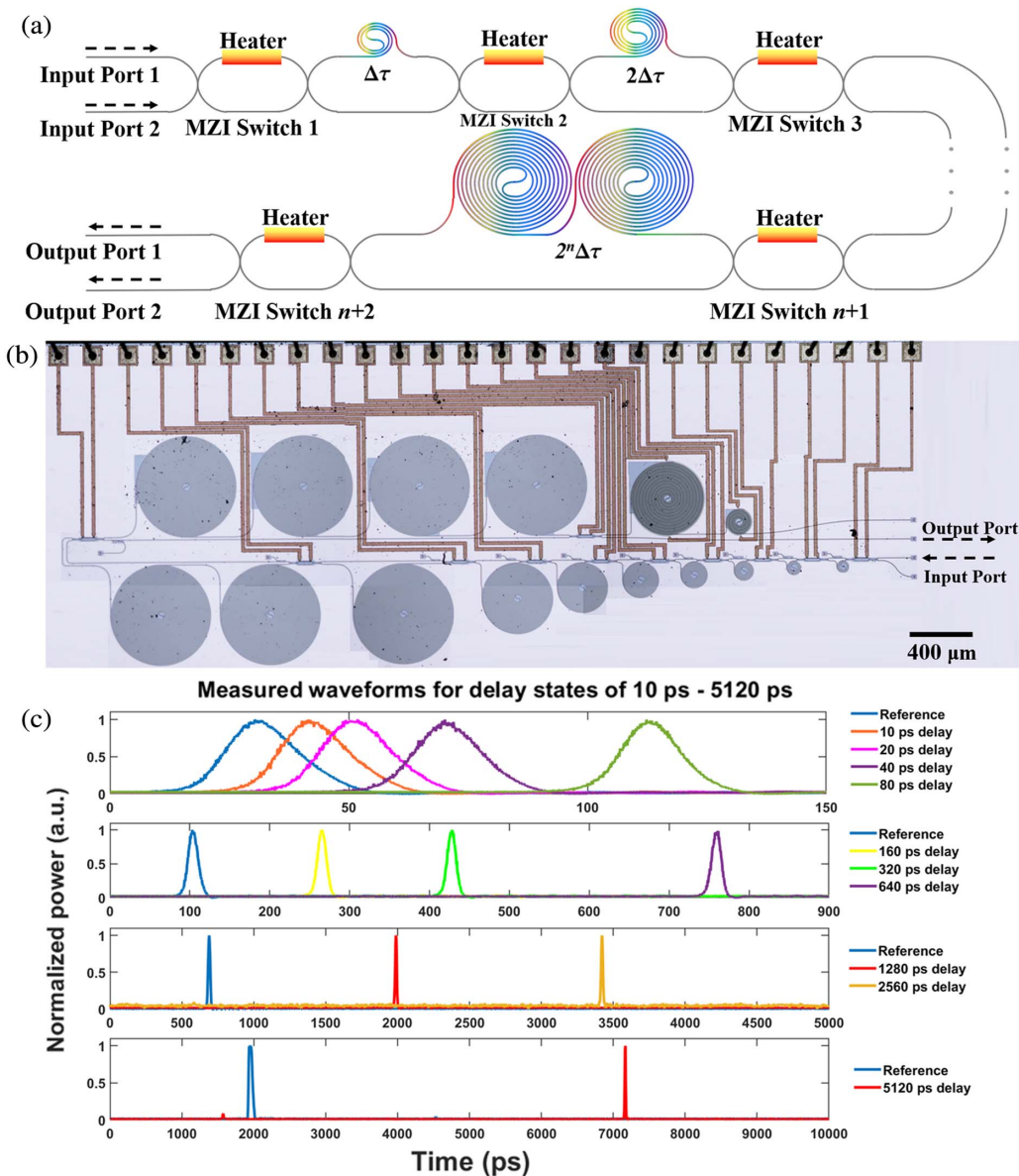


Fig. 6. (a) Schematic configuration of the n -stage tunable optical delay line. (b) Microscope images of the fabricated tunable delay line chip. (c) Measured optical output waveforms of the tunable delay line system with a time delay of 10–5120 ps. Here the blue curves are the reference signals passing through the corresponding straight waveguide.

Table 1. Performance Comparison of On-Chip Tunable Delay Lines Based on Silicon-on-Insulator Waveguides^a

Reference	Waveguide (WG) Type	Delay Tuning		Resolution	Loss	Footprint
		Bit	Range (ps)	(ps)	(dB/cm)	(mm ²)
[1]	Subwavelength grating silicon WG ($H_r = 220$ nm, $W_t = 500$ nm, $\Lambda = 250$ nm)	1	181.9	4.7	2.6	56.55
[5]	Ridge WG ($H_r = 70$ nm, $H_t = 220$ nm, $W_t = 650$ nm)	7	191.37	1.42	2.47	13.32
[4]	Thin silicon WG ($H_r = 60$ nm, $W_t = 1$ μ m)	7	1280	Small (BW = 0.48 nm)	0.6	28.62
[3]	Ridge Si WG ($H_r = 160$ nm, $H_t = 220$ nm, $W_t = 3$ μ m)	7	1270	10	0.9	11.84
This work	Broadened silicon WG ($H_r = 220$ nm, $W_t = 2$ μ m)	10	5110	10	0.28	12.98

^a H_r is the ridge height, H_t is the total height, W_t is the core width, and Λ is the pitch of the subwavelength grating.

thermally by heating their micro-heaters controlled by a multi-channel voltage source (XPOW-40AX-CCvCV-U, Nicslab). Figure 6(c) shows the measured optical output waveforms with the time delay varying from 10 to 5120 ps, which is the longest broadband tunable time delay on a silicon chip with the smallest footprint of 2.2 mm \times 5.9 mm.

Table 1 gives a summary of on-chip tunable optical delay lines reported up to now. In particular, here only broadband time-delay lines are taken into account. Owing to the strong mode confinement, the propagation loss of regular silicon photonic waveguide spirals is usually as high as 2–3 dB/cm [1,5], which can be reduced to 0.6 dB/cm by introducing special thin silicon photonic waveguides or to 0.9 dB/cm by shallow etching to ridge-type waveguides as demonstrated in Refs. [3,4]. In contrast, our proposed silicon waveguide spiral has a propagation as low as 0.28 dB/cm and a minimal bending radius as compact as 10 μ m, which makes it possible to realize a long time delay (e.g., 5.12 ns), a high resolution (e.g., 10 ps), as well as a compact footprint (e.g., 12.98 mm²). More importantly, the proposed silicon waveguide spiral and the time-delay chip can be fabricated with a simple single-etching process provided by a standard MPW foundry. Therefore, it is very easy to achieve arrayed optical time-delay lines for realizing complicated on-chip systems.

4. CONCLUSION

In summary, we have proposed and demonstrated a novel silicon photonic waveguide spiral consisting of single-mode input/output waveguides, two bent waveguide tapers, two broadened Archimedean spiral waveguides, and a tapered Euler-curve S-bend in the middle. The core width of the Archimedean spiral waveguides is chosen optimally to be $W_m = 2$ μ m according to the analyses of the scattering loss, in which way the scattering loss at the sidewalls has been reduced greatly. The tapered Euler-curve S-bend inserted in the middle has been designed carefully to minimize the bending loss as well as the higher-order-mode excitation even for a compact waveguide spiral. The measured propagation loss is about 0.28 dB/cm, which is consistent with our theoretical model. Finally, an on-chip 10-bit tunable optical time delay has been designed and fabricated on the same chip, demonstrating a time delay as long as 5120 ps with a fine resolution of 10 ps. To the best

of our knowledge, this is the first silicon chip with a long delay line up to 100 cm and a broadband time delay up to 5120 ps, owing to the low loss and compact footprint of the proposed waveguide spiral with a tapered Euler-curve S-bend. More importantly, all the waveguides/structures can be fabricated with a simple single-etching process by a standard MPW foundry, which makes it possible to be integrated monolithically with on-chip light sources, amplifiers [37], as well as photodetectors [38]. This provides an excellent option potentially in many applications in the future, such as true-time-delay lines [1–6], on-chip programmable systems [39], photonic beamformers [11], and data centers [40].

Funding. National Major Research and Development Program (2018YFB2200200, 2018YFB2200201); National Science Fund for Distinguished Young Scholars (61725503); National Natural Science Foundation of China (61961146003, 91950205); Zhejiang Provincial Major Research and Development Program (2021C01199); Zhejiang Provincial Natural Science Foundation (LD19F050001, LZ18F050001); Fundamental Research Funds for the Central Universities.

Disclosures. The authors declare no conflicts of interest.

REFERENCES

1. Y. Wang, H. Sun, M. Khalil, W. Dong, I. Gasulla, J. Capmany, and L. R. Chen, "On-chip optical true time delay lines based on subwavelength grating waveguides," *Opt. Lett.* **46**, 1405–1408 (2021).
2. R. L. Moreira, J. Garcia, W. Li, J. Bauters, J. S. Barton, M. J. R. Heck, J. E. Bowers, and D. J. Blumenthal, "Integrated ultra-low-loss 4-bit tunable delay for broadband phased array antenna applications," *IEEE Photon. Technol. Lett.* **25**, 1165–1168 (2013).
3. J. Xie, L. Zhou, Z. Li, J. Wang, and J. Chen, "Seven-bit reconfigurable optical true time delay line based on silicon integration," *Opt. Express* **22**, 22707–22715 (2014).
4. X. Wang, L. Zhou, R. Li, J. Xie, L. Lu, K. Wu, and J. Chen, "Continuously tunable ultra-thin silicon waveguide optical delay line," *Optica* **4**, 507–515 (2017).
5. P. Zheng, C. Wang, X. Xu, J. Li, D. Lin, G. Hu, R. Zhang, B. Yun, and Y. Cui, "A seven bit silicon optical true time delay line for Ka-band phased array antenna," *IEEE Photon. J.* **11**, 5501809 (2019).
6. H. Sun, Y. Wang, and L. R. Chen, "Integrated discretely tunable optical delay line based on step-chirped subwavelength grating waveguide Bragg gratings," *J. Lightwave Technol.* **38**, 5551–5560 (2020).

7. B. Wu, Y. Yu, J. Xiong, and X. Zhang, "Silicon integrated interferometric optical gyroscope," *Sci. Rep.* **8**, 8766 (2018).
8. S. Gundavarapu, M. Belt, T. A. Huffman, M. A. Tran, T. Komljenovic, J. E. Bowers, and D. J. Blumenthal, "Interferometric optical gyroscope based on an integrated Si₃N₄ low-loss waveguide coil," *J. Lightwave Technol.* **36**, 1185–1191 (2018).
9. G. Yurtsever, B. Považay, A. Alex, B. Zabihian, W. Drexler, and R. Baets, "Photonic integrated Mach-Zehnder interferometer with an on-chip reference arm for optical coherence tomography," *Biomed. Opt. Express* **5**, 1050–1061 (2014).
10. X. Ji, X. Yao, Y. Gan, A. Mohanty, M. A. Tadayon, C. P. Hendon, and M. Lipson, "On-chip tunable photonic delay line," *APL Photon.* **4**, 090803 (2019).
11. C. Zhu, L. Lu, W. Shan, W. Xu, G. Zhou, L. Zhou, and J. Chen, "Silicon integrated microwave photonic beamformer," *Optica* **7**, 1162–1170 (2020).
12. P. Zheng, X. Xu, D. Lin, P. Liu, G. Hu, B. Yun, and Y. Cui, "A wideband 1×4 optical beam-forming chip based on switchable optical delay lines for Ka-band phased array," *Opt. Commun.* **488**, 126842 (2021).
13. J. F. Bauters, M. J. R. Heck, D. D. John, J. S. Barton, C. M. Bruinink, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding," *Opt. Express* **19**, 24090–24101 (2011).
14. H. Lee, T. Chen, J. Li, O. Painter, and K. J. Vahala, "Ultra-low-loss optical delay line on a silicon chip," *Nat. Commun.* **3**, 867 (2012).
15. K. K. Lee, D. R. Lim, L. C. Kimerling, J. Shin, and F. Cerrina, "Fabrication of ultralow-loss Si/SiO₂ waveguides by roughness reduction," *Opt. Lett.* **26**, 1888–1890 (2001).
16. J. Cardenas, C. B. Poitras, J. T. Robinson, K. Preston, L. Chen, and M. Lipson, "Low loss etchless silicon photonic waveguides," *Opt. Express* **17**, 4752–4757 (2009).
17. D. K. Sparacin, S. J. Spector, and L. C. Kimerling, "Silicon waveguide sidewall smoothing by wet chemical oxidation," *J. Lightwave Technol.* **23**, 2455–2461 (2005).
18. F. Gao, Y. Wang, G. Cao, X. Jia, and F. Zhang, "Improvement of sidewall surface roughness in silicon-on-insulator rib waveguides," *Appl. Phys. B* **81**, 691–694 (2005).
19. C. Bellegarde, E. Pargon, C. Sciancalepore, C. Petit-Etienne, V. Hugues, D. Robin-Brosse, J.-M. Hartmann, and P. Lyan, "Improvement of sidewall roughness of submicron SOI waveguides by hydrogen plasma and annealing," *IEEE Photon. Technol. Lett.* **30**, 591–594 (2018).
20. P. Dong, W. Qian, S. Liao, H. Liang, C. C. Kung, N. N. Feng, R. Shafiqi, J. Fong, D. Feng, A. V. Krishnamoorthy, and M. Asghari, "Low loss shallow-ridge silicon waveguides," *Opt. Express* **18**, 14474–14479 (2010).
21. W. Bogaerts and L. Chrostowski, "Silicon photonics circuit design: methods, tools and challenges," *Laser Photon. Rev.* **12**, 1700237 (2018).
22. D. Dai, "Advanced passive silicon photonic devices with asymmetric waveguide structures," *Proc. IEEE* **106**, 2117–2143 (2018).
23. D. Thomson, A. Zilkie, J. E. Bowers, T. Komljenovic, G. T. Reed, L. Vivien, D. Marris-Morini, E. Cassan, L. Virôt, J.-M. Fédéli, J.-M. Hartmann, J. H. Schmid, D.-X. Xu, F. Boeuf, P. O'Brien, G. Z. Mashanovich, and M. Nedeljkovic, "Roadmap on silicon photonics," *J. Opt.* **18**, 073003 (2016).
24. Y. Vlasov and S. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Opt. Express* **12**, 1622–1631 (2004).
25. S. Suzuki, M. Yanagisawa, Y. Hibino, and K. Oda, "High-density integrated planar lightwave circuits using SiO₂-GeO₂ waveguides with a high refractive index difference," *J. Lightwave Technol.* **12**, 790–796 (1994).
26. T. Barwicz and H. A. Haus, "Three-dimensional analysis of scattering losses due to sidewall roughness in microphotonic waveguides," *J. Lightwave Technol.* **23**, 2719–2732 (2005).
27. C. Ciminelli, V. M. N. Passaro, F. Dell'Olio, and M. N. Armenise, "Three-dimensional modelling of scattering loss in InGaAsP/InP and silica-on-silicon bent waveguides," *J. Eur. Opt. Soc.* **4**, 09015 (2009).
28. J. F. Bauters, M. J. Heck, D. John, D. Dai, M. C. Tien, J. S. Barton, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Ultra-low-loss high-aspect-ratio Si₃N₄ waveguides," *Opt. Express* **19**, 3163–3174 (2011).
29. C. Qiu, F. Gan, Z. Sheng, H. Li, W. Liu, L. Li, A. Pang, A. Wu, X. Wang, and S. Zou, "Fabrication, characterization and loss analysis of silicon nanowaveguides," *J. Lightwave Technol.* **32**, 2303–2307 (2014).
30. K. K. Lee, D. R. Lim, H.-C. Luan, A. Agarwal, J. Foresi, and L. C. Kimerling, "Effect of size and roughness on light transmission in a Si/SiO₂ waveguide: experiments and model," *Appl. Phys. Lett.* **77**, 1617–1619 (2000).
31. T. Barwicz and H. I. Smith, "Evolution of line-edge roughness during fabrication of high-index-contrast microphotonic devices," *J. Vac. Sci. Technol. B* **21**, 2892 (2003).
32. L. B. Soldano and E. C. M. Pennings, "Optical multi-mode interference devices based on self-imaging: principles and applications," *J. Lightwave Technol.* **13**, 615–627 (1995).
33. X. Jiang, H. Wu, and D. Dai, "Low-loss and low-crosstalk multimode waveguide bend on silicon," *Opt. Express* **26**, 17680–17689 (2018).
34. L. Zhang, L. Jie, M. Zhang, Y. Wang, Y. Xie, Y. Shi, and D. Dai, "Ultrahigh-Q silicon racetrack resonators," *Photon. Res.* **8**, 684–689 (2020).
35. M. Cherchi, S. Ylisen, M. Harjanne, M. Kapulainen, and T. Aalto, "Dramatic size reduction of waveguide bends on a micron-scale silicon photonic platform," *Opt. Express* **21**, 17814–17823 (2013).
36. L. Song, H. Li, and D. Dai, "Mach-Zehnder silicon-photonic switch with low random phase errors," *Opt. Lett.* **46**, 78–81 (2021).
37. S. Liu and A. Khope, "Latest advances in high-performance light sources and optical amplifiers on silicon," *J. Semicond.* **42**, 041307 (2021).
38. C. Liu, J. Guo, L. Yu, J. Li, M. Zhang, H. Li, Y. Shi, and D. Dai, "Silicon/2D-material photodetectors: from near-infrared to mid-infrared," *Light Sci. Appl.* **10**, 123 (2021).
39. Y. Zhao, X. Wang, D. Gao, J. Dong, and X. Zhang, "On-chip programmable pulse processor employing cascaded MZI-MRR structure," *Front. Optoelectron.* **12**, 148–156 (2018).
40. H. Wang, H. Chai, Z. Lv, Z. Zhang, L. Meng, X. Yang, and T. Yang, "Silicon photonic transceivers for application in data centers," *J. Semicond.* **41**, 101301 (2020).