PHOTONICS Research

80 GHz germanium waveguide photodiode enabled by parasitic parameter engineering

Yang Shi,† De Zhou,† Yu Yu,* and Xinliang Zhang

Wuhan National Laboratory for Optoelectronics & School of Optical and Electronic Information, Huazhong University of Science and Technology, Wuhan 430074, China
**Corresponding author: yuyu@mail.hust.edu.cn*

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A high-speed germanium (Ge) waveguide photodiode (PD) is one of the key components of an integrated silicon photonics platform for large-capacity data communication applications, but the parasitic parameters limit the increase of its bandwidth. Several studies have been reported to reduce parasitic parameters, at the cost of compromising other performances. Here, we propose and investigate a bandwidth-boosting technique by comprehensively engineering the parasitic parameters. Experimentally, a bandwidth up to 80 GHz is realized for vertical positive-intrinsic-negative (PIN) Ge PDs without decreasing the responsivity and dark current, indicating that parasitic parameter engineering is a promising method to promote high-speed performance of Ge PDs.

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1. INTRODUCTION

Silicon photonics is promising for the demands of large-capacity data communications applications such as data centers, high-performance computers, and biomedical sensing [1,2]. One of the indispensable technologies in silicon photonics is high-speed signal detection for the near-infrared (~1550 nm), and germanium (Ge) is one of the most promising materials for near-infrared photodiodes (PDs) in optoelectronic integrated circuits due to its large absorption coefficient and compatibility with complementary metal-oxide-semiconductor (CMOS) technology [3]. Its superiority has led to substantial investigations of Ge PDs featuring high-frequency and responsivity in recent decades [4–10], while the parasitic parameters from either junction or electrodes limit a further increase in the bandwidth [11–13]. The Ge PDs can be divided into vertical and lateral positive-intrinsic-negative (PIN) junction structures. Although the bandwidth has achieved 120 GHz at −1 V for lateral ones [7], the dark current is very large and the fabrication processes are complex, requiring silicon corrosion and a Ge chemical mechanical polish [14,15]. On the other hand, vertical PIN PDs enjoy great popularity, for their simple fabrication processes. However, they suffer from low bandwidth due to high parasitic parameters [16,17]. Therefore, the parasitic parameters are optimized in different ways to overcome these issues, such as shrinking the intrinsic region to reduce the junction capacitance [11], optimizing silicon doping to reduce the series resistance [18], and introducing spiral inductors in the electrodes to offset part of capacitance effect [5]. However, all of these reported schemes optimize the parasitic parameters separately, without comprehensively considering the relationships between different aspects. For instance, in Ref. [11], only the junction capacitance is reduced, and the bandwidth is still limited by series resistance and electrode parasitic parameters. In addition, they also suffer from optical responsivity degradation or fabrication complexity.

In this work, we propose and demonstrate a high-speed Ge vertical PIN PD, by comprehensively optimizing the parasitic parameters from both junction and electrodes. An equivalent circuit model containing transit time and all parasitic parameters is considered. The bandwidth limit under a given intrinsic region size is investigated through two-dimensional (2D) joint optimization, by varying the silicon doping concentration and electrodes inductance. Experimentally, the bandwidth is enhanced from 27 to 80 GHz, with a low dark current of 6.4 nA and an optical responsivity of 0.89 A/W, leading to a high detectivity. This is, to the best of our knowledge, the highest bandwidth of a CMOS-compatible vertical Ge PIN PD reported to date. This work provides guidance for the design of high-speed and high-detectivity Ge PDs.

2. OPERATION PRINCIPLE

Herein, we give a comprehensive bandwidth analysis of Ge PDs on a silicon-on-insulator (SOI) platform. Figure 1 shows the cross-section view of the conventional Ge PD, and the corresponding equivalent circuit is also provided. The PIN diode is formed by the N++ doped germanium, intrinsic

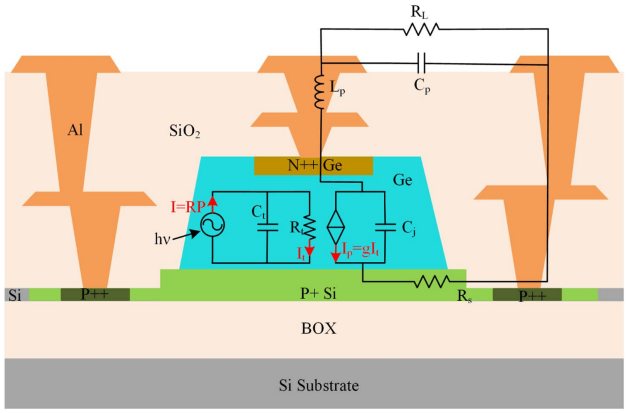

Fig. 1. Cross-section view and equivalent circuit for a conventional PD.

germanium, and P+ doped silicon, while the N++ doped germanium and P++ doped silicon constitute the ohmic contact with the metal. In the circuit, the current source I represents the photoelectric conversion in the absorption region. The bandwidth of the PD is determined by both the transit time and parasitic parameters. The transit time is represented by the equivalent resistance R_t and the equivalent capacitance C_t [19]. The parasitic parameters contain the junction capacitance C_j, the series resistance R_s that mainly comes from the P+ doping region and silicon-metal contact resistance, and the electrode parasitic parameters L_p and C_p, as well as the external load R_L. The current-controlled current source I_p acts as a bridge between the transit time and the parasitic parameters, while the I_t is the current flowing through the R_t and the g relates to the absolute amplitude of the load current, which can be eliminated in normalization.

The normalized frequency response of the radio frequency (RF) current through the load is shown in

$$H(f) = \frac{1}{1 + j2\pi f R_t C_t} \cdot \frac{1}{1 + j2\pi f R_p C_j} \cdot \frac{1}{1 + j2\pi f R_L C_p}, \tag{1}$$

where $R_p = R_L/(1 + j2\pi R_L C_p) + R_s + j2\pi f L_p$.

Then, the 3 dB bandwidth can be obtained by solving the equation $|H(f)|^2 = 1/2$. Figure 2(a) shows the simulated bandwidth related to the R_s and the L_p. The inserts are other parameters used in the simulation with the intrinsic region of $d = 400$ nm, $W = 5$ μm, and $L = 10$ μm. They are

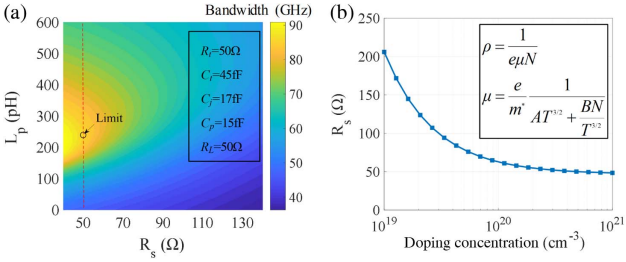

Fig. 2. (a) Simulated bandwidth varying with R_s and L_p. (b) Calculated R_s varying with p-type doping concentration.

calculated or simulated using the equations in Refs. [19,20]. According to Fig. 2(a), the bandwidth increases with the decreased R_s for a fixed L_p. When R_s is fixed, the bandwidth increases first and then decreases, with the inductance increasing. This is because the capacitance effect is canceled out and the bandwidth increases with increase in the inductance. However, as the inductance continues to increase, the high-frequency and medium-frequency responses are quickly cut off and the bandwidth instead decreases [21]. Note that one can always find an appropriate inductance that maximizes the bandwidth.

As an implementation, the series resistance R_s can be changed effectively by the silicon P+ doping concentration calculated via the model in Ref. [22], as shown in Fig. 2(b). When the doping concentration increases, the resistance decreases until it reaches a constant of ∼50 Ω for the given footprint of silicon we adopted. The resistance of P+ doped silicon will not be further reduced until ∼10 Ω, considering that the impurities cannot be completely ionized at a sufficiently high doping concentration [22]. The minimum of R_s is mainly limited by the unchanged silicon-metal contact resistance of ∼40 Ω [18]. Based on the analyses above, the full P++ doping is used in the whole silicon layer to minimize the resistance. On the other hand, for conventional ground-source-ground (GSG) electrodes, the L_p is very small and can be significantly enlarged by introducing inductors of different lengths to generate a gain peaking effect [5,6]. When the inductance is about 240 pH, the bandwidth limit is ∼85 GHz for the minimum series resistance of 50 Ω, signed in Fig. 2(a). Note that other parasitic parameters remain almost unchanged for a fixed intrinsic region size, and it is reasonable to perform the 2D optimization for R_s and L_p. Thus, the theoretical limit can be obtained compared to the individual optimization.

3. FABRICATION AND EXPERIMENTAL RESULTS

We design and fabricate three PDs, namely PD-A, PD-B, and PD-REF with different silicon doping concentrations and electrode shapes, corresponding to different R_s and L_p, as shown in Table 1. The PD-A and PD-B are the ones with 2D optimization and inductance-only optimization, while the PD-REF is the conventional scheme. Optimizing the R_s alone, which has been reported in Ref. [18], usually does not revolutionize the bandwidth and it is not repeated here. The inductance is mainly determined by the geometry of the electrodes. The thickness of the electrode is fixed at 2 μm, and the plane shape can be freely designed and optimized. The series resistance is mainly determined by the geometry and doping concentration of silicon. A larger doping concentration contributes to a

Table 1. Silicon Doping and Electrode Inductors of Three Kinds of PDs

Type	Silicon Doping	Simulated Inductor
PD-A	P++	With 240 pH
PD-B	P+	With 300 pH
PD-REF	P+	Without

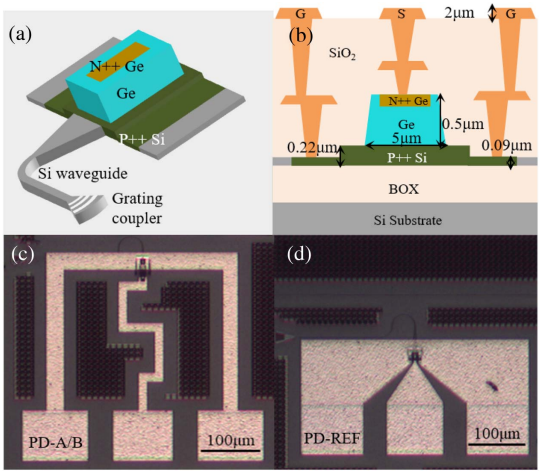

Fig. 3. (a) 3D schematic of the PD-A. (b) Cross-section of the PD-A with full silicon P++ doping. (c) Microscopic image for the PD-A/B with inductor. (d) Microscopic image for the PD-REF without inductor.

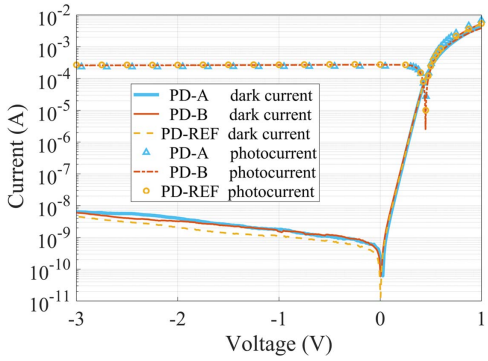

Fig. 4. *I-V* characteristics of PDs at dark and with light incidence.

smaller series resistance, for a given geometry size. The 3D schematic of the PD-A is shown in Fig. 3(a). The light is coupled from the laser to the PDs using the grating coupler and Si waveguide. The cross-section and microscopic image of the PD-A are shown in Figs. 3(b) and 3(c), respectively. The footprints and electrodes of the PD-A and PD-B are the same, and only the microscopic image of the PD-A is provided for simplicity. The microscope image of the PD-REF with conventional doping and GSG electrodes is shown in Fig. 3(d).

The PDs are fabricated using an SOI wafer with an 220 nm thick silicon top layer and a 2 μm buried oxide (BOX). The grating coupler is first etched 70 nm from 220 nm silicon layer. After that, the silicon layer is etched into a ridge waveguide with a 90 nm slab for better light constraints. Then, the silicon top layer is P++ or P+ doping using different doses of boron. A 500 nm thick germanium is deposited on the doping region of the silicon, and ~100 nm depth N++ doping of phosphorus is implanted on top of the Ge to form the vertical PIN junction. The area of the Ge is 5 μm wide and 10 μm in length. The first via and metal to N++ Ge and P++ silicon are fabricated; subsequently, the second via and metal are fabricated to form different inductors. PD-A, PD-B, and PD-REF were fabricated on the same wafer and at the same time.

A. Static Measurements

The *I–V* characteristics of the PDs are measured using a source meter (B2900, Keysight Technologies, Santa Rosa, CA, USA), a probe station, and a tunable laser (TLG-200, Alnair Labs Corp., Tokyo, Japan). The photocurrent is measured at 1550 nm under a received optical power of −5.8 dBm, by extracting the coupling loss of the grating coupler. We do not use a normalization silicon waveguide to remove the losses caused by propagation because the loss is negligible. Figure 4 shows the *I-V* characteristics of the three PDs. The dark currents are similar under different bias voltages, indicating that engineering the parasitic parameters does not degrade the dark current. The photocurrent is almost constant under 0 to −3 V owing to the strong built-in electric field that is capable of sweeping out most of the photo-generated carriers within their lifetime. Table 2 presents the dark currents of PD-A, PD-B, and PD-REF at −3 V, and they are 6.4, 6.0 and 4.5 nA, respectively. The measured responsivities are 0.89, 1.00, and 1.00 A/W. The PD-A shows a slightly lower responsivity induced by a stronger free carrier absorption [23]. These suggest that engineering the parasitic parameters rarely degrades the responsivity and dark current because they are not directly related to the parasitic parameters.

Table 2. Responsivities and Dark Currents of Three Kinds of PDs

Type	Responsivity (A/W)	Dark Current (nA)
PD-A	0.89	6.4
PD-B	1.00	6.0
PD-REF	1.00	4.5

B. Small-Signal Measurements

Small-signal RF measurements are carried out using a 67 GHz vector network analyzer (VNA: MS4647B, Anritsu Corp., Kanagawa, Japan) in the test range of 10 MHz to 70 GHz with 50 Ω load resistance. The impedance standard substrate [101-190C, FormFactor (formerly Cascade Microtech), Beaverton, OR, USA] is used to calibrate the bias-tee, cables, and microprobe (I67-GSG-150, FormFactor).

The normalized S_{21} parameters are shown in Fig. 5. The measured 3-dB bandwidths of PD-A and PD-B are larger than 70 GHz, while the bandwidth of PD-REF is only 27 GHz. The frequency response beyond 70 GHz cannot be tested due to the limited bandwidth of the VNA. To further estimate the bandwidth, the equivalent circuit model is used. The measured S_{21} curve is first fitted in the range of 0–70 GHz to extract the parasitic parameters. Then it is simulated in the range of 0–90 GHz, and the 3-dB bandwidths of PD-A and PD-B are found to be 80 and 73 GHz, respectively, as the dashed lines in Fig. 5 show. The fitting results agree well with the test ones. The extracted series resistances are 62.1 and 82.4 Ω, respectively, corresponding to a bandwidth limit of 82 and 75 GHz. Obviously, the proposed 2D parameters optimization

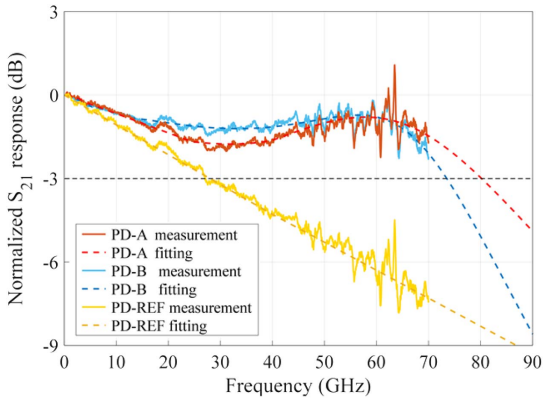

Fig. 5. Measured and fitted bandwidth characteristics of Ge PDs.

helps to reach the theoretical limit for a given intrinsic region. Further enhancement of bandwidth is possible by reducing the thickness of Ge, as the bandwidths of the optimized PDs are now transit time limited. For example, the theoretical bandwidth limit is up to 100 GHz for intrinsic Ge that is 300 nm thick.

4. DISCUSSION

To fairly characterize the proposed PDs, we take advantage of the concept of detectivity (D^*), which is calculated using [24]

$$D^* = \frac{R\sqrt{A\Delta f}}{\sqrt{I_{\text{shot}}^2 + I_{\text{ther}}^2}}, \tag{2}$$

where R is the responsivity, Δf is the unit bandwidth (1 Hz), I_{shot} is the shot noise, and I_{ther} is the thermal noise. I_{shot} and I_{ther} can be expressed as

$$I_{\text{shot}} = \sqrt{2qI_{\text{dark}}\Delta f}, \tag{3}$$

$$I_{\text{ther}} = \sqrt{\frac{4kT\Delta f}{R_{\text{shunt}}}}, \tag{4}$$

where I_{dark} is the dark current and R_{shunt} is the shunt resistance, which is extracted by taking $\mathrm{d}I/\mathrm{d}V$ at $V = 0$. It can be seen from Eq. (2) that D^* includes both the responsivity and the dark current, and it is a more suitable metric to characterize the comprehensive performance of the PD. A higher responsivity and a lower dark current can lead to a higher D^*. Table 3 summarizes the comparison of the high-speed waveguide-coupled Ge PDs in literature and our work. The latter has the best detectivity, thanks to the ultralow dark current and highest responsivity. The bandwidth is also the highest among the reported vertical Ge PDs using conventional fabrication processes. Although Ref. [7] demonstrated a bandwidth as high as 120 GHz, the process is complex (requiring silicon corrosion and a Ge chemical mechanical polish) and the dark current is large, resulting in a ~15× lower detectivity. We believe the proposed work is very attractive for applications such as a high-speed data communications system, considering the high-performance and zero-change fabrication process in the standard silicon photonics platform.

Table 3. Comparison of the High-Speed Waveguide-Coupled Ge PDs

Refs.	Type	Dark Current (nA)	Responsivity (A/W)	Bandwidth (GHz)	Detectivity ($\text{cm}\cdot\text{Hz}^{1/2}\cdot\text{W}^{-1}$)
[4]	Vertical	19	0.6	50	2.56×10^9
[5]	Vertical	3000	0.75	60	6.85×10^8
[6]	Vertical	61	0.85	67	4.30×10^9
[7]	Lateral	4000	0.8	120	8.94×10^8
[8]	Lateral	2.5	0.72	67	6.78×10^9
[9]	Lateral	40	0.5	50	3.13×10^9
This work	Vertical	6.4	0.89	80	1.33×10^{10}

5. CONCLUSION

We have demonstrated that 2D parasitic parameter engineering enables a significant bandwidth boost for Ge PDs. The bandwidth is experimentally enhanced from 27 to 80 GHz, and approaches the limit of 82 GHz. This method does not cause a degradation in responsivity and the dark current, which results in a very high detectivity. We believe it will pave the way toward the design of high-speed, high-detectivity Ge PDs.

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†These authors contributed equally to this paper.

REFERENCES

1. A. H. Atabaki, S. Moazeni, F. Pavanello, H. Gevorgyan, J. Notaros, L. Alloatti, M. T. Wade, C. Sun, S. A. Kruger, H. Y. Meng, K. Al Qubaisi, I. Wang, B. H. Zhang, A. Khilo, C. V. Baiocco, M. A. Popovic, V. M. Stojanovic, and R. J. Ram, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," Nature **556**, 349–354 (2018).
2. J. You, Y. K. Luo, J. Yang, J. H. Zhang, K. Yin, K. Wei, X. Zheng, and T. Jiang, "Hybrid/integrated silicon photonics based on 2D materials in optical communication nanosystems," Laser Photon. Rev. **14**, 2000239 (2020).
3. J. Michel, J. F. Liu, and L. C. Kimerling, "High-performance Ge-on-Si photodetectors," Nat. Photonics **4**, 527–534 (2010).
4. H. T. Chen, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, P. Absil, G. Roelkens, and J. Van Campenhout, "High-responsivity low-voltage 28-Gb/s Ge p-i-n photodetector with silicon contacts," J. Lightwave Technol. **33**, 820–824 (2015).
5. A. Novack, M. Gould, Y. S. Yang, Z. Xuan, M. Streshinsky, Y. Liu, G. Capellini, A. E. J. Lim, G. Q. Lo, T. Baehr-Jones, and M. Hochberg, "Germanium photodetector with 60 GHz bandwidth using inductive gain peaking," Opt. Express **21**, 28387–28393 (2013).
6. G. Y. Chen, Y. Yu, S. P. Deng, L. Liu, and X. L. Zhang, "Bandwidth improvement for germanium photodetector using wire bonding technology," Opt. Express **23**, 25700–25706 (2015).

7. L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, and J. M. Fedeli, "Zero-bias 40 Gbit/s germanium waveguide photodetector on silicon," Opt. Express **20**, 1096–1101 (2012).
8. H. Chen, P. Verheyen, P. De Heyn, G. Lepage, J. De Coster, S. Balakrishnan, P. Absil, W. Yao, L. Shen, G. Roelkens, and J. Van Campenhout, "–1 V bias 67 GHz bandwidth Si-contacted germanium waveguide p-i-n photodetector for optical links at 56 Gbps and beyond," Opt. Express **24**, 4622–4631 (2016).
9. L. Virot, D. Benedikovic, B. Szelag, C. Alonso-Ramos, B. Karakus, J. M. Hartmann, X. Le Roux, P. Crozat, E. Cassan, D. Marris-Morini, C. Baudot, F. Boeuf, J. M. Fedeli, C. Kopp, and L. Vivien, "Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction," Opt. Express **25**, 19487–19496 (2017).
10. J. F. Song, A. L. Eu-Jin, X. S. Luo, Y. Huang, X. G. Tu, L. X. Jia, Q. Fang, T. Y. Liow, M. B. Yu, and G. Q. Lo, "Microring resonator photodetector for enhancement in L-band performance," Opt. Express **22**, 26976–26984 (2014).
11. C. T. DeRose, D. C. Trotter, W. A. Zortman, A. L. Starbuck, M. Fisher, M. R. Watts, and P. S. Davids, "Ultra compact 45 GHz CMOS compatible germanium waveguide photodiode with low dark current," Opt. Express **19**, 24897–24904 (2011).
12. S. R. Liao, N. N. Feng, D. Z. Feng, P. Dong, R. Shafiiha, C. C. Kung, H. Liang, W. Qian, Y. Liu, J. Fong, J. E. Cunningham, Y. Luo, and M. Asghari, "36 GHz submicron silicon waveguide germanium photodetector," Opt. Express **19**, 10967–10972 (2011).
13. L. Vivien, J. Osmond, J. M. Fedeli, D. Marris-Morini, P. Crozat, J. F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n germanium photodetector integrated in a silicon-on-insulator waveguide," Opt. Express **17**, 6252–6257 (2009).
14. S. Lischke, D. Knoll, C. Mai, L. Zimmermann, A. Peczek, M. Kroh, A. Trusch, E. Krune, K. Voigt, and A. Mai, "High bandwidth, high responsivity waveguide-coupled germanium p-i-n photodiode," Opt. Express **23**, 27213–27220 (2015).
15. R. Going, T. J. Seok, J. Loo, K. Hsu, and M. C. Wu, "Germanium wrap-around photodetectors on silicon photonics," Opt. Express **23**, 11975–11984 (2015).
16. X. L. Li, Z. Liu, L. Z. Peng, X. Q. Liu, N. Wang, Y. Zhao, J. Zheng, Y. H. Zuo, C. L. Xue, and B. W. Cheng, "High-performance germanium waveguide photodetectors on silicon," Chin. Phys. Lett. **37**, 038502 (2020).
17. T. Yin, R. Cohen, M. M. Morse, G. Sarid, Y. Chetrit, D. Rubin, and M. J. Paniccia, "31 GHz Ge *n-i-p* waveguide photodetectors on silicon-on-insulator substrate," Opt. Express **15**, 13965–13971 (2007).
18. J. M. Lee, M. Y. Kim, and W. Y. Choi, "Series resistance influence on performance of waveguide-type germanium photodetectors on silicon," Chin. Opt. Lett. **15**, 100401 (2017).
19. G. Wang, T. Tokumitsu, I. Hanawa, K. Sato, and M. Kobayashi, "Analysis of high speed pin photodiode S-parameters by a novel small-signal equivalent circuit model," IEEE Microw. Wireless Compon. Lett. **12**, 378–380 (2002).
20. Y. Ishikawa and K. Wada, "Near-infrared Ge photodiodes for Si photonics: operation frequency and an approach for the future," IEEE Photon. J. **2**, 306–320 (2010).
21. M. Gould, T. Baehr-Jones, R. Ding, and M. Hochberg, "Bandwidth enhancement of waveguide-coupled photodetectors with inductive gain peaking," Opt. Express **20**, 7101–7111 (2012).
22. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, 2006).
23. J. Isenberg and W. Warta, "Free carrier absorption in heavily doped silicon layers," Appl. Phys. Lett. **84**, 2265–2267 (2004).
24. M. J. Deen and P. K. Basu, *Silicon Photonics: Fundamentals and Devices* (Wiley, 2012).