Inverse design of digital nanophotonic devices using the adjoint method

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A high-efficiency inverse design of "digital" subwavelength nanophotonic devices using the adjoint method is proposed. We design a single-mode 3 dB power divider and a dual-mode demultiplexer to demonstrate the efficiency of the proposed inverse design approach, called the digitized adjoint method, for single- and dual-object optimization, respectively. The optimization comprises three stages: 1) continuous variation for an "analog" pattern; 2) forced permittivity biasing for a "quasi-digital" pattern; and 3) a multilevel digital pattern. Compared with the conventional brute-force method, the proposed method can improve design efficiency by about five times, and the performance optimization can reach approximately the same level. The method takes advantages of adjoint sensitivity analysis and digital subwavelength structure and creates a new way for the efficient and high-performance design of compact digital subwavelength nanophotonic devices, which could overcome the efficiency bottleneck of the brute-force method, which is restricted by the number of pixels of a digital pattern, and improve the device performance by extending a conventional binary pattern to a multilevel one. © 2020 Chinese Laser Press

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1. INTRODUCTION

A reduction in the size of integrated all-dielectric silicon photonic devices while maintaining a high level of performance is a key challenge for applications with limited physical space such as on-chip optical interconnects. An inverse design approach has recently emerged as a promising way to realize ultracompact and high-performance nanophotonic devices for high-density integration, including nanostructured photonic crystals [1], wavelength demultiplexers [2-4], power dividers [5-9], polarization beam splitters [10], polarization rotators [11], mode demultiplexers [12,13], mode converters [14,15], waveguide bends [16], and twisted light emitters [17]. The basic idea of inverse design is that the design area of a subwavelength photonic device is first discretized into different numbers of nanoscale elements; then, we use optimization methods to find an optimized refractive index distribution of each element to fulfill the design requirements.

Generally, inverse-designed subwavelength nanophotonic devices may be classified into two categories: analog and digital. Because the unit element dimensions of the analog devices are much smaller than those of the digital ones, the etching patterns of analog devices usually have "arbitrarily" curved boundaries [1–4,8,12,14,18], and those of digital ones are normally rectangular- or circular-like shapes [6,7,10,11,13,15–17].

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In general, analog nanophotonic devices offer more degrees of freedom for inverse design at the expense of higher computational and likely fabrication costs, whereas digital nanophotonic devices have a simpler design procedure, easier-to-fabricate patterns, and comparably high performance in various applications. Topology optimization, level-set method, and other gradient-based methods are commonly used for inverse design of analog devices, in which the adjoint method is indispensable to reduce the tremendous ultrafine-element-induced computational cost to a reasonable degree and make the analog inverse design feasible because it could provide the topology or shape gradient information using only a forward and adjoint (backward) simulation regardless of the number of design elements [1-4,8,12,14]. Unfortunately, the conventional adjoint method can be hardly applied to the inverse design of digital devices because one cannot calculate the gradient of a digital pattern. Simple brute-force methods, such as the direct-binary search (DBS) algorithm, have been successfully used for optimization of digital patterns [6,7,10,13,15,16]. However, the number of fully vectorial 3D simulations in brute-force methods will increase exponentially with the pixel number in a pattern, which may drastically limit the inverse design capability of digital nanophotonic devices. Recently, complex fabrication constraints, such as limiting the minimum feature size and maximum curvature of the pattern, have been used to inversely design easy-to-fabricate analog devices based on the adjoint method [3,4], which is usually accompanied by a reduction in design freedom. In addition, artificial neural networks are employed in the inverse design of integrated nanophotonic devices [19–23]. However, it is still a huge challenge to train an artificial neural network, which can effectively replace the real-time optical field simulation for a large-scale device.

In this work, we propose a method for efficient inverse design of digital subwavelength nanophotonic devices based on adjoint sensitivity analysis. For demonstration purposes, the PhC-like subwavelength structure is used as the base nanostructure of digital nanophotonic devices, and its unit element is a silicon cuboid with a central cylinder filled with silicon or air [6]. The inverse design process of the proposed inverse design approach, called the digitized adjoint method, can be divided into three stages. The first stage is geometry-fixed topology optimization. We tune the relative permittivities of all cylinders (i.e., inverse design domain) with a fixed shape continuously and individually and obtain an optimized analog pattern with "gray" cylinders using adjoint sensitivity analysis. In the second stage, we employ a linear-biasing approach to convert the analog pattern in the first stage to a "quasi-digital" one in which the relative permittivities of most cylinders are close to the two boundary values. The optimization process of this stage is the same as the first stage, except that a forced biasing is used to update the cylinders' relative permittivities. In the last stage, we introduce a fabrication-constraint brute-force quantization method to transform the quasi-digital pattern into an N-ary digital pattern, in which intermediate cylinders with different 'gray" relative permittivities in the quasi-digital pattern are replaced with air cylinders with 45 nm radius, silicon cylinders, or air cylinders with N - 2 different radii on the basis of effective medium theory to try to minimize the performance degradation due to the digitalization process. Here, we use a ternary pattern (N = 3) based on a two-level threshold for demonstration.

2. INVERSE DESIGN OF POWER DIVIDER

First, we design a single-mode 3 dB power divider to demonstrate the proposed digitized adjoint method for inverse design under single-objective optimization. To compare with the brute-force method, we choose the same device design parameters as in Ref. [6]. Specifically, the 3 dB power divider has a compact footprint of 2.6 μ m × 2.6 μ m and is discretized into



Fig. 1. Schematic diagram of the single-mode 3 dB power divider (before optimization).

 20×20 pixels for inverse design, as shown in Fig. 1. The device is designed on the 220 nm thick top silicon layer of the silicon-on-insulator (SOI) platform. Each pixel of the PhC-like subwavelength structure is in the shape of a silicon cuboid (130 nm × 130 nm × 220 nm) with a central cylinder with an initial radius of 45 nm and a depth of 140 nm. The depth of air holes in this device is the same as that used in Ref. [6]. The device layout is axisymmetric. The width of input and output waveguides is 500 nm, and the gap between the two output ones is 1 µm. The relative permittivities of air and silicon are set to 1 and 12 in simulations, respectively. Both types of devices were fabricated using an electron-beam lithography system (Vistec EBPG 5000 Plus) to form the optimum pattern on an SOI platform with a 220 nm thick top silicon layer and a 2.0 µm buried oxide layer and an inductively coupled plasma etcher (Plasmalab System 100) to transfer the mask to the silicon device layer based on a single-step etching process.

We define the figure-of-merit (FOM) of the device for inverse design as the transmission into the fundamental transverse electric mode (TE_0) in the two output waveguides, and the transverse magnetic (TM) mode is neglected for simplicity. Because we keep all intermediate patterns axisymmetric, the FOM can be expressed as

$$FOM = \frac{1}{4} \frac{\left| \int_{S} [\mathbf{E}(p') \times \overline{\mathbf{H}_{0}(p')} + \overline{\mathbf{E}_{0}(p')} \times \mathbf{H}(p')] \cdot d\mathbf{S} \right|^{2}}{\int_{S} \operatorname{Re}[\mathbf{E}_{0}(p') \times \overline{\mathbf{H}_{0}(p')}] \cdot d\mathbf{S}}, \quad (1)$$

where *S* is the cross section of the upper output waveguide, p' represents an arbitrary point in *S*, \mathbf{E}_0 and \mathbf{H}_0 represent the electric and magnetic fields of the TE₀ mode, and **E**, **H** denote the actual electric and magnetic fields at *S*, respectively. The overline means complex conjugation.

For a cylinder at position p, a small change of its relative permittivity, $\delta \varepsilon_r(p)$, introduces an electric dipole moment, which leads to a variation of the electromagnetic field at p'. When we change the relative permittivities of all cylinders simultaneously, the total change of electric field at p' will be a superposition of variations caused by all cylinders. Based on the adjoint method for inverse design of analog patterns [1,5], the variation in FOM is given by

$$\delta \text{FOM} = 2\varepsilon_0 V \int_{\chi} \delta \varepsilon_r(p) \text{Re}[\mathbf{E}^A(p) \cdot \mathbf{E}^{\text{old}}(p)] \mathrm{d}^3 p,$$
 (2)

where χ is the design region in all 20 × 20 cylinders with the same and fixed shape, ε_0 is the permittivity of vacuum, V is the volume of a single cylinder, $\mathbf{E}^{\text{old}}(p)$ means the electric field at position p before permittivity change, and $\mathbf{E}^A(p)$ represents the adjoint field at p. Thus, the path to a gradient-based optimization could be reached by updating relative permittivity of each cylinder in iterations as

$$\delta \varepsilon_r(p) = \operatorname{Re}[\mathbf{E}^A(p) \cdot \mathbf{E}^{\operatorname{old}}(p)], \qquad (3)$$

to ensure that δ FOM maintains positive; thus, device performance can be continuously optimized during the iteration process.

In the first stage of the digitized adjoint method, all cylinders are uniformly filled with an intermediate material with a relative permittivity of 6.5, and the other area is filled with silicon in the initial pattern. In each iteration, $\mathbf{E}^{\text{old}}(p)$ and $\mathbf{E}^{A}(p)$



Fig. 2. 3 dB power divider. The optimized (a) analog and (b) quasi-digital patterns in the first and second stages, respectively. (c) The optimized ternary pattern in which the smaller air cylinders with a radius of 35 nm are highlighted in orange. (d) Simulated excess loss profiles for the three patterns. (e) Measured excess loss profiles and (f) the SEM image of the fabricated device based on the ternary pattern. Inset in (e) shows the simulated steady-state intensity distribution.

can be computed from forward and adjoint 3D finite-difference time domain (FDTD) simulations, respectively. Then, we calculate $\delta \varepsilon_r(p)$ for each cylinder based on Eq. (3) and update the relative permittivity of each cylinder through $\varepsilon_r^{\text{new}}(p) =$ $\varepsilon_r^{\text{old}}(p) + \Delta \cdot \delta \varepsilon_r(p)$, where Δ is a variable to control the speed of convergence. The relative permittivity change of each cylinder in each iteration should be small enough to realize reliable adjoint sensitivity analysis based on Eq. (2) derived in the context of perturbation theory. Here, we choose $\Delta = 1/\max{\delta \varepsilon_r(p)}$, and convergence is obtained after 50 iterations. The generated analog pattern is shown in Fig. 2(a), in which the relative permittivity of each cylinder is distributed between 1 and 12.

In the second stage, we convert the analog pattern in the first stage to a quasi-digital one in which the relative permittivities of most cylinders are close to 1 or 12. We use the same adjoint method to calculate the forward field $\mathbf{E}^{\text{old}}(p)$ and adjoint field $\mathbf{E}^{A}(p)$ but update the relative permittivities with a forced biasing in each iteration, expressed as

$$\varepsilon_r^{\text{biased}}(p) = (1+m) \cdot [\varepsilon_r^{\text{new}}(p) - 6.5] + 6.5.$$
 (4)

Here, we set the variable *m* to be 0.05 to slightly enlarge the distance between the relative permittivity and the central value 6.5, which may force the relative permittivity smaller than 1 or larger than 12; further, it will be clipped to be 1 or 12, respectively. This linear-biasing approach is an analogy similar to discrete optimization in the inverse design of analog nanophotonic devices [3], i.e., the inverse design region, which may help to ease the performance degradation caused by discretization of relative permittivities. We calculate the mean square error of the permittivity distribution (σ) in each iteration as

$$\sigma = \frac{1}{M} \sum_{n=1}^{M} \rho_n, \rho_n = \begin{cases} |\varepsilon_r(n) - 1|^2, & 1 \le \varepsilon_r(n) < 6.5\\ |\varepsilon_r(n) - 12|^2, & 6.5 \le \varepsilon_r(n) \le 12 \end{cases},$$
(5)

where *M* is the number of cylinders, and $\varepsilon_r(n)$ is the relative permittivity of the *n*th cylinder. The mean square error decreases significantly from 6.42 to 1.01 after 50 iterations, accompanied by a 0.002 dB increase of excess loss at 1550 nm. Figure 2(b) shows the optimized quasi-digital pattern in the second stage.

In the third stage, the quasi-digital pattern is transformed to an N-ary digital pattern on the basis of effective medium theory. The basic idea is that cylinders with intermediate permittivities and an initial 45 nm radius in the quasi-digital pattern will be replaced with air cylinders with 45 nm radius, air cylinders with an appropriate radius smaller than 45 nm, or silicon cylinders. We use a ternary pattern (N = 3) based on a three-level threshold for demonstration. The range of relative permittivity is divided into three segments with two intermediate values of 3.75 and 9.25. Cylinders with relative permittivities larger than 9.25 or smaller than 3.75 in the quasi-digital pattern will be simply filled with silicon or an air pattern, respectively. Meanwhile, cylinders with relative permittivities between 3.75 and 9.25 are replaced with smaller air cylinders based on a simple brute-force method. We decrease the radius of all smaller air cylinders from 44 to 30 nm with a step of 1 nm and then choose the value corresponding to the best FOM based on 15 rounds of 3D FDTD simulation results. Considering the fabrication constraint, the lower boundary value of the possible radius range is set to 30 nm. Here, the optimized smaller radius is 35 nm. In our simulation, the feature-size-dependent lag effect of RIE etching depth is always considered, and the etching depth of a cylinder with a radius of 35 nm is 124 nm [6]. Figure 2(c) shows the optimized ternary pattern in which the smaller air cylinders with a radius of 35 nm are highlighted in orange. Notably, if smaller quantization errors of intermediate relative permittivities are preferred, we can use the same method to obtain an N-ary digital pattern with N - 2 intermediate radii (smaller than the initial radius) for small air cylinders based on an N-level threshold.

The simulated excess loss profiles of the analog, quasidigital, and ternary patterns are given in Fig. 2(d). The average excess loss over 40 nm bandwidth (1530–1570 nm) is 0.32 dB for the analog pattern, and it increases slightly to 0.33 dB for the ternary digital pattern. The measured excess loss profiles and the scanning electron microscope (SEM) picture of the fabricated 3 dB power divider with the optimized ternary pattern are illustrated in Figs. 2(e) and 2(f), respectively. The measured average excess loss is 0.44 dB with a fluctuation up to 0.40 dB. The unbalance of excess loss between the two output waveguides is 0.36 dB at most and 0.14 dB on average.

3. INVERSE DESIGN OF THE DUAL-MODE DEMULTIPLEXER

We also design a dual-mode demultiplexer to demonstrate the digitized adjoint method for the dual-objective inverse design problem. As shown in Fig. 3, the layout of the dual-mode demultiplexer is the same as that chosen in Ref. [13] for comparison. Specifically, the device has a compact footprint of 2.4 μ m × 3 μ m. The widths of the input and output waveguides are, respectively, 900 and 450 nm. The gap between the two output waveguides is 1.05 μ m. The design region is discretized into 20 × 25 pixels. Each pixel is a cuboid (120 nm × 120 nm × 220 nm) with a central cylinder. The cross-section radius of each cylinder is initially 45 nm, and the depth is set to 220 nm (fully etched).

Here, two FOMs are used for inverse design. One (FOM_1) represents the transmission into the TE_0 in the upper output waveguide when TE_0 is input. The other (FOM_2) represents the transmission into the TE_0 in the lower output waveguide when TE_1 is input.

In the first stage of the digitized adjoint method, each iteration comprises four simulations for two FOMs. The forward and adjoint simulations for each FOM are similar to those in the optimization of a 3 dB power divider, and we first obtain the $\delta \varepsilon_{r1}(p)$ and $\delta \varepsilon_{r2}(p)$ based on the independent



Fig. 3. Schematic diagram of the dual-mode demultiplexer (before optimization).

gradient-based optimizations of two FOMs, respectively. Then, we update the relative permittivity of each cylinder as

$$\varepsilon_r^{\text{new}}(p) = \varepsilon_r^{\text{old}}(p) + \Delta \cdot \frac{1}{2} [\delta \varepsilon_{r1}(p) + \delta \varepsilon_{r2}(p)].$$
 (6)

Here, we set $\Delta = 0.8 / \max\{\delta \varepsilon_r(p)\}\)$, and the convergence of the analog pattern optimization is reached after 100 iterations.

In the second and the last stages, we adopt the same methods used in inverse design of a 3 dB power divider to digitize the analog pattern. Specifically, we obtain the quasi-digital pattern of the dual-mode demultiplexer with $\sigma = 0.54$ after 100 iterations in the linear-biasing adjoint optimization based on Eq. (4). For the optimized ternary pattern, the radius of the small air cylinders is 36 nm.

Figures 4(a)-4(d) show the three types of patterns and the simulated insertion loss and crosstalk profiles of the ternary pattern, respectively. The simulated insertion loss for both modes is 0.68 dB on average, and the crosstalk is less than -25 dB from 1530 to 1570 nm. The simulated and measured performance of a mode-division multiplexing system composed of a dual-mode multiplexer and a demultiplexer based on the ternary pattern is illustrated in Figs. 4(e) and 4(f), respectively. The simulated insertion loss of this mode-division multiplexing system for both modes is 1.36 dB on average, and the crosstalk is less than -20 dB from 1530 to 1570 nm. Further, the measured insertion loss of this mode-division multiplexing system for both modes is 1.51 dB on average, and the crosstalk is less than -18 dB over a bandwidth of 40 nm centered at 1550 nm. The SEM pictures of the fabricated dual-mode demultiplexer and the mode-division multiplexing system are given in Figs. 4(g) and 4(h). A computer with an eight-core CPU (Intel Xeon E5-2637 at 3.5 GHz) and 64 GB memory was employed for simulation. The 3D FDTD simulations were performed via commercial software (Lumerical FDTD Solutions). We also simulated both types of devices using the inverse design methods described in Refs. [6,13] on the same computer for comparison of design efficiency, respectively. A mesh size of 32.5 nm × 32.5 nm × 30 nm was used in the design of 3 dB power divider. In the design of the dual-mode demultiplexer, the mesh size was 30 nm × 30 nm × 30 nm.

4. DISCUSSION AND CONCLUSION

The computation times for the designs of the 3 dB power divider and dual-mode demultiplexer using the digitized adjoint method are about 1.2 and 7 h, respectively. For inverse designs of the two same devices using the conventional DBS method, the time spent on a single optimization process (convergence of the FOM) is approximately 5.5 to 36 h. Meanwhile, the simulated average excess losses over a 40 nm wavelength span (1530–1570 nm) of the 3 dB power dividers designed by the digitized adjoint method and DBS method are 0.33 dB and about 0.2 dB, respectively. For the dual-mode demultiplexer designed by the digitized adjoint method, the simulated insertion loss for both modes is 0.68 dB on average, and the crosstalk is –26 dB from 1530 to 1570 nm, while such two parameters for the multiplexer designed by DBS method are 0.47 dB and less than –24 dB from 1530



Fig. 4. Dual-mode demultiplexer. The optimized (a) analog and (b) quasi-digital patterns in the first and second stages, respectively. (c) The optimized ternary pattern in which the smaller air cylinders with a radius of 36 nm are highlighted in orange. (d) Simulated insertion loss and crosstalk profiles for the ternary pattern. Insets show the simulated steady-state intensity distributions of TE_0 and TE_1 modes, respectively. (e) and (f) Respectively, simulated and measured performance of a mode-division multiplexing system composed of a dual-mode multiplexer and a demultiplexer based on the ternary pattern. (g) and (h) Respectively, SEM images of the fabricated device based on the ternary pattern and the mode-division multiplexing system.

to 1590 nm, respectively. Compared with the brute-force DBS method, the proposed digitized adjoint method could improve the design efficiency by nearly five times, and the performance optimization can reach approximately the same level.

In conclusion, the digitized adjoint method is a hybrid of topology optimization and brute-force optimization to improve the efficiency of inverse design of high-performance digital subwavelength nanophotonic devices. Using the proposed method, we have designed and experimentally demonstrated a singlemode 3 dB power divider and a dual-mode demultiplexer with ternary digital patterns based on a PhC-like subwavelength structure, respectively. Compared with the DBS brute-force method, the digitized adjoint method increases the design efficiency by nearly five times while achieving approximately the same device performance. We expect that the digitized adjoint method can be used to design digital nanophotonic devices based on various types of subwavelength structures different from the PhC-like one. By breaking the efficiency bottleneck of the conventional brute-force method with computational time exponentially increased with the number of pixels and extending the conventional binary pattern to the multilevel pattern, the digitized adjoint method could be applied to the inverse design of large-scale digital subwavelength patterns for exploring digital nanophotonic devices with previously unattainable functionality or higher performance.

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