

PHOTONICS Research

25 Gbps low-voltage hetero-structured silicon-germanium waveguide pin photodetectors for monolithic on-chip nanophotonic architectures

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Near-infrared germanium (Ge) photodetectors monolithically integrated on top of silicon-on-insulator substrates are universally regarded as key enablers towards chip-scale nanophotonics, with applications ranging from sensing and health monitoring to object recognition and optical communications. In this work, we report on the high-data-rate performance pin waveguide photodetectors made of a lateral hetero-structured silicon-Ge-silicon (Si-Ge-Si) junction operating under low reverse bias at 1.55 μm . The pin photodetector integration scheme considerably eases device manufacturing and is fully compatible with complementary metal-oxide-semiconductor technology. In particular, the hetero-structured Si-Ge-Si photodetectors show efficiency-bandwidth products of ~ 9 GHz at -1 V and ~ 30 GHz at -3 V, with a leakage dark current as low as ~ 150 nA, allowing superior signal detection of high-speed data traffic. A bit-error rate of 10^{-9} is achieved for conventional 10 Gbps, 20 Gbps, and 25 Gbps data rates, yielding optical power sensitivities of -13.85 dBm, -12.70 dBm, and -11.25 dBm, respectively. This demonstration opens up new horizons towards cost-effective Ge pin waveguide photodetectors that combine fast device operation at low voltages with standard semiconductor fabrication processes, as desired for reliable on-chip architectures in next-generation nanophotonics integrated circuits. © 2019 Chinese Laser Press

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1. INTRODUCTION

In order to meet the increasing demands of an information-driven society, various levels of communication systems call upon components able to handle dense data streams. Indeed, recently adopted copper-based interconnects, with their inferior electronic and thermal properties, cannot fully satisfy future data traffic requirements of cloud and data center industries in terms of bandwidth, speed, energy consumption, and cost [1–5].

Silicon nanophotonics, notably on silicon-on-insulator (SOI) substrates [5–8], has emerged as a promising platform to overcome deficient data traffic flows in on-chip interconnects [9–11]. In this field, optical photodetectors integrated on an accessible SOI technology are inevitable for myriad applications ranging from optical communications, sensing, or health monitoring to object recognition. However, silicon (Si),

an indirect band-gap semiconductor with a cutoff wavelength of ~ 1.1 μm , is not a reliable material for photodetection at near-infrared (near-IR) wavelengths, i.e., the 1.3–1.55 μm spectral range historically harnessed by optical communication windows of low fiber attenuation and dispersion. To address this deficiency, rather expensive III–V compound semiconductors integrated on SOI wafers via flip-chip bonding or direct heteroepitaxy can be used [11–13]. However, such integration typically comes with added fabrication complexity and possibly some contamination of the Si complementary metal-oxide-semiconductor (CMOS) pilot lines.

As an alternative, germanium (Ge) has appeared as a prime choice for near-IR light detection [14–34]. Ge's appeal comes from high optical absorption, good crystalline quality, and most importantly, a low-cost integration scheme that leverages processes and tools of Si CMOS foundries. Good quality Ge-based

material can be obtained via various growth processes [35–41]. The use of Ge-based alloys can be envisioned in near-IR photodetectors, lasers [42,43], and modulators [44,45]. Such components should ease the monolithic integration of complex functionalities in all group-IV nanophotonic chips, with prospects for nanoelectronics [46], as well.

Various types of waveguide-integrated Ge pin photodetectors have been investigated [17–34] since the early 2000s. The homojunction integration scheme [17–29], where both doping and metal via-contacts are implemented directly on the Ge layer, suffers from deleterious absorption losses, however. The device photo-responsivity, a core requisite for competitive photonic receivers, is then reduced. Additionally, specific Ge technological steps are mandatory to fabricate such structures. Conversely, integration strategies that avoid junction formation on heavily doped Ge regions and the use of metal via-plugs directly on Ge have been proposed and demonstrated [30–34]. Experimental realizations of Si-contacted Ge pin photodetectors have shown convincing device performances, approaching the standards set by III–V epitaxial hetero-structures.

The ideal pin waveguide photodetector should have high responsivity (quantum efficiency), fast response, and reduced power consumption, preferably with an easy to implement process flow available in photonic foundries. Therefore, advanced pin photodetector architectures that are not curtailed by traditional tradeoffs are definitely needed.

In the spirit of our previous proof-of-concept demonstrations [34], we report here on high-data-rate operation of pin waveguide photodetectors with a lateral Si-Ge-Si heterojunction. The butt-waveguide-coupling integration facilitates fabrication and yields improved device performances. In particular, we achieve a low-bias pin photodetector operation, with an efficiency-bandwidth product of ~ 9 GHz at -1 V bias, ~ 30 GHz at -3 V, and a dark-current leakage lower than 150 nA. In addition, the close-up eye diagram shows the ability of Si-Ge-Si photodetectors to preserve high-speed signal transmissions up to 40 Gbps. Last, but not least, a bit-error-free operation, herein reported for the first time, to the best of our knowledge, reaching a level of 10^{-9} is obtained for data rates of 10 Gbps, 20 Gbps, and 25 Gbps, providing received power sensitivities of -13.85 dBm, -12.70 dBm, and -11.25 dBm, respectively.

2. PIN PHOTODIODE DESIGN AND FABRICATION

Figure 1(a) shows a cross-sectional view of the pin waveguide photodetector formed by a lateral (across the horizontal x axis) Si-Ge-Si heterojunction. The Ge pin photodetectors are implemented here on a standard SOI waveguide platform, with 220-nm-thick Si waveguides and 2- μm -thick buried oxide (BOX) layers. The intrinsic Ge (i-Ge) region, serving as an absorption medium, is inherently defined by the thickness and the width ($h_{\text{Ge}} \times w_{\text{Ge}}$) of the Ge layer. As illustrated in Fig. 1(a), the i-Ge region is situated in a cavity (h_{Seed}), with a target thickness of about 60 nm, and laterally sandwiched between two Si slabs, with p-type (p-Si) and n-type (n-Si) dopings, respectively. The whole is positioned at the end of the

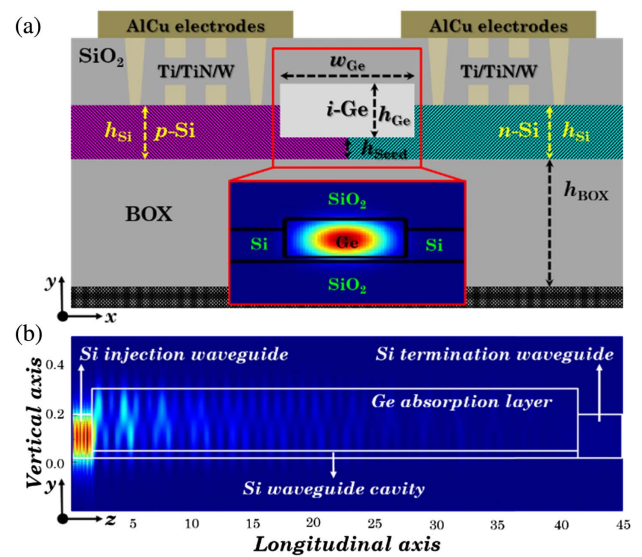


Fig. 1. (a) Transversal schematics (x - y plane) of the pin photodetector with a lateral Si-Ge-Si heterojunction architecture. Inset: electric field profile of the fundamental TE-polarized optical mode in a $0.260\text{-}\mu\text{m}$ -thick and $1\text{-}\mu\text{m}$ -wide hetero-structured photodetector. (b) Longitudinal view (y - z plane) of the optical intensity distribution in the $1\text{-}\mu\text{m}$ -wide and $40\text{-}\mu\text{m}$ -long butt-waveguide-coupled pin Si-Ge-Si photodetector, as obtained from 3D FDTD simulations. The fundamental TE mode is injected from the Si waveguide on the left-hand side.

Si waveguide for butt-coupling injection of light inside the photodetector.

The photodetector transversal dimensions have been optimized to yield the best device performances possible within a compact sub-micrometric area. The resulting device configuration was set to $0.260\ \mu\text{m} \times 1\ \mu\text{m}$ ($h_{\text{Ge}} \times w_{\text{Ge}}$) in order to have an efficient propagation of transverse electrical (TE) modes at C-band (around $1.55\ \mu\text{m}$) wavelengths. As seen in the calculated electric field profile of the fundamental TE mode, shown in the inset in Fig. 1(a), the resulting optical power occupies the Ge area almost completely. More specifically, numerical calculations suggest that a $1\text{-}\mu\text{m}$ -wide intrinsic region provides an excessively large power confinement of up to 87%, while a comparatively low power of only 7% is present in the p-type and n-type doped Si regions. The improved field confinement is facilitated by the enhanced lateral index contrast, i.e., the index difference between the Ge core and the Si-doped regions, as compared to the conventional Ge pin homojunction configuration [17–29]. This optical design reduces the overlap between the evanescent field tails of the fundamental TE mode and lossy Si-doped slabs, substantially decreasing absorption losses from photo-generated carriers in the Si-doped regions. Furthermore, this also enables an efficient coupling of light from the injection Si waveguide into the fundamental TE-polarized mode in the device. The estimated coupling loss between the injection waveguide and the Ge photodetector is -0.61 dB ($\sim 87\%$ of coupling efficiency). Figure 1(b) presents side schematics of the integrated butt-waveguide-coupled pin photodetector with optical intensity distribution, as modeled

with a full-vectorial three-dimensional (3D) finite-difference time domain (FDTD) method [47], along the central plane of the structure. Since the Ge pin photodetector is an extension of the Si waveguide, the optical power is efficiently transferred from the injection waveguide into the i-Ge zone.

The integration strategy, combining butt-waveguide coupling and a lateral pin heterojunction configuration, facilitates the fabrication of compact photodetectors with properly engineered waveguides. Such an approach substantially eases photodetector fabrication and yields improved device performances in terms of photo-responsivity and opto-electrical bandwidth [31,32,34]. In particular, such an approach makes it possible to fabricate the metallic contacts directly on n-type and p-type doped Si, which are robust steps in comparison to metallization on Ge. It should also be mentioned that the very same masking levels and mature manufacturing steps, such as ion implantation in Si, are involved in the fabrication of optical modulators on Si platforms [45], paving the way for monolithic integration of both passive and active photonic components with a significantly reduced number of process steps and thus cost.

The pin photodetectors with a lateral Si-Ge-Si heterojunction were fabricated in CEA-LETI's cleanroom facilities on a fully integrated photonic platform with 200-mm SOI wafers and standard CMOS processes, as detailed in Ref. [34]. First, passive nanophotonic components, including interconnecting waveguides and fiber-to-chip surface grating couplers, were fabricated via 193-nm deep-ultraviolet (deep-UV) photolithography and dry etching. Thermal oxidation was performed to have a SiO₂ cap layer prior to ion implantation. The p-type and n-type Si regions were obtained by boron and phosphorous ion implantation. An oxide cladding was deposited prior to the cavity patterning. Subsequently, the upper oxide was etched down to the Si surface, followed by Si film patterning and deep-rib etching to form cavities with ~60-nm-thick Si floors above the BOX. A more than 1 μm Ge layer was then selectively grown with GeH₄ in those cavities via a 450°C/750°C reduced pressure-chemical vapor deposition (RP-CVD) process, followed by a 1-hour-long annealing at 750°C and chemical mechanical polishing (CMP) to reduce the Ge film thickness down to ~260 nm and recover a flat surface. Afterwards, a few-μm-thick oxide cladding was deposited for Ge passivation and insulation. 400-nm × 400-nm vias were patterned and etched down to Si doped regions. Ni-based silicidation was then conducted to improve contact resistance. At the end, Ti/TiN/W stacks were used as metal plugs. Electrodes consisted of a patterned AlCu layer.

3. DEVICE EXPERIMENTS: RESULTS AND DISCUSSION

A. Static Current-Voltage Measurements

Conventional static current-voltage (I - V) measurements, under dark- and light-illuminated conditions, were performed on the Si-Ge-Si pin photodetectors. More specifically, the light coming from a tunable laser was coupled into the Si chip through a standard single-mode optical fiber (SMF-28). Optical interfacing was realized due to surface grating couplers, optimized for TE polarization and a central wavelength of 1.55 μm. The surface grating couplers were connected to short single-mode Si

strip waveguides, with 220-nm-thick and 500-nm-wide transversal geometry, delivering light into the Ge pin waveguide photodetector through a butt-coupling scheme. The on-chip photodetectors were biased using an electrical probe.

I - V characteristics of the leakage dark current (I_d) and the generated photo current (I_p), in 1-μm-wide × 40-μm-long Si-Ge-Si photodetectors, are shown in Fig. 2(a). Measured devices exhibit low dark currents, 7 nA under low-bias conditions (-1 V) for 5-μm-long devices. The dark current increases monotonously with the device length. The inset in Fig. 2(a) shows dark-current evolution as a function of the device junction area at -1 V bias. The linear trend observed in this

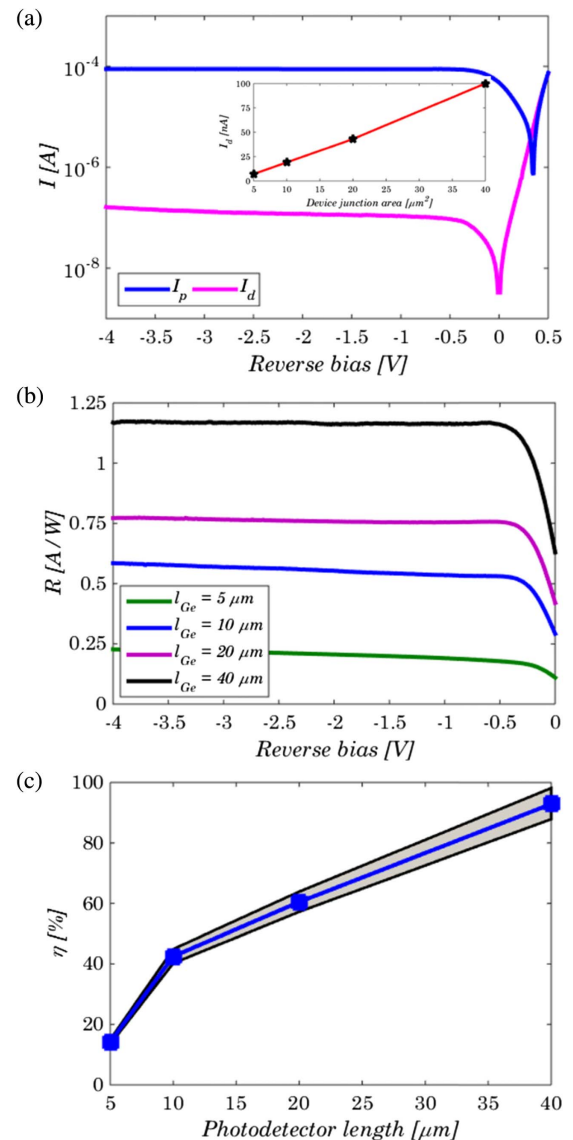


Fig. 2. (a) Static current-voltage (I - V) characteristics of 1-μm-wide by 40-μm-long hetero-structured pin photodetector in dark- and light-illuminated states. Inset: leakage dark-current evolution as a function of device junction area. Photodetectors were biased at -1 V. (b) Photo-responsivity as a function of the reverse voltage for different device lengths. (c) Quantum efficiency as a function of the device length under -0.5 V reverse bias. The shadowed region denotes a range of quantum efficiencies for an estimated power uncertainty of ±0.24 dB.

evolution suggests that the surface leakage is negligible compared to bulk leakage. In addition, the dark currents for 10 μm -, 20 μm -, and 40 μm -long photodetectors are equal to 19 nA, 43 nA, and 100 nA, respectively (for a bias of -1 V). Further increases in reverse voltage yield moderate dark-current increase, up to 150 nA at -4 V for the longest devices. The measured values compare favorably to previous reports on Si-contacted pin waveguide photodetectors [30–34] and are substantially lower than that of pure homojunction devices with micrometric cross-sectional areas [17–29]. Trap-assisted tunneling, dominating at low electric fields, and band-to-band tunneling, which governs carrier generation at moderate/high electric fields, are the main dark-current contributors. In agreement with expectations, hetero-structured Si-Ge-Si pin photodetectors provide leakage dark currents substantially lower than 1 μA [16], making them suitable for high-speed and low-power consumption photonic receivers in established SOI nanophotonic platforms.

The responsivity of the photodetector ($R = I_p/P_i$) was calculated as the ratio between the generated photo current (here, I_p stands for the net-light current, i.e., a photo current without the contribution of the leakage dark current) and the input optical power (P_i). P_i corresponds to the received power that reaches the photodiode, including the insertion loss of the fiber-chip surface grating coupler. The optical power coupled into the waveguide photodetector was estimated to be -11.2 dBm in these measurement conditions. The power uncertainty associated with this estimation is in the range of ± 0.24 dB.

Figure 2(b) shows the photo-responsivity of a 1- μm -wide detector as a function of the reverse voltage for different device lengths. The photodetector responsivities at -1 V for the shortest (5 μm long) and the longest (40 μm long) devices are 0.19 A/W and 1.19 A/W, respectively, among the highest values reported so far for Si-Ge-Si pin photodetectors [30–34]. As shown in Fig. 2(b), the responsivities of Ge pin waveguide photodetectors reach their maxima at bias voltages as low as -0.5 V, one of the lowest reverse biases demonstrated so far. This behavior is consistently observed on all measured devices, independently of the device length. It is also worth highlighting that, beyond a -0.5 V bias, the device responsivity reaches a plateau and remains virtually flat, with negligible voltage dependence. The presence of the strong built-in electrical field at low-bias states demonstrates the outstanding capability of hetero-structured pin photodetectors to sweep out the vast majority of the photo-generated carriers (electron–hole pairs) within their lifetime.

As a consequence, Si-Ge-Si hetero-structured photodetectors have an ultra-high quantum efficiency (η), defined as follows: $\eta = (R \cdot 1.24)/\lambda$, where λ is the operating wavelength of 1.55 μm . As shown in Fig. 2(c), the quantum efficiency increases from $\sim 14.2\%$ for the shortest device (5 μm long) up to $\sim 95\%$ for the longest device (40 μm long) at -0.5 V reverse bias. In other words, this suggests that a 40- μm photodetector is sufficiently long to absorb 95% of the incoming light in the Ge waveguide. In addition, the estimated power uncertainty of ± 0.24 dB results in changes in quantum efficiency, with a maximum range of $\pm 4\%$. This also confirms the superior collection efficiency of lateral pin Si-Ge-Si heterojunction

photodetectors, i.e., the high conversion of incident photons into electrons contributing to the generated photo current.

B. Small-Signal Radio-Frequency Measurements

To assess the opto-electrical bandwidth properties of the hetero-structured Si-Ge-Si photodetectors, we carried out small-signal radio-frequency (RF) measurements. Experiments were performed using a conventional RF-test setup with a light-wave component analyzer (LCA), with an internally built laser and modulator. Similarly to the static I - V measurements, the optical interfacing that delivers the modulated light signal into the Si chip calls upon fiber-chip grating couplers. The pin waveguide photodetectors were reversely biased due to a bias-tee using a Keithley source measurement unit. Prior to testing, the calibrations of the RF path were carried out to take into account the contributions from cables and probes. The small-signal RF experiments were performed by collecting the response of the S_{21} transmission parameter in the LCA tool as a function of frequency.

Figure 3(a) shows a set of S_{21} frequency responses, as retrieved from the small-signal RF measurements performed on a Si-Ge-Si pin waveguide photodetector. The device was probed at various bias states in a range from 0 V to -4 V, using an average optical power coupled to the photodetector of -11 dBm. The cutoff frequency of only ~ 1.8 GHz was measured at a bias of 0 V. Indeed, the opto-electrical bandwidth is limited under the zero-bias state. This is due to the long transit time of carriers. In that case, photo-generated carriers can be efficiently collected only by the built-in electric field, whose strength is, however, relatively weak under such biasing conditions [34].

Those results are also consistent with the observed low responsivity at zero bias. Such a behavior sets practical limits for a zero-bias operation of a hetero-structured Si-Ge-Si photodetector, as compared to pure Ge photodetectors [17–29]. Conversely, with increasing reverse bias, the enhanced electric field present inside the intrinsic Ge zone yields an increase in both the cutoff frequency and responsivity. Specifically, as summed up in Fig. 3(b), the cutoff frequency becomes ~ 13 GHz at -1 V reverse bias, while at -2 V, a ~ 24 GHz bandwidth is reached. For higher reverse biases of -3 V and -4 V, the device opto-electrical bandwidth further increases up to ~ 32 GHz. Comparable trends have been observed for all measured devices. The cutoff frequency of the hetero-structured Si-Ge-Si pin photodetectors becomes roughly independent of the device lengths, as shown in the inset in Fig. 3(a), with a -1 V bias, i.e., the measured bandwidth is not limited by the resistance-capacitance (RC) delay.

Figure 3(c) shows the product of the quantum efficiency and the opto-electrical RF bandwidth, labeled as $\text{QE} \times \text{BW}$, as a function of the reverse bias, for different Ge pin waveguide photodetector lengths. As expected, the highest efficiency-bandwidth product is achieved for the longest photodetector configuration, i.e., with a 40- μm -long i-Ge zone. The efficiency-bandwidth product is around 9 GHz at -1 V and further rises to 30 GHz for a -3 V reverse voltage, with an estimated variation of ± 2.3 GHz for a previously introduced power uncertainty. These achievements show that Si-Ge-Si pin photodetectors are promising to simultaneously have high responsivity and high-speed operation.

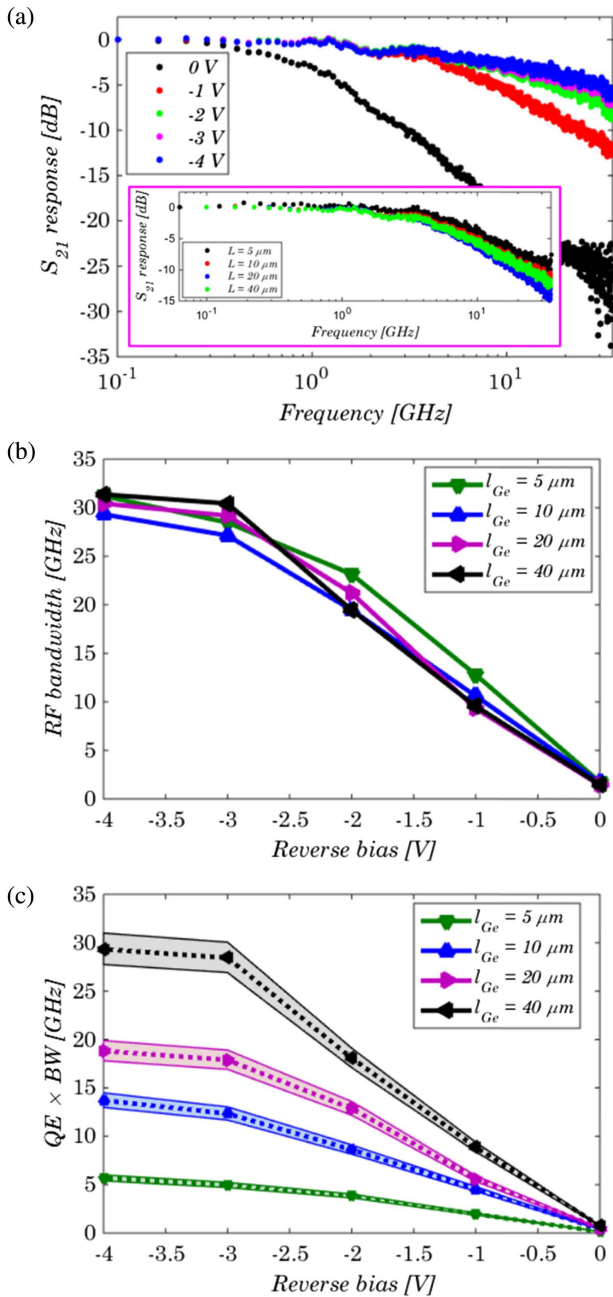


Fig. 3. (a) Small-signal RF measurements of the S_{21} responses of the 1- μm -wide \times 40- μm -long hetero-structured Si-Ge-Si photodetector, under different bias conditions in a range from 0 V to -4 V. Inset: S_{21} RF traces of different length Si-Ge-Si pin waveguide photodetectors biased at -1 V. (b) Opto-electrical bandwidth versus reverse bias for different device lengths. (c) Product of the quantum efficiency by the RF bandwidth versus reverse bias for Si-Ge-Si pin waveguide photodetectors with different lengths. The shadowed regions denote ranges of efficiency-bandwidth product for an estimated power uncertainty of ± 0.24 dB.

C. Large-Signal Data Measurements: Eye-Diagram Acquisitions and Bit-Error-Rate Assessments

The high-speed operation of hetero-structured Si-Ge-Si pin photodiodes was further investigated by performing data detection measurements. Experiments consisted of eye-diagram

large-signal acquisitions and input power sensitivity assessments with bit-error-rate (BER) testing. Data were transmitted in non-return-to-zero (NRZ) optical modulation format. The pseudo-random-binary-sequence (PRBS) data pattern $2^7 - 1$ was considered for different rates of 10 Gbps, 20 Gbps, 25 Gbps, 28 Gbps, 32 Gbps, and 40 Gbps. The externally modulated laser wavelength was 1.55 μm . The transmitted signal was amplified with an erbium-doped fiber amplifier (EDFA), followed by an optical filter to reduce spontaneous emission noise. The average optical power was controlled due to a variable optical attenuator and an in-line power meter. Optical TE polarization was adjusted with a polarization controller to optimize the intensity of the detected signal. The modulated signal was sent into the Si chip due to a surface grating coupler, followed by on-chip detection in the hetero-structured Si-Ge-Si pin photodetector, without the use of an integrated trans-impedance amplifier (TIA) or on-chip limiting amplifier (LA). Electrical data were retrieved through the RF setup previously used for small-signal RF testing, by applying the reverse bias to the photodetector with the use of an RF probe connected to a bias tee. Data were directly sent from the RF bias-tee output to a high-speed sampling oscilloscope, depicting eye diagrams. BER assessments were performed by inserting an external 38-GHz broadband electrical amplifier between the RF bias-tee output and the BER detection module,

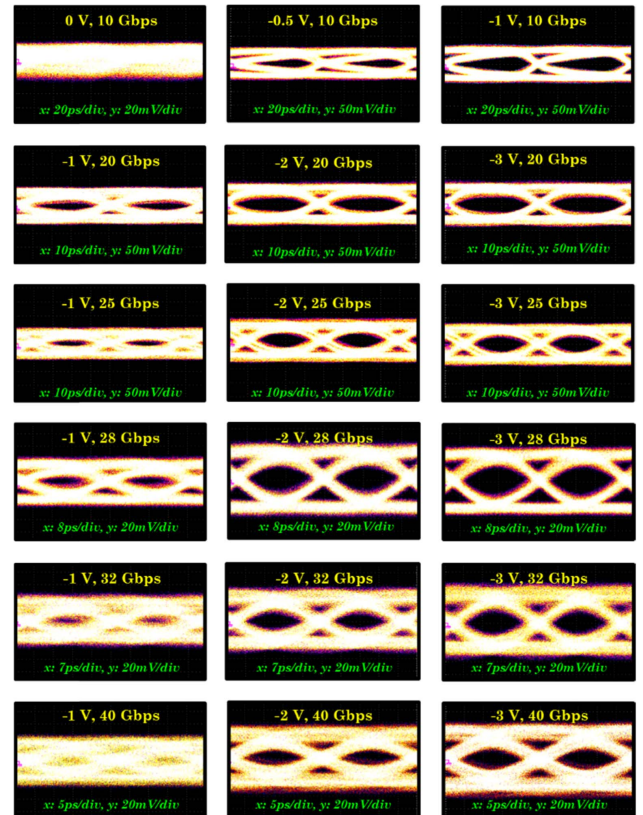


Fig. 4. Evolution of eye diagram apertures within a low-reverse-bias range at 10 Gbps, 20 Gbps, 25 Gbps, 28 Gbps, 32 Gbps, and 40 Gbps. Here, x [ps/div] and y [mV/div] correspond to the horizontal and vertical scope axes within the particular measurement setting. 1- μm \times 40- μm (Ge width \times Ge length) Si-Ge-Si photodetector.

whose minimum level requirement was 100 mV peak-to-peak signal voltage. The measured eye diagrams and BER, for different transmission rates and various bias conditions, are shown in Figs. 4 and 5, respectively. Large-signal data testing was carried out in a $1\text{-}\mu\text{m} \times 40\text{-}\mu\text{m}$ (Ge width \times Ge length) Si-Ge-Si photodetector.

In agreement with small-signal RF measurements, the eye diagram is closed at 0 V bias, as shown in Fig. 4 for a 10-Gbps data rate. This behavior was also observed for other transmission rates. A reverse bias increase (-0.5 V and -1 V at 10 Gbps line rate) results in a clear opening of the eye diagram, because of the generated electrical field within the intrinsic region, as explained previously. Clearly opened eye diagrams are obtained for conventional data rates of 10 Gbps, 20 Gbps, and 25 Gbps, with reverse voltages of -1 V, -2 V, and -3 V,

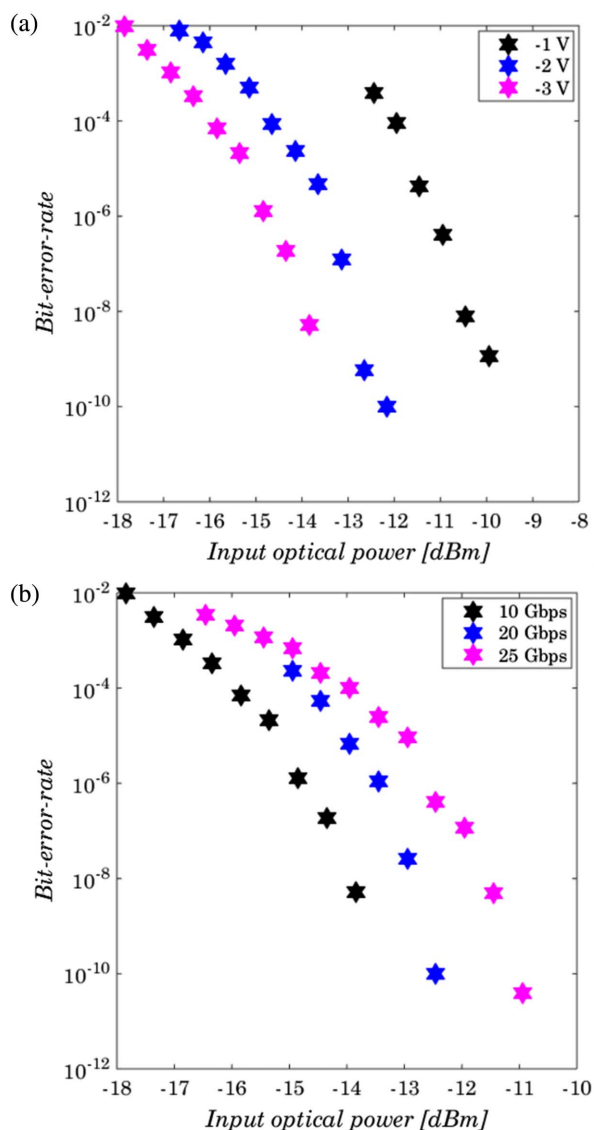


Fig. 5. Bit-error-rate measurements of the Si-Ge-Si pin waveguide photodetector as a function of the input optical power. BER assessments performed (a) at 10 Gbps under low-reverse-bias states and (b) at 10 Gbps, 20 Gbps, and 25 Gbps, all biased at -3 V. $1\text{-}\mu\text{m} \times 40\text{-}\mu\text{m}$ (Ge width \times Ge length) Si-Ge-Si photodetector.

enabling BER examination. Additionally, eye diagram apertures also suggest that high-speed signal detection is potentially achievable from -2 V biasing up to 40 Gbps data speeds. The restricted photodetector bandwidth at -1 V bias explains why eye diagrams are closing, as the data rate increases. Yet, the voltage adjustment possibility preserves high-bit-rate signal detection capability up to 40 Gbps.

Figure 5(a) shows BER measurements as a function of the received optical power for a 10 Gbps data rate, under -1 V, -2 V, and -3 V bias conditions. Optical power sensitivities, defined as yielding a 10^{-9} BER, are equal to -9.95 dBm, -12.75 dBm, and -13.85 dBm for those biases. Figure 5(b) shows the measured BER for transmission data rates of 10 Gbps, 20 Gbps, and 25 Gbps under -3 V bias. BER 10^{-9} optical power sensitivities of -13.85 dBm, -12.70 dBm, and -11.25 dBm are associated with those data rates. It is worth noting that the low induced penalty measured when the bit rate increases from 10 Gbps up to 20 Gbps is attributed to the fact that sensitivity at 10 Gbps should be lower with a better suited electrical error detection chain with a much lower bandwidth. Lower peak-to-peak signal voltage requirements at the error detection module input should decrease sensitivity values as well.

4. CONCLUSION

In summary, we have experimentally shown that pin waveguide photodetectors with lateral Si-Ge-Si junctions have superior performances when operating under low reverse bias at $1.55\text{ }\mu\text{m}$. The devices strongly benefit from the combination of butt-waveguide coupling with lateral Si-Ge-Si pin junctions, resulting in compact devices with a definitely reduced fabrication complexity and substantially improved performances. More specifically, hetero-structured pin waveguide photodetectors yield efficiency-bandwidth products of ~ 9 GHz at -1 V, ~ 30 GHz at -3 V, and dark-currents lower than 150 nA. Eye diagram inspections confirm that Si-Ge-Si pin photodetectors enable a detection of high-speed signals up to 40 Gbps. A bit-error-free operation of 10^{-9} is achieved for data rates of 10 Gbps, 20 Gbps, and 25 Gbps, with optical power sensitivities of -13.85 dBm, -12.70 dBm, and -11.25 dBm, respectively. This demonstration holds promising prospects for the development of high-speed, energy-efficient, and low-cost photodetectors at the chip scale, which ultimately could usher in a future generation of Si nanophotonic architectures in optical integrated circuits.

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