PHOTONICS Research

High-performance AlGaInP light-emitting diodes integrated on silicon through a superior quality germanium-on-insulator

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High-performance GaInP/AlGaInP multi-quantum well light-emitting diodes (LEDs) grown on a low threading dislocation density (TDD) germanium-on-insulator (GOI) substrate have been demonstrated. The low TDD of the GOI substrate is realized through Ge epitaxial growth, wafer bonding, and layer transfer processes on 200 mm wafers. With O_2 annealing, the TDD of the GOI substrate can be reduced to $\sim 1.2 \times 10^6$ cm^{-2}. LEDs fabricated on this GOI substrate exhibit record-high optical output power of 1.3 mW at a 670 nm peak wavelength under 280 mA current injection. This output power level is at least 2 times higher compared to other reports of similar devices on a silicon (Si) substrate without degrading the electrical performance. These results demonstrate great promise for the monolithic integration of visible-band optical sources with Si-based electronic circuitry and realization of high-density RGB (red, green, and blue) micro-LED arrays with control circuitry.

OCIS codes: (230.3670) Light-emitting diodes; (130.5990) Semiconductors; (160.6000) Semiconductor materials.

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1. INTRODUCTION

Micro-LEDs are a promising candidate for the next-generation display technology for smart lighting, Internet of Things (IoT), wearables, and augmented-reality devices [1]. For full-color display applications, white LED backlights with red, green, and blue (RGB) filters are the most commonly used light sources. The preferable scheme to form one pixel is to use separate red, green, and blue LEDs. The pixel is formed either via direct emission of the desired primary color wavelengths, or by using blue LEDs optically pumping red and green phosphors to generate the latter two colors [2,3]. The problems associated with these technologies are the relatively large pixel pitches and form factors due to challenges in assembling the multiple color LEDs into RGB pixels, as well as in addressing them and connecting them to the electronic driver circuits. This makes them unsuitable for applications requiring high-density micro-LED arrays. To address this limitation, it is preferable to monolithically integrate red, green, and blue LEDs with Si-CMOS control circuitry in a single die through a scalable integrated circuits manufacturing process.

We have successfully demonstrated the integration of Si-CMOS and III–V materials on a common 200 mm Si platform through our well-established wafer bonding process [4,5]. Recent developments in epitaxy of InGaN blue and green LEDs on Si (111) substrates are promising [6]. However, the red LEDs rely on lattice-matched gallium arsenide (GaAs) substrates. The large lattice-mismatch between GaAs and Si makes the direct growth of the red LEDs on Si substrates a challenge [7], where red LEDs typically are of low brightness due to the high threading dislocation density (TDD) generation. The highest reported output optical power density of red LEDs on a Si substrate is 0.53 mW/mm^2, achieved through the use of SiGe buffers [7,8].

To minimize the effect of the lattice mismatch, our group has successfully demonstrated the direct epitaxial growth of Ge-on-Si (Ge/Si) with a TDD of $\sim 5 \times 10^6$ cm^{-2} [9,10].

Since the minority carrier lifetime is sensitive to TDDs [11], to further reduce the TDD, we have developed an engineered germanium-on-insulator (GOI) on Si substrate with a TDD reduced to ~1.2×10^6 cm^{-2} by wafer bonding and layer transfer techniques.

In this work, we explore the formation of the GOI substrate with low dislocation density. Red color GaInP/AlGaInP multi-quantum well (MQW) LEDs are then grown and fabricated on the engineered GOI substrates and characterized. We also fabricate similar devices on commercially available Ge/Si and bulk Ge substrates for comparison.

2. EXPERIMENTAL DETAILS

A. Fabrication of GOI Substrates

The GOI substrate was fabricated through epitaxy, bonding, and layer transfer processes. The Ge epitaxial film was grown directly (bufferless) on a 200 mm Si (001) donor wafer with 6° off-cut towards the [110] direction by a two-step growth approach and followed by *in situ* thermal cyclic annealing in a metal-organic chemical vapor deposition (MOCVD) system [12,13]. After that, a SiO_2 layer was deposited on both Ge/Si donor and Si (001) handle wafers by plasma-enhanced chemical vapor deposition (PECVD). Prior to bonding, both wafers were subjected to O_2 plasma exposure, rinsed with deionized water, and then spin-dried. The two wafers were then bonded together and annealed at 300°C to enhance the bond strength. Subsequently, the Si from the Ge/Si donor wafer was removed to realize the initial GOI substrate. The GOI substrate was then annealed at temperatures between 700°C–850°C in O_2 ambient for several hours. After that, the sample was dipped in a diluted hydrofluoric acid solution to remove the oxidized Ge layer. Lastly, the Ge surface, which was roughened during the high-temperature annealing step, was smoothened by chemical mechanical planarization (CMP) to realize the high-quality GOI substrate. The overall process flow is shown schematically in Fig. 1.

B. Growth and Fabrication of AlGaInP LED

GaInP/AlGaInP LED structures were then grown on the GOI substrates. A GaAs buffer layer was initiated on the Ge surface

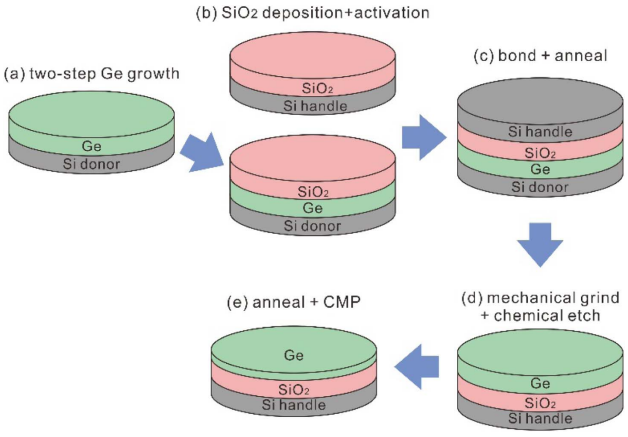

Fig. 1. Schematic flow of the fabrication of germanium-on-insulator (GOI) substrates with low threading dislocation density (TDD). All substrates are 200 mm in diameter.

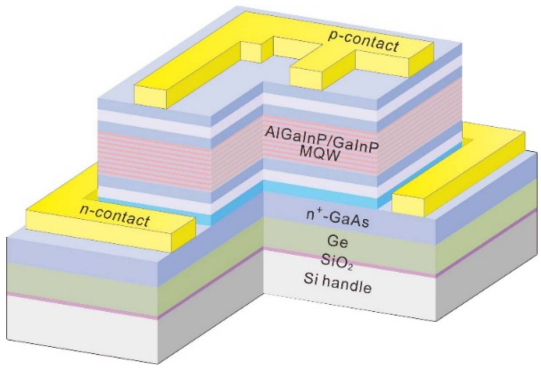

Fig. 2. Schematic layout and layer structure of $(Al_{0.3}Ga_{0.7})_{0.51}In_{0.49}P/Ga_{0.51}In_{0.49}P$ multi-quantum well (MQW) LEDs on a GOI substrate.

using our optimized GaAs-on-Ge growth conditions [14]. A one-λ thick AlGaInP optical cavity was grown, which consists of 10 periods of $Ga_{0.51}In_{0.49}P/(Al_{0.3}Ga_{0.7})_{0.51}In_{0.49}P$ MQWs surrounded by AlGaInP set-back layers and followed by n- and p-AlGaInP spacer layers. For comparison, commercially available Ge/Si and bulk Ge substrates were included in the same growth. The wafers were processed into devices with mesa dimensions ranging from 100 μm × 100 μm to 1 mm × 1 mm by photolithography and a wet etch process. Ni/Ge/Au/Ni/Au annealed at 380°C for 30 s, and unannealed Ti/Au were used as the n-type and p-type contacts, respectively. The device structure is shown schematically in Fig. 2.

3. RESULTS AND DISCUSSION

A. Characterization of the GOI Substrate

Etch pit density (EPD) measurements were used to determine the TDD of the Ge epitaxial films before MQW growth. As shown in Fig. 3(a), the EPD of our GOI substrate before O_2 annealing is $(5.80 \pm 0.57) \times 10^8$ cm^{-2}; this value is significantly reduced by the O_2 annealing and CMP processes. The misfit dislocations, which were previously mostly confined close to the Ge/Si interface, were exposed and accessible from the top of the GOI substrate after the layer transfer. The exposed misfit dislocations could then be removed by the CMP and/or annealing. The EPD of the GOI substrate is reduced by more than two orders of magnitude to $(1.20 \pm 1.37) \times 10^6$ cm^{-2} after O_2 annealing and CMP processes as depicted in Fig. 3(b), which is more than 1 order of magnitude lower compared to commercial Ge/Si with EPD of $(5.78 \pm 0.57) \times 10^7$ cm^{-2}, as shown in Fig. 3(c).

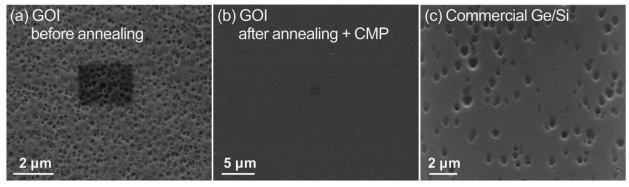

Fig. 3. Etch pit density (EPD) determination for (a) GOI substrate after layer transfer, (b) GOI substrate after O_2 annealing and CMP processes, and (c) commercially available Ge/Si substrate.

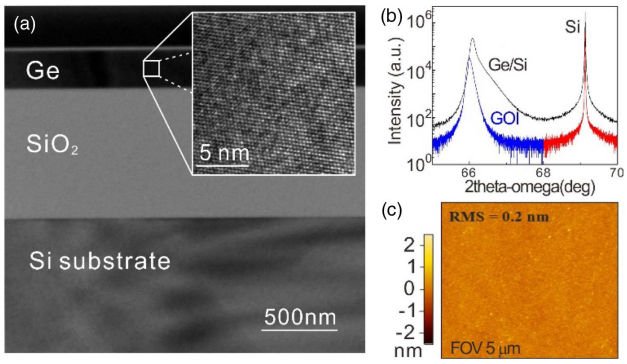

Fig. 4. Characteristics of the GOI substrate after O_2 annealing and CMP processes. (a) Cross-sectional transmission electron microscopy (X-TEM) bright field image of the GOI substrate; inset is a high-resolution TEM image of the Ge layer. (b) HRXRD curves of the commercial Ge/Si and our GOI substrates. The Ge signal curve is symmetric, which suggests that the intermixed $Si_{1-x}Ge_x$ material near the Ge/Si interface was removed after the annealing. (c) A 5 μm × 5 μm atomic force microscopic scan of the GOI substrate. The RMS roughness is ~0.2 nm.

No misfit or threading dislocations were observed in the cross-sectional transmission electron microscopy (X-TEM) image of the GOI substrate after O_2 annealing, as shown in Fig. 4(a), suggesting that the TDD of the GOI sample was greatly reduced. O_2 annealing was chosen because: (i) the Si/Ge intermixed layer and part of the Ge layer could be oxidized, thereby removing misfit dislocations; (ii) threading dislocations could be annihilated once the misfit dislocations were eliminated; and (iii) high-temperature annealing could re-crystallize the Ge epitaxial film with high crystalline quality. The high-resolution X-ray diffractometry (HRXRD) curves shown in Fig. 4(b) confirm that the intermixed $Si_{1-x}Ge_x$ material was totally removed after the annealing process, and only pure Ge remained. The root mean square (RMS) surface roughness of the Ge epilayer after CMP is ~0.2 nm, and no cross-hatch patterns are observed, as shown in Fig. 4(c). Table 1 shows the comparison of different Ge/Si substrate fabrication techniques, and our approach is competitive with thin Ge buffer thickness and low surface roughness while maintaining a low dislocation density.

Table 1. Quality of Ge Epitaxial Films on Si Substrates Using Different Approaches

	SiGe Graded Buffer [15]	Selective Epitaxial Growth (SEG) [16]	Two-Step Growth Approach [13]	This Work
Ge thickness (μm)	12	~1	1	0.6
Dislocation density (cm^{-2})	2.1×10^6	$\sim 1 \times 10^6$	$\sim 5 \times 10^7$	$\sim 1 \times 10^6$
RMS surface roughness (nm)	24.2	NA (undulated surface)	1–2	0.2 (CMP)

B. Characterization of AlGaInP LEDs

Figure 5 shows X-TEM images of MQWs grown on commercial Ge/Si and our GOI substrates. For the MQW structures that were grown on the commercial Ge/Si substrate, clear threading dislocations are observed on the Ge layer, which propagate through the n^+ GaAs layer and are observed in the p^+ AlGaInP spacer. In contrast, dislocation-free layers are observed for MQW structures that were grown on our GOI substrate.

Figure 6 shows the measured I–V curves of LEDs fabricated on three different substrates. High leakage current was observed for the LEDs fabricated on a commercial Ge/Si substrate. The ideality factors of the LEDs on bulk Ge, commercial Ge/Si, and our GOI substrates at high voltages calculated by linear curve fitting are 1.207, 1.494, and 1.308, respectively, before reaching the high current injection region that is characterized by series resistance roll-off. This confirms the good material quality of the epilayers grown on our GOI substrate compared to the commercial Ge/Si substrate, due to the lower TDD.

Figure 7(a) shows the normalized room-temperature photoluminescence (PL) spectra of the LEDs grown on various substrates under the same excitation power. The peak wavelengths of the LEDs fabricated on our GOI and the commercial Ge/Si substrates are around 667 nm. The minor shift of peak wavelength of LEDs fabricated on the Ge substrate is due to different strain levels in the device epilayers and different relaxation states of the starting Ge layers. Figure 7(b) shows the electroluminescence (EL) spectra of the LEDs fabricated on various substrates, measured under an injection current of 20 mA. The full width at half-maximum (FWHM) of the emission spectra for the LEDs on the Ge, our GOI, and the commercial Ge/Si substrates is 17, 19, and 20 nm, respectively. Superior high emission intensity is observed for the LEDs fabricated on our GOI substrate compared to on the Ge and the commercial Ge/Si substrates, suggesting that high-quality AlGaInP

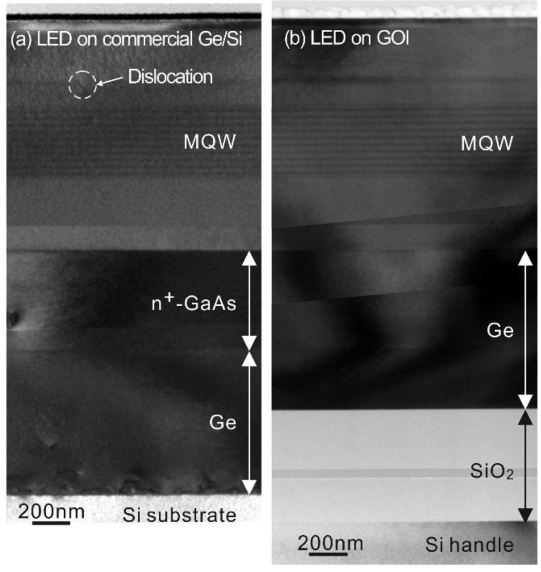

Fig. 5. X-TEM bright field images showing LEDs grown on (a) a commercial Ge/Si substrate and (b) our GOI substrate after it had been subjected to O_2 annealing and CMP processes.

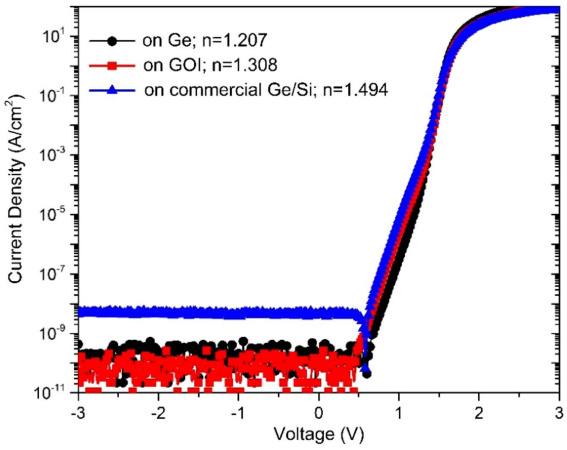

Fig. 6. *I–V* characteristics for LEDs on bulk Ge, our GOI, and commercial Ge/Si substrates, with mesa size of 600 μm × 600 μm. The ideality factor for the LEDs on Ge, GOI, and commercial Ge/Si is 1.207, 1.308, and 1.494, respectively.

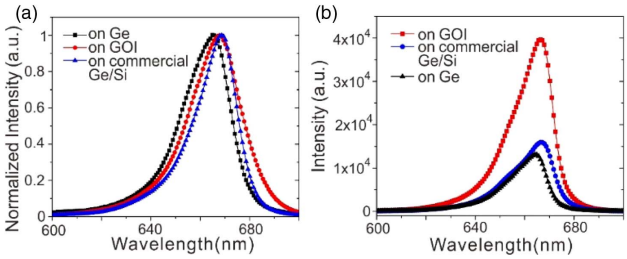

Fig. 7. (a) Room-temperature photoluminescence (PL) spectra (with input laser power of 20 mW) and (b) electroluminescence (EL) spectra (with injection current of 20 mA) of the LEDs grown on three different substrates.

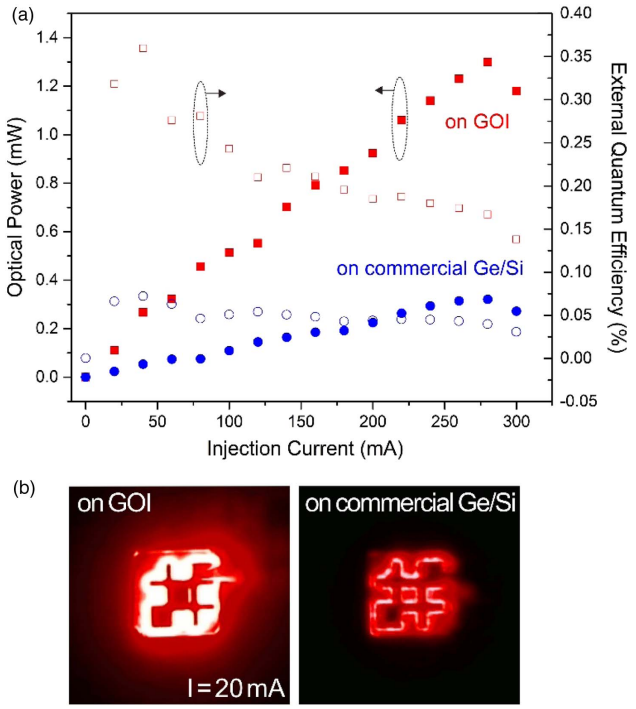

Fig. 8. (a) Optical output power (L–I) and external quantum efficiency (EQE) of LEDs grown on commercial Ge/Si and our GOI substrates measured by an integrating sphere that is 1 m in diameter. (b) Optical images of emitting 100 μm × 100 μm LEDs on the commercial Ge/Si and our GOI substrates under a continuous injection current of 20 mA.

MQW films have been grown on the GOI substrate. A relatively low emission intensity is observed for LEDs fabricated on the Ge substrate. This is because of the introduction of a small amount of indium during the growth to compensate for the 0.08% lattice mismatch between GaAs and Ge, using a process optimized for GOI and Ge/Si substrates. However, this small amount of indium causes undesired stress build-up and generates new dislocations on the device layers that were grown on the bulk Ge substrate.

Figure 8 shows the optical output power (L–I) measured by a 1 m diameter integrating sphere setup. The optical output power of the LED on the bulk Ge substrate was below the measurement range of the setup. A maximum output power of 1.3 mW under 280 mA of injection current was obtained for 1 mm × 1 mm size LEDs on our GOI substrate. The output power is at least 2 times higher compared to other reports in the literature as shown in Table 2, and 4 times higher than the LED grown on the commercial Ge/Si substrate. This is attributed to the low density of threading dislocations in the MQW structures grown on our GOI substrate. TDDs act as nonradiative recombination centers and cause carrier scattering, which hinders the light output of LEDs. Despite the improved performance, the external quantum efficiency remains low due to the presence of the absorbing Si substrate. Higher output power can be realized through improving the light extraction efficiency, such as surface roughening [17], substrate removal [18], and incorporating distributed Bragg reflectors (DBRs) [19].

The internal quantum efficiency of the LED depends on the junction temperature. The junction temperature of the LEDs can be calculated from the PL spectrum emission intensity by the following equations [20,21]:

$$I(E) \propto (E - E_g)^{1/2} \exp\left(-\frac{E - E_g}{k_B T}\right). \quad (1)$$

The maximum emission intensity occurs at $E_g + \frac{k_B T}{2}$, and therefore, the FWHM can be extracted as

$$\Delta E = 1.8 k_B T, \quad (2)$$

where E is the energy state, E_g is the energy bandgap, k_B is the Boltzmann constant, and T is the junction temperature. Figure 9 shows the junction temperature versus peak emission wavelength of the LEDs fabricated on different substrates calculated based on FWHM of the measured PL spectrum. In general, the increase of the excitation laser power leads to the redshift of peak emission wavelength with a broader FWHM, and thus a higher junction temperature based on Eq. (2). The LED fabricated on our GOI substrate exhibits a lower junction temperature compared to the LED on the Ge substrate, which has a much lower TDD than on our GOI substrate. This is mainly due to the large thermal conductivity difference between

Table 2. Performance of Red LEDs on Si Substrates from Literatures

	Bao *et al.* [22]	Chulukuri *et al.* [8]	Kwon *et al.* on Ge [7]	Kwon *et al.* on SiGe Graded Buffer [7]	This Work
Number of quantum wells	5	1	4	4	10
DBR	No	No	Yes	Yes	No
Output power (mW/mm^2)	<0.1	0.00175	0.327	0.531	1.3
Ideality factor	NA	NA	1.95	1.95	1.308

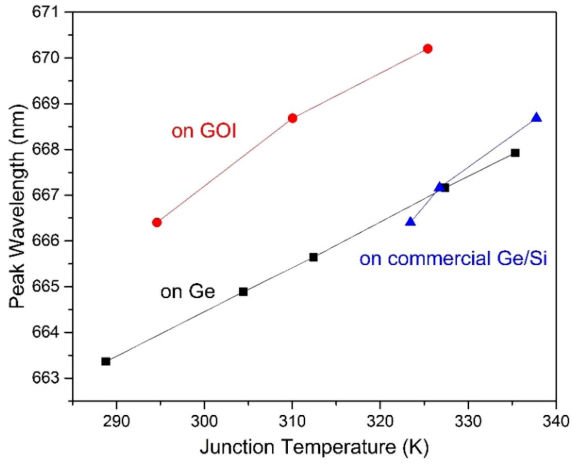

Fig. 9. Junction temperature versus peak emission wavelength of LEDs grown on different substrates.

the silicon ($1.3\ W \cdot cm^{-1} \cdot C^{-1}$) and Ge ($0.58\ W \cdot cm^{-1} \cdot C^{-1}$) substrates, even with the addition of thin dielectric layers between the Ge film and Si substrate. Although Si substrate was used as the bottom substrate of the commercial Ge/Si wafer, the performance of the LED fabricated on the commercial Ge/Si substrate suffers severely from the high junction temperature. This is because of the heat generated in the active region originated from the nonradiative recombinations at the dislocation sites [22]. The LED operating at high temperatures leads to a shortened device lifetime.

Reliability tests have also been conducted on the LEDs grown on GOI and commercial Ge/Si substrates. The LEDs on our GOI substrate demonstrate longer lifetimes (>100 h) than the LEDs on the commercial Ge/Si substrate (52 h) after the LEDs were stressed at 200 A/cm^2 at room temperature as shown in Fig. 10. Catastrophic failures were observed for LEDs on the commercial Ge/Si substrate. This shortened lifetime could be associated with the high dislocation densities in LEDs grown on commercial Ge/Si, compared to the LEDs on our GOI substrate. The dislocations are mainly from the propagation of defects present in the starting substrate into the LED device layers. During LED operation, heat generated in the

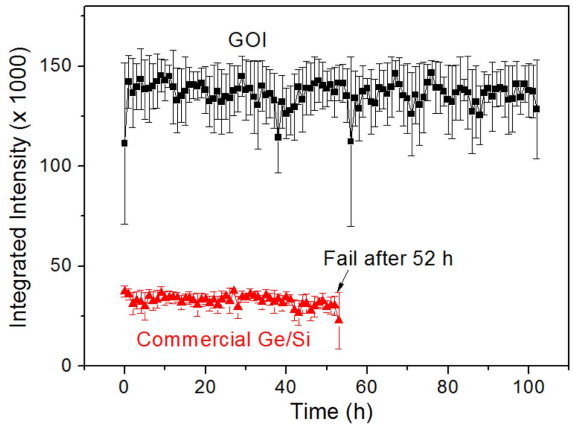

Fig. 10. Reliability of LEDs on commercial Ge/Si and our GOI substrates under a stressing condition of 200 A/cm^2 at room temperature.

active region causes the propagation of the defects through the device layers, forming a network of nonradiative regions (e.g., dark line defects), which leads to the degradation of the LED and causes catastrophic failure through a feedback mechanism [23].

With the demonstration of high-performance red LEDs grown on our superior-quality GOI substrates, we are able to realize red LEDs that can be operated and controlled by inexpensive Si-CMOS control circuitry as shown in Fig. 11(a). In addition, through the multiple wafer bonding and layer transfer technique, RGB micro-LED arrays can be achieved as shown in Fig. 11(b). Through controlling the Si-CMOS control circuitry, the on/off state and the intensity of the

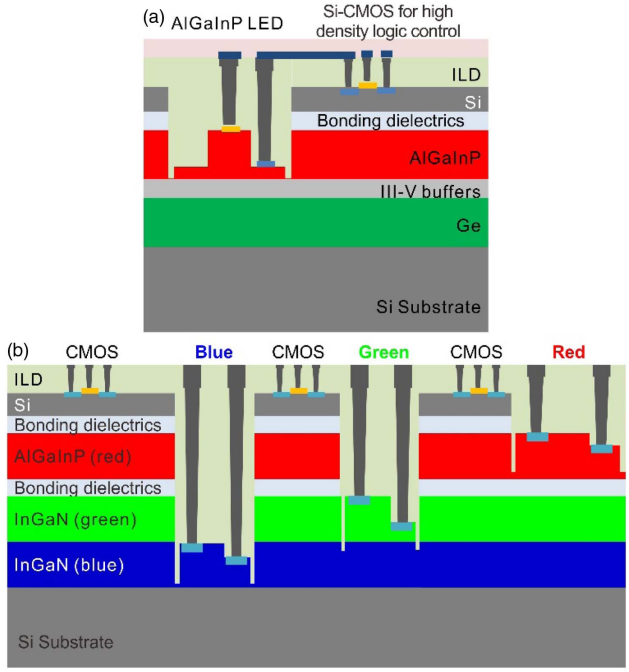

Fig. 11. Schematics show the integration of (a) Si-CMOS and red LEDs, and (b) red, green, and blue LEDs with Si-CMOS control circuitry through multi-wafer bonding and layer transfer processes.

respective LEDs can be controlled, and hence various colors can be visualized.

4. CONCLUSION

High-quality 200 mm GOI substrates with a TDD of 1.2×10^6 cm^{-2} have been successfully achieved though layer transfer, high-temperature oxygen annealing, and CMP processes. The high-quality GOI substrates enable minority carrier devices on Si substrates. For demonstration purposes, visible 670 nm AlGaInP/GaInP LEDs were grown and fabricated on GOI substrates. High-performance red LEDs with a record-high output power of 1.3 mW were demonstrated for the first time on Si substrates. This performance can be further improved by optimizing the growth structure and fabrication steps, such as inserting distributed Bragg reflectors, enhanced current spreading layers, Si_3N_4 passivation layers for minimizing leakage currents, and replacing the absorbing substrate with transparent substrates (such as quartz). These results on large-area 200 mm Si substrates serve as a pathway to enable monolithic integration of visible-band optical sources with Si-based electronic circuitry. This will allow the realization of high-density RGB (red, green, and blue) micro-LED arrays with Si-CMOS control circuitry on a single Si platform, which will see use in various applications and products that require small form factor displays.

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