Photonic integrated circuit components based on amorphous silicon-on-insulator technology

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Received March 2, 2016; revised April 1, 2016; accepted April 7, 2016;
posted April 8, 2016 (Doc. ID 260153); published May 11, 2016

We present integrated-optic building blocks and functional photonic devices based on amorphous silicon-on-insulator technology. Efficient deep-etched fiber-to-chip grating couplers, low-loss single-mode photonic wire waveguides, and compact power splitters are presented. Based on the sub-μm photonic wires, 2 × 2 Mach–Zehnder interferometers and add/drop microring resonators (MRRs) with low device footprints and high finesse up to 200 were realized and studied. Compact polarization rotators and splitters with ≥10 dB polarization extinction ratio were fabricated for the polarization management on-chip. The tuning and trimming capabilities of the material platform are demonstrated with efficient microheaters and a permanent device trimming method, which enabled the realization of energy-efficient photonic circuits. Wavelength multiplexers in the form of cascaded filter banks and 4 × 4 routers based on MRR switches are presented. Fabrication imperfections were analyzed and permanently corrected by an accurate laser-trimming method, thus enabling eight-channel multiplexers with record low metrics of sub-mW static power consumption and ≤1°C temperature overhead. The high quality of the functional devices, the high tuning efficiency, and the excellent trimming capabilities demonstrate the potential to realize low-cost, densely integrated, and ultralow-power 3D-stacked photonic circuits on top of CMOS microelectronics.

OCIS codes: (130.0250) Optoelectronics; (130.7408) Wavelength filtering devices; (200.4650) Optical interconnects; (220.4241) Nanostructure fabrication; (230.3120) Integrated optics devices; (230.5750) Resonators.
http://dx.doi.org/10.1364/PRJ.4.000126

1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) provides a versatile and low-loss integrated-optic material platform for high index contrast (HIC) photonic circuits. The HIC of $\Delta n \geq 2$, the low absorption loss ≤0.5 dB/cm at the telecommunication bands 1.3–1.55 μm [1,2], and the flexible fabrication capabilities make amorphous silicon-on-insulator (a-SOI) highly attractive for a variety of integrated optic applications. In principle, the material shares the two major advantages of crystalline silicon (c-SOI), which are the high integration density and compatibility to mature complementary metal-oxide semiconductor (CMOS) technology; the almost identical refractive index facilitates the adaptation of existing SOI designs and manufacturing processes.

However, a sharp distinction is evident in the integration approaches: for instance, to realize photonic-electronic-integrated-circuits (PEICs). Whereas c-SOI is first choice for front-end-of-line (FEOL) integration with microelectronics, it does not provide the same flexibility for the integration on top of the microchips at the back-end-of-line (BEOL). Compared with that, it is not practicable to integrate low-loss a-Si:H with FEOL processes because the optical properties start degrading at elevated temperatures ($T \geq 350$°C–400°C) due to dehydrogenation. On the other hand, a-Si:H emphasizes excellent fabrication capabilities to be integrated in multiple layers at the BEOL, including the possibility to integrate FEOL photonics by optical vias. Notwithstanding the limited electrical properties of intrinsic a-Si:H, significant progress has been reported for active photonic devices, e.g., based on pn-doping and/or crystallization [3–7], by deposition on electro-optic substrates [8,9], or all-optically employing the high nonlinear figure of merit [10–12]. Further integration potential includes BEOL-compatible inorganic (AlN, Al_2O_3, SiN, TiO_2, etc.) [13–16], III-V [17–19], and polymer/plasmonic materials [20–22], unfolding the functional capacity of integrated photonics by merging diverse opto-electronic strengths of several materials. Hence, the flexible and low-temperature manufacturing options enable novel concepts to realize hybrid 3D-stacked PEICs.

In this work, we present numerous photonic devices that were fabricated with a-Si:H deposited on top of oxidized Si-wafer substrates and review their functional performances. The components were patterned with electron-beam lithography (EBL) and structured using an advanced silicon deep-etch process [23]. If not stated otherwise, the systems are based on high-confinement 480 nm × 200 nm photonic wire waveguides (PWs), and the measurement results are reported for the fundamental transverse-electric TE_0 mode. In Section 2, nonuniform grating couplers (GCs), low-loss PWs, power splitters, and polarization splitters/rotators (PSRs) are studied; functional devices such as microring resonators (MRRs) and Mach–Zehnder-interferometers (MZIs) are presented. Efficient strategies to actively tune photonic devices by integrated microheaters and to permanently adjust components by UV trimming are discussed in Section 3. Optical multiplexers and routers in the form of cascaded filter banks and 4 × 4 photonic routers are presented in Section 4. The potential energy savings by the device trimming enabling sub-mW static power consumption for, e.g., eight-channel multiplexers and the anticipated mitigation of the thermal chip budget are discussed.

2. PHOTONIC BUILDING BLOCKS

A. Fiber-to-Chip Grating Couplers

Probably, the most commonly used fiber-chip couplers for HIC photonic circuits are the shallow-etched GCs with a uniform grating period. However, a drawback of this GC type is the coupling efficiency limitation ($\eta_{GC} \approx 40\%$) due to the exponential decay of the guided light along the grating, which is not well matched with single-mode fibers (SMFs) and the fraction of downward diffracted light. In case of a-Si:H, the GC directionality can be increased by bottom reflectors fabricated either by metal layers or by distributed Bragg reflectors (DBRs), which can be deposited prior the bottom silica layer. For instance, a two-stage SiO_2/a-Si:H DBR with layer thicknesses of $t = \frac{\lambda}{4n}$ combined with a standard 65 nm shallow-etch GC with 630 nm half-pitch grating period results in an improved efficiency of $\eta_{GC} = 72\%$ but requires considerably more process steps.

From a fabrication viewpoint, it is advantageous to define all photonic structures in one etch step. One solution to achieve this and to overcome the efficiency limitation is the employment of a nonuniform apodized grating coupler (AGC). The apodization minimizes reflections, which are severe for deep-etched uniform GCs, and the optimized duty cycle promotes the radiation of phase fronts that are better matched to the mode profile of optical fibers. The design was adapted to a-SOI wafers with SiO_2 thicknesses ranging from $t_{box} = 2.93$–$2.94\ \mu m$ with a 200 nm core layer. Parameters of similar devices were taken as starting values [24]; the gap and bar widths were iteratively improved by several optimization loops using the eigenmode expansion method [25]. The nonuniform GC consists of 18 duty cycles; the parameters are summarized in Table 1. The footprint is $12\ \mu m \times 13.49\ \mu m$. The theoretical coupling efficiency to a SMF-28 fiber under a 10°-angle was calculated to be $\eta_{GC} = 76\%$ (−1.2 dB), comparable with the state of the art [26–29]. The optimized coupling efficiencies of the discussed GC types are provided in Fig. 1.

An optical measurement of the AGC is shown in Fig. 2; the spectra are cleaned from Fabry–Perot reflections that increase approximately ±15 nm from the center wavelength. The coupling efficiency averaged over 12 GCs is about 42% ($\eta_{GC} \approx 3.8$ dB), the 3 dB bandwidth is $\Delta\lambda_{3\,dB} \approx 60$ nm with a center wavelength of about 1560 nm for a polymer cladding. The difference to the theoretical limit is most probably attributed to fabrication tolerances caused by lithography and nonuniform etching, particularly in the narrow gaps.

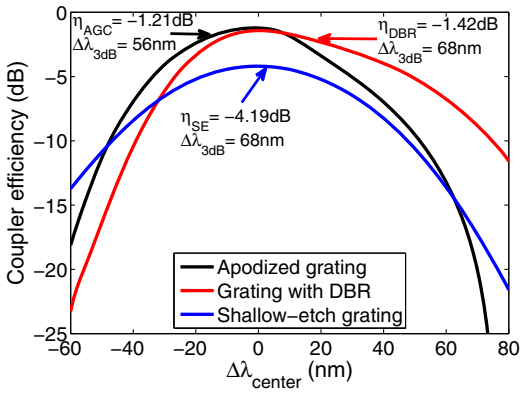

Fig. 1. Calculated coupling efficiencies and 3 dB bandwidth of shallow-etch (SE) GCs with/without DBR and of the AGC.

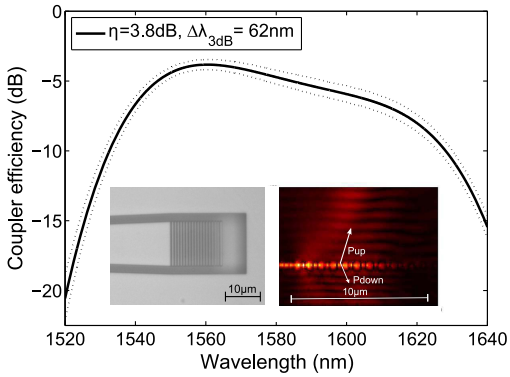

Fig. 2. Measured coupling efficiency of the AGCs with a micrograph and simulation inset.

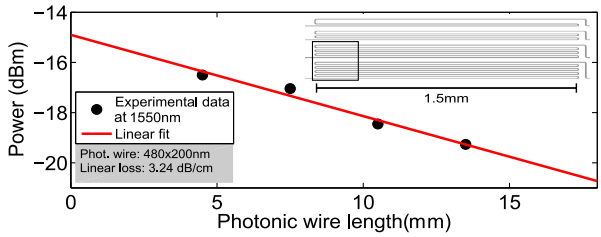

Fig. 3. Propagation loss measurements for the TE_0 mode. Inset: Mask layout of the meandered waveguides indicating a writing field.

B. Photonic Wire Losses

The propagation loss of 480 nm × 200 nm PWs was determined by virtual cut-back measurements. The linear loss for the fundamental TE mode was determined to be 3.24 dB/cm at 1550 nm wavelength, as presented in Fig. 3. The waveguides may include a small loss contribution due to the nonoptimal cladding and by stitching because the meandered waveguides were not patterned within a single EBL writing field (250 μm × 250 μm); a homogeneous wafer surface coverage promotes a uniform reactive gas consumption during ICP etching and supports low spectral nonuniformity of the photonic circuit components. Even lower a-Si:H waveguide losses of 1.2 dB/cm slightly higher than for SOI have been already demonstrated; benchmark results from the literature are summarized in Table 2. A direct performance comparison of a-Si:H and SOI PWs, bend losses, and couplers with comparable metrics has been recently reported [30].

Table 1. Nonuniform AGC Parameters

Duty cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Bar (μm)	0.60	0.56	0.56	0.57	0.57	0.56	0.55	0.55	0.54	0.54	0.54	0.53	0.53	0.53	0.50	0.42	0.45	0.61
Gap (μm)	0.18	0.18	0.18	0.18	0.20	0.24	0.22	0.20	0.20	0.20	0.23	0.24	0.24	0.25	0.35	0.26	0.23	—

Table 2. Linear Loss Comparison of a-SOI/c-SOI Photonic Wires

Ref.	Material	Dim. (nm^2)	Cladding	Loss (dB/cm)
[30]	a-/c-SOI (DUV)	500×220	SiO_2	4.5/4
[31]	c-SOI (EBL)	500×220	HSQ	0.92
[32]	a-SOI (EBL)	470×220	SiO_2	1.2
[33]	c-SOI (DUV)	450×220	I-line (SiO_2)	5.74 (2.84)
This work	a-SOI (EBL)	480×200	I-line	3.25

C. Power Splitters and Mach–Zehnder Interferometers

The HIC enables compact power dividers e.g., based on directional couplers (DCs). Experimental results of DCs with a 150 nm coupling gap for coupler length increments of $\Delta L_{DC} = 2$ μm are presented in Fig. 4. The graph shows the normalized power splitting between the two output ports at $\lambda = 1.55$ μm. The experimental results are in good agreement with the simulations as verified by the fitting. The offsets at the ordinate originate from the access bends with 20 μm radius. As evident, the 3 dB splitting is achievable with 4 μm long couplers, and any arbitrary split ratio between the bar and cross ports can be realized within $L_{DC} \approx 10$ μm supporting dense integration. The measurement of a 2×2 MZI with $L_c = 4$ μm and an arm-length difference of $\Delta L \approx 100$ μm is shown in Fig. 5. The FSR of 5.9 nm agrees well with optical simulations, and the 25 dB beat fringe depths of the MZI bar and cross port signals confirm a splitting ratio close to 3 dB.

D. Microring Resonators

Optical add–drop MRRs belong to the most universally applicable integrated-optic devices and facilitate wavelength-selective filtering functions on a small footprint. We systematically analyzed compact-sized MRRs with 5 and 10 μm radius for different bus-to-ring coupling gaps and evaluated the quality-factor Q and finesse $\mathcal{F}$. Through- and drop-port measurements are provided in Fig. 6. The MRRs exhibit mean FSRs of about 9/18 nm and through-port extinction ratios of ER ≥ 15/12.5 dB for $R = 10/5$ μm, respectively. The average drop losses were determined to be ≈1 and ≤2 dB with drop-port ERs exceeding 25 dB.

For a given fabrication process quality and a preliminary choice of the waveguide geometry including the cladding material, the coupling strength is the main parameter that can be used to define the resonator quality. Figure 7 summarizes the loaded Q-factors Q_l and the finesse values that were identified by a Lorentz fit for coupling gaps ranging from 140 to 260 nm. The graph shows that both parameters increase for wider coupling gaps, thus indicating that, within this relatively tight coupling regime, the MRR metrics according to Eq. (1) are governed by the bus-to-ring coupling quality Q_c or coupler losses, less limited by the intrinsic quality Q_i:

$$Q_l^{-1} = Q_i^{-1} + Q_c^{-1}. \tag{1}$$

Quality factors of $Q_l \approx 2 \cdot 10^4$ were determined for both ring radii and the finesse exceeds $\mathcal{F} = 100$ and $\mathcal{F} = 200$ with gaps wider than 240 nm for the 10 and 5 μm MRRs, respectively. The results are comparable with similar dimensioned devices

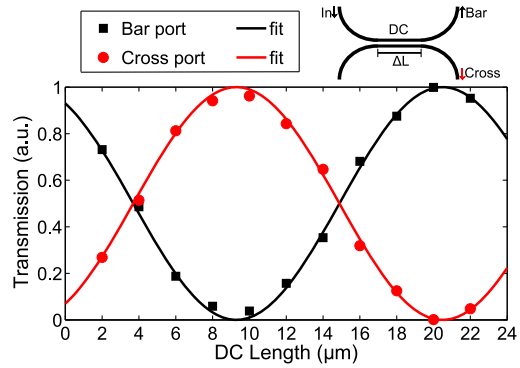

Fig. 4. Power splitting of DCs for different coupler lengths with schematic (inset).

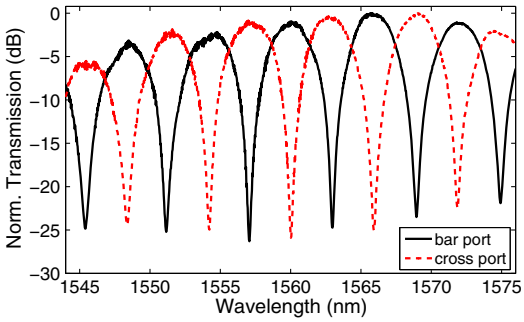

Fig. 5. Bar and cross-port signals of an MZI.

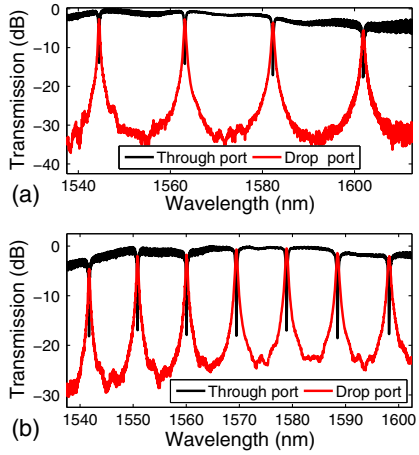

Fig. 6. Spectral characterization of add/drop microring filters: Microring with (a) 5 μm radius and (b) 10 μm radius.

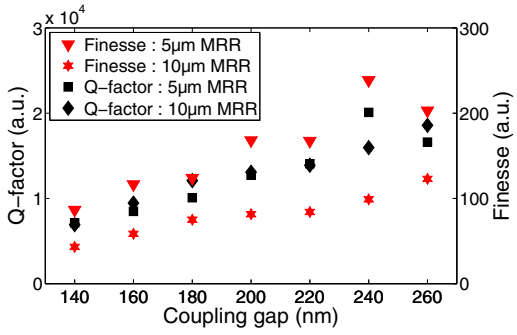

Fig. 7. Q-factor and finesse of 5 and 10 μm radius add/drop filters measured for different coupling gaps.

on c-SOI [34,35] and are well-suited for practical applications such as, e.g., biosensing [36] or wavelength-division multiplexing (WDM) [37].

E. Polarization Rotators and Splitters

Highly confined 500 nm × 200 nm PWs offer significant advantages in terms of small device footprints and scalability compared with lower-index materials; however, they exhibit higher birefringence resulting in different propagation constants of the fundamental TE and TM modes. Hence, on-chip polarization management with rotating and splitting devices is essential in certain types of applications. Efficient polarization splitter-rotators (PSRs) can be, e.g., realized by breaking the horizontal waveguide symmetry due to adjustments of the waveguide shape [38,39] or with asymmetric refractive index cladding materials. In this work, the latter approach has been pursued because the PSR fabrication relies on a single deep-etch process.

The PSR is based on an adiabatic taper for the TM- and TE-mode rotation and an asymmetric DC that performs the polarization mode conversion, as proposed in [40]. The functional principle is illustrated by the dispersion diagram in Fig. 8. The polarization rotation is realized by a flat-angle linear taper that gradually converts TM_0 to TE_1 within the hybridized mode region. The PSR is cascaded in three parts: first, the PW widths are widened to 580 nm close to the hybrid region; in the second section, the PW gradually expands with a smooth slope through the hybrid region where TM_0 is rotated to TE_1 during transition; finally, the third waveguide section, predominantly guiding TE_0 and TE_1, is tapered for directional coupling. The mode conversion is realized with asymmetric DCs, which transfer TE_1 to TE_0; however, they leave TE_0 mostly unaffected due to a large phase-mismatch. The broad waveguide was designed to be 800 nm such that the adapted narrow waveguide of 388 nm in widths provides sufficient guidance in the subsequent curvature. The coupler lengths for a complete $TE_1 - TE_0$ power transfer was calculated from the even ($n_{\mathrm{eff},e} \approx 2.015$) and odd ($n_{\mathrm{eff},o} \approx 1.96$) supermodes according to

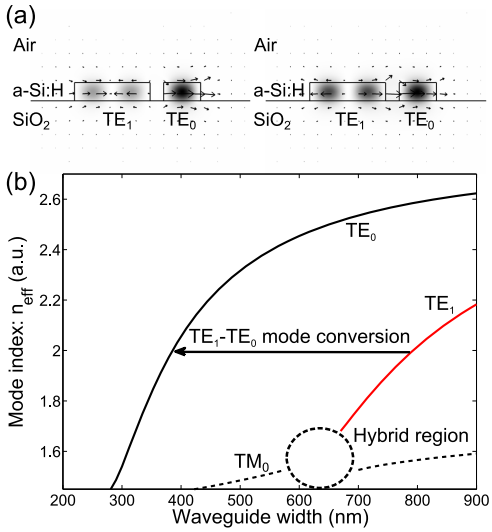

Fig. 8. (a) Even and odd supermodes of the asymmetric DC with electric field inset. (b) Mode indices of TE_0, TM_0, and TE_1 versus waveguide widths illustrating the PSR principle.

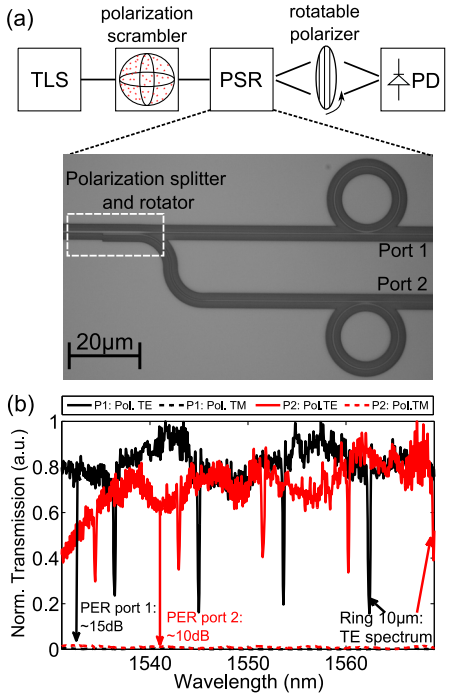

Fig. 9. (a) Measurement setup and micrograph of the PSR. (b) PSR measurements with arbitrary input polarization and polarizer cube set to TE (x axis) and TM (y axis).

$$L_{\mathrm{TE}_1-\mathrm{TE}_0} = \frac{\lambda}{2(n_{\mathrm{eff},e} - n_{\mathrm{eff},o})}, \tag{2}$$

resulting in ≈14.4 μm at $\lambda = 1.55$ μm for an air cladding with a fabrication tolerant gap of 150 nm. The overall PSR lengths is approximately 80 μm. The output arms are coupled to MRRs in order to determine the polarization rotation after the PSR due to the wavelength selective filter function.

A picture and the measurement setup are shown in Fig. 9(a). The AGCs were cleaved for the optical characterization using a tunable laser source (TLS) and the chip facet was endfire-coupled with a lensed fiber. The light was collected by a microscope objective at the output, guided through a rotatable polarizer cube via free space, and fiber-collimated to a photo detector (PD). A polarization synthesizer (Agilent N7786B) was utilized to randomly scramble the input light with arbitrary polarization states, and the PSR spectra were measured at both output ports.

The measurement results are presented in Fig. 9(b). The figure shows the two characteristic MRR spectra for the TE_0 mode with the polarizer cube oriented to the TE polarization state. The spectra do not show the existence of the TE_1 mode, and the polarization extinction ratios ($\mathrm{PER} = 10 \cdot \log_{10}(P_{\mathrm{TM0}}/P_{\mathrm{TE0}})$) at the ports P_1 and P_2 were measured to be −15 and −10 dB, respectively. The PSR insertion loss of about 1 dB was determined from reference measurements. The mode conversion efficiency can be further improved by simply cascading PSRs in series at the cost of higher transmission loss and footprint.

3. PHOTONIC DEVICE TUNING AND TRIMMING

Integrated optical devices are susceptible to fabrication inhomogeneities and even sub-nm deviations result in considerable

spectral device disorder, which is particularly relevant on a wafer scale. Hence, efficient tuning and trimming strategies for the correction of the photonic circuits are inevitable. Amorphous silicon exhibits excellent material properties for the active tuning of photonic devices by using the strong thermo-optic coefficient TOC $\geq 2 \cdot 10^{-4}(1/°C)$, up to 40% higher than for SOI $[1.86 \cdot 10^{-4}(1/°C)]$ [15], and facilitates a permanent correction of photonic components by modifying the refractive index post-fabrication. In the following, the active tuning capabilities with metal microheaters and the passive compensation by laser trimming are discussed.

A. Thermo-optic Tuning by Microheaters

The most prominent method to counteract fabrication imperfections and/or to actively tune photonic circuit components is based on the thermo-optic effect (TOE). The TOE originates from the temperature-dependent refractive material index, which in the following is treated as a real scalar value TOE $\approx \frac{\partial n}{\partial T} \cdot \Delta T$, suitable for moderate temperatures relevant for PIC tuning. The strong TOE of a-Si:H can be efficiently employed to adjust photonic circuit components with high precision over several nanometers. The temperature-dependent wavelength shift (TDWS) of a MRR is linearly proportional to temperature and is described by

$$\Delta\lambda_r = \frac{\partial n_{\text{eff}}}{\partial T} \cdot \frac{\lambda_r}{n_{\text{gr}}} \cdot \Delta T, \tag{3}$$

with n_{gr} as group index. Photonic chips were gradually heated with $\Delta T = 2.5°C$ by using a temperature-controlled chip mount in order to determine the TDWS and to evaluate the microheater design. Resonance shifts of $\Delta\lambda_r \approx 92$ pm/°C were measured for 10 μm MRRs with a sputtered SiO_2 cladding.

The integrated microheaters were optimized with the finite element method (COMSOL FEM). The metal heaters were positioned on top of the photonic structures in order to facilitate a good heat transfer to the photonic components with low tuning power and to simplify the routing of the optical and electrical layers. A 1 μm thick SiO_2 cladding was sputtered on top of the bare photonic chips, followed by sputtering titan (Ti) for the heaters and gold (Au) for the bond pads. The microheaters with 2 μm widths and 200 nm thickness were patterned with I-line exposure contact photolithography using alignment markers and reference structures in the a-Si:H core layer and were wet-etched: Au ($KI:I_2:H_2O$) and Ti ($HF:H_2O_2:H_2O$).

The microheater arrays were wire-bonded to a printed circuit board, which was connected to a digital/analog data acquisition card serving as driver. The successive redshift of the drop-port resonance due to different heating powers is shown in Fig. 10. The efficiency on different chips was determined to range between $P/\lambda \approx 2.1$–2.4 mW/nm, corresponding to a more universal and ring-size-independent metric of $P/\text{FSR} \approx 19$–22 mW. The deviations result primary from nonuniform wet-etching dependent on the pattern density and can be reduced by lift-off processes. The current heater performance allows tuning a 5 μm MRR over its full FSR of 18 nm with a voltage of about 6.5 V, whereas a 10 μm MRR with 9 nm FSR requires 4.5 V. The microheater efficiency is in line with the best reported values based on SOI devices typically ranging between $P/\text{FSR} = 20$–40 mW [41,42]. In principle, due to the higher TOC, higher efficiencies are possible

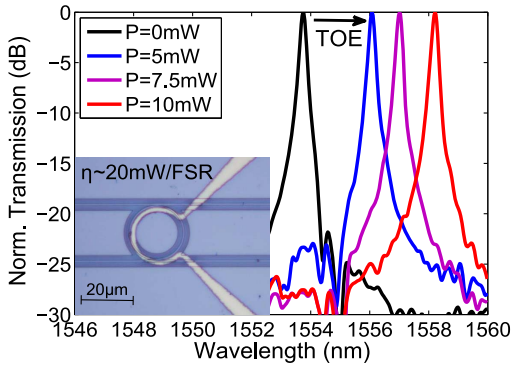

Fig. 10. Measured tuning efficiency of microheaters placed on top of a 10 μm resonator with microscope picture (inset).

with a-SOI. Further methods that enhance the tuning efficiency with same-dimensioned microheaters include the isolation of the photonic components, e.g., by locally etching the Si/SiO_2-substrate from the front- or backside [43–45].

B. Device Adjustments by Laser Trimming

Photonic devices based on HIC materials demand high-precision fabrication, and any perturbation of the guided mode index affects the circuit performance. Although microheaters are ideally suited to actively control photonic circuit components, the correction of manufacturing imperfections dissipates a significant amount of energy and increases the overall thermal load of the photonic chip, which, in turn, demands further run-time compensation. Both effects substantially increase the power budget and may contribute several 10 percents of the overall photonic circuit power [46–48]. Hence, a method that is capable of compensating fabrication tolerances and adjusting the amplitude and phase characteristics of photonic circuit components is advantageous for wafer-scale photonics.

The resonance shift $\Delta\lambda_r$ due to a change in guided mode index Δn_{eff}, which was calculated with an FEM mode solver and numerical calculations, is shown Fig. 11. The results provide that it is possible to trim the MRR spectrum over 10 nm with sub-percentile index modifications. In case of a-Si:H, the material index is trimmable by photolytic processes, so that readily-fabricated PIC devices can be adjusted. The trimming setup, range, velocity, and the tuning accuracy are reported elsewhere [49]. Measurement results of an MRR, which was

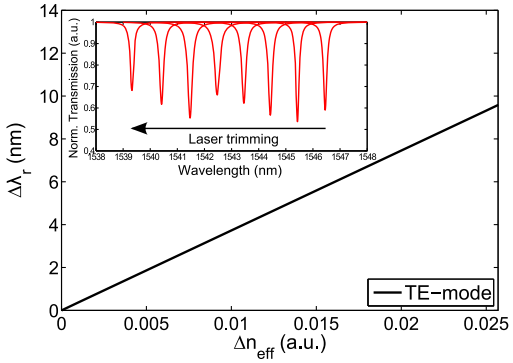

Fig. 11. Resonance shift due to modifications of the effective mode index. Resonance trimming of an uncladded 10 μm MRR blueshifted in 1 nm increments.

gradually blueshifted by $\Delta\lambda_r = 7$ nm ($\Delta n_{\text{eff}} \approx 0.02$) with about 20 pm spectral resolution due to UV-laser irradiation with 405 nm wavelength are inset.

4. PHOTONIC SWITCH NETWORKS AND MULTIPLEXERS

The ability to guide multiple high-data-rate signals within a single waveguide by WDM is a significant property of optical transmission systems. In recent years, high-bandwidth WDM systems have evolved from passive fiber optic communication networks (PONs) down to reconfigurable network-on-chip (NoC) systems [50,51]. In particular, photonic interconnects for high-performance computing and data center communication are promising technologies that could push the technological limits of electronic interconnects that are increasingly affected by RC latency, increased power consumption, and heat generation. Silicon photonics is a potential platform to overcome these bottlenecks because HIC optical interconnects facilitate energy-efficient communication networks with low device footprints fabricated at moderate costs. Integrated optical add/drop multiplexers (OADMs) are essential key devices to perform the selective filtering and routing for these low-power applications [52].

A. Optical Add/Drop Multiplexer

Wavelength multiplexers made of cascaded microrings and racetracks with up to eight channels were realized on a dense 100 GHz grid ($\Delta\lambda_r \approx 0.8$ nm). The compact filters were designed to provide a reasonable trade-off between high-data-rate capability, low inter-channel cross talk, and tolerable drop-port loss. The wavelength channels were defined by the ring radii ($\Delta R_{\text{ch}} = 6$–10 nm). The bus-to-ring gaps were outlined with 150 nm for 10 μm radius MRRs. Racetracks with the same curvature were designed with straight coupling sections of 4 μm and 300 nm coupling gaps. For the given parameters, assuming 3 dB propagation and 0.025 dB coupling losses, the simulations reveal drop-port losses of about 1 dB, 15–20 dB inter-channel isolation, and 3 dB bandwidths in the range of 0.18–0.3 nm supporting data rates beyond 20 Gb/s [37].

Measurement results of a low-footprint four-channel racetrack OADM are presented in Fig. 12; a micrograph is inset. The 3 dB bandwidths are 0.22 nm, the channel cross talk is –20 dB, and low drop-port losses of about 1.5 dB were determined. The channels are clearly resolved with 30 dB extinction and spaced by 100 GHz. The TOE was employed in order to counterbalance the fabrication imperfections of $\sigma_{\lambda_r} \approx 0.3$ nm, which were measured per MRR. In spite of the low spectral nonuniformity from fabrication, a non-negligible steady-state power of $P \approx 0.7$ mW/MRR is still permanently consumed for the channel alignment using the as-presented top heaters.

In this context, we studied the device variability of eight-channel OADMs, as presented in Fig. 13, and evaluated the power requirement for compensation as well as the potential energy savings per device due to the trimming method. The statistical variations of such a-SOI OADMs were determined to range between $\sigma_{\lambda_r} = 0.3$–0.6 nm. Based on our measurements, the channel alignment to the nearest possible ITU specified 100 GHz grid requires about 10–30 mW per eight-channel device. However, this is a simplified scenario because several hundreds to thousands of such devices can be fabricated on a single wafer; hence, the assignment on a wafer-scale is more complex. The process variation of c-SOI MRRs manufactured in CMOS-lines accounts for approximately 1.3 nm^2/cm [53], which, e.g., corresponds to an additional power increase of 3 mW/cm per channel for top heaters with state-of-the-art performance, if the OADMs are targeted to operate on the same grid. In comparison, on a-SOI and EBL, we determined a similar process variation of about 0.7 nm/cm for 50% of the devices and about 2–3 nm/cm for $3-\sigma$ [54]. Note that, again, this power is only consumed to equalize the OADM channels relative to each other and the nearest 100 GHz grid and might be significantly higher if an absolute alignment of on-/off-chip lasers with predefined channels is required.

Furthermore, the static tuning of the photonic devices introduces significant local thermal loads, roughly 10°C/cm based on the above metrics, which may affect the photonic link reliability and might require further run-time compensation [55]. Evidently, a passive device trimming, which avoids the overhead tuning power and associated thermal budget and which, in addition, allows assigning athermal filters [16,48] or

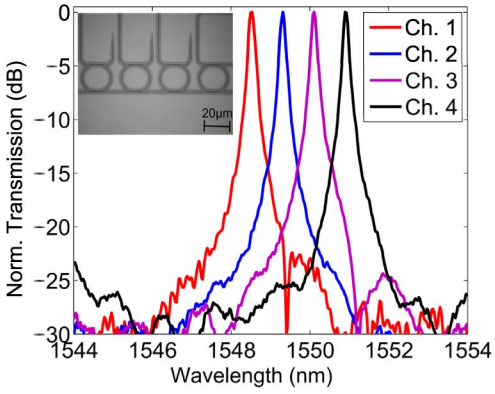

Fig. 12. Racetrack-based multiplexer TOE aligned to the 100 GHz DWDM grid with micrograph inset.

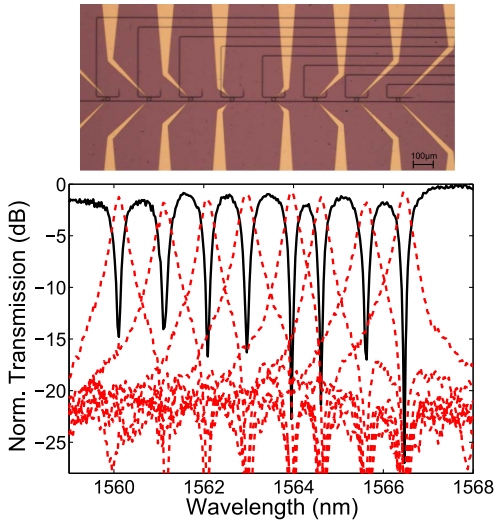

Fig. 13. Through- and drop-port spectra of a wavelength-trimmed eight-channel multiplexer with micrograph.

PICs with hybrid integrated or external sources, is advantageous in terms of energy efficiency. Apart from that, a vertically integrated photonic backplane will be even more challenging from a manufacturing viewpoint, and the PIC nonuniformity will probably be higher than discussed above.

The potential energy savings of the presented OADMs considering only the static power reduction for the nonuniformity compensation are presented in Fig. 14. The channel variability of the as-fabricated multiplexers and the remaining variations after the trimming are shown in Fig. 14(a). The power estimates for the most simplified scenario, which means that the OADMs are configured to the nearest possible 100-GHz grid for top and suspended microheaters (20 and 2.4 mW/FSR), are presented in Fig. 14(b). The power budget is significantly reduced by more than an order of magnitude down to the sub-mW region per eight-channel device with a thermal load $\Delta T \leq 1°C$ due to alignment, even for top heaters that provide faster switching speed than their under-etched counterparts [42].

B. Photonic Router

The optical routes of cascaded OADMs are fixed and, hence, link transmitters and receivers in a predefined way. A more versatile concept is based on reconfigurable NoCs, as shown in Fig. 15(a), with MRR switches, which distribute signals among shared optical paths, thereby reducing resources such as lasers and detectors. In the off-resonant state, the signal passes the crossing whereas it can be routed by shifting the MRR on-resonance, e.g., with microheaters. Prototype 4×4 NoCs with 10 and 20 μm radii MRRs were realized with 260 nm coupling gaps. The crossing with about 1 dB loss is based on a simple design using linear tapers. The devices were characterized in the static case, the results of the 10 μm MRRs are summarized in Fig. 15(b). The rows correspond to the inputs ($I_1 - I_4$) and the columns to the output ports ($O_1 - O_4$) that were accessible within this design. The MRRs are undercoupled at 1.55 μm and perform better at 1.6 μm and beyond, where the extinction ratios were determined to be about 10 and 25 dB for the through and drop ports, respectively. The static measurements showcase the potential to realize reconfigurable NoCs in 3D arrangement at BEOL, thus employing a combination of permanent trimming and energy-efficient tuning methods.

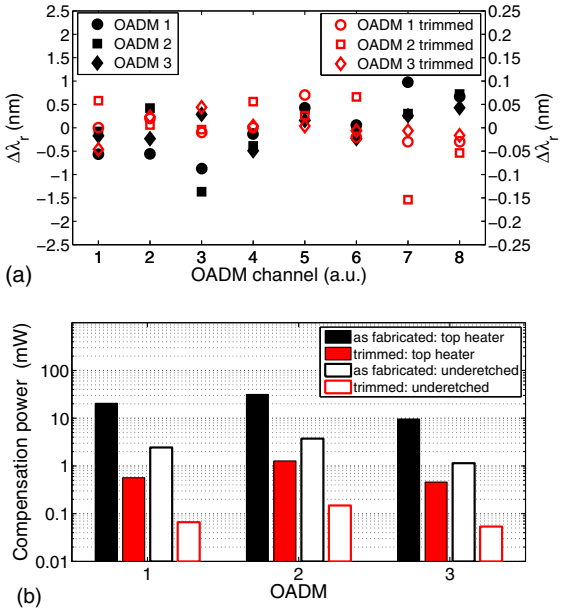

Fig. 14. (a) Spectral disorder of as-fabricated and trimmed OADMs. (b) Static power consumption for the eight-channel assignments of as-fabricated and trimmed OADMs.

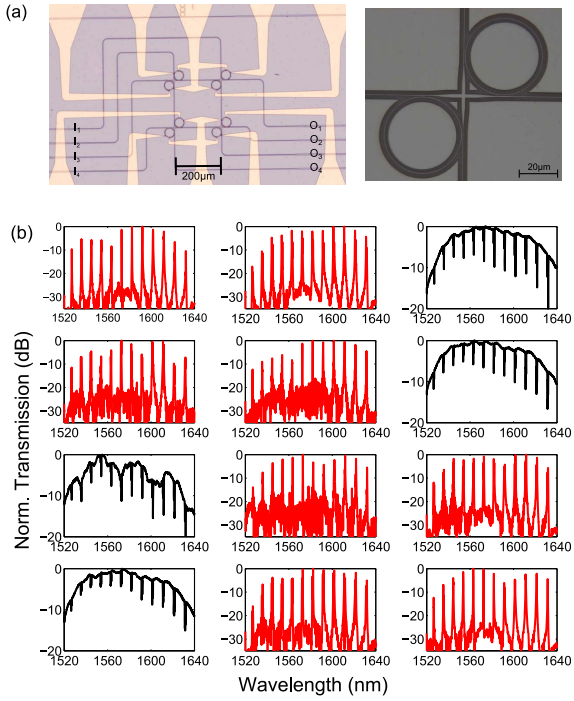

Fig. 15. (a) Micrographs of a 4×4 photonic router and a MRR-switch. (b) Static measurements with inputs (I_{1-4}) and output ports (O_{1-4}) from top to bottom: Row 1: $I_1 - O_{1-3}$. Row 2: $I_2 - O_{2,3,4}$. Row 3: $I_3 - O_{1,2,4}$. Row 4: $I_4 - O_{2-4}$.

5. CONCLUSION

We fabricated and systematically characterized photonic components based on a-SOI material platform. Fiber-to-chip GCs, low-loss PWs, Mach–Zehnder interferometers, and MRRs with key metrics broadly comparable to SOI are reported. Compact power splitters and polarization rotators for on-chip polarization management are presented. The functional quality of the devices is well-suited for practical applications in the areas of biosensing, data-, and telecommunication. Due to the low-deposition temperature, it might be reasonably assumed that devices with comparable quality can be fabricated with low-cost substrate materials such as glasses or even plastics.

The thermo-optic tuning capabilities of a-Si:H material are analyzed, and efficient microheaters with 20 mW/FSR tuning efficiency are demonstrated. Low-footprint wavelength multiplexers and 4×4 photonic routers are presented. Fabrication imperfections were analyzed and permanently corrected, so that record low metrics of sub-mW consumption per eight-channel multiplexer with ≤1°C temperature introduction due to tuning become feasible. The efficient tuning and accurate trimming capabilities demonstrate the potential to realize low-cost, densely integrated, and ultralow-power 3D-stacked photonic circuits on top of microelectronics.

Acknowledgment

This publication was supported by DFG and TUHH in the funding programme Open Access Publishing. Fraunhofer (HHI-Berlin) is acknowledged for EBL.

REFERENCES

1. G. Cocorullo, F. G. D. Corte, I. Rendina, C. Minarini, A. Rubino, and E. Terzini, "Amorphous silicon waveguides and light modulators for integrated photonics realized by low-temperature plasma-enhanced chemical-vapor deposition," Opt. Lett. **21**, 2002–2004 (1996).
2. A. Harke, M. Krause, and J. Müller, "Low-loss singlemode amorphous silicon waveguides," Electron. Lett. **41**, 1377–1379 (2005).
3. F. G. Della Corte, S. Rao, G. Coppola, and C. Summonte, "Electro-optical modulation at 1550 nm in an as-deposited hydrogenated amorphous silicon p-i-n waveguiding device," Opt. Express **19**, 2941–2951 (2011).
4. F. Corte and S. Rao, "Use of amorphous silicon for active photonic devices," IEEE Trans. Electron Devices **60**, 1495–1505 (2013).
5. Y. H. D. Lee, M. O. Thompson, and M. Lipson, "Deposited low temperature silicon ghz modulator," Opt. Express **21**, 26688–26692 (2013).
6. H. Byun, J. Bok, K. Cho, K. Cho, H. Choi, J. Choi, S. Choi, S. Han, S. Hong, S. Hyun, T. J. Jeong, H.-C. Ji, I.-S. Joe, B. Kim, D. Kim, J. Kim, J.-K. Kim, K. Kim, S.-G. Kim, D. Kong, B. Kuh, H. Kwon, B. Lee, H. Lee, K. Lee, S. Lee, K. Na, J. Nam, A. Nejadmalayeri, Y. Park, S. Parmar, J. Pyo, D. Shin, J. Shin, Y.-H. Shin, S.-D. Suh, H. Yoon, Y. Park, J. Choi, K.-H. Ha, and G. Jeong, "Bulk-si photonics technology for dram interface [invited]," Photon. Res. **2**, A25–A33 (2014).
7. S. Rao, G. Coppola, C. Summonte, and F. G. D. Corte, "Progress towards a high-performing a-si:h-based electro-optic modulator," J. Opt. **16**, 055501 (2014).
8. C. Xiong, W. H. P. Pernice, J. H. Ngai, J. W. Reiner, D. Kumah, F. J. Walker, C. H. Ahn, and H. X. Tang, "Active silicon integrated nanophotonics: Ferroelectric batio3 devices," Nano Lett. **14**, 1419–1425 (2014).
9. L. Cao, A. Aboketaf, Z. Wang, and S. Preble, "Hybrid amorphous silicon (a-si:h)-linbo3 electro-optic modulator," Opt. Commun. **330**, 40–44 (2014).
10. Y. Shoji, T. Ogasawara, T. Kamei, Y. Sakakibara, S. Suda, K. Kintaka, H. Kawashima, M. Okano, T. Hasama, H. Ishikawa, and M. Mori, "Ultrafast nonlinear effects in hydrogenated amorphous silicon wire waveguide," Opt. Express **18**, 5668–5673 (2010).
11. K. Narayanan, A. W. Elshaari, and S. F. Preble, "Broadband all-optical modulation in hydrogenated-amorphous silicon waveguides," Opt. Express **18**, 9809–9814 (2010).
12. S. Suda, K. Tanizawa, Y. Sakakibara, T. Kamei, K. Nakanishi, E. Itoga, T. Ogasawara, R. Takei, H. Kawashima, S. Namiki, M. Mori, T. Hasama, and H. Ishikawa, "Pattern-effect-free all-optical wavelength conversion using a hydrogenated amorphous silicon waveguide with ultra-fast carrier decay," Opt. Lett. **37**, 1382–1384 (2012).
13. J. Müller, M. Mahnke, G. Schoer, and S. Wiechmann, "Inorganic materials integrated optics," AIP Conf. Proc. **709**, 268–289 (2004).
14. M. Sodagar, R. Pourabolghasem, A. A. Eftekhar, and A. Adibi, "High-efficiency and wideband interlayer grating couplers in multilayer si/sio2/sin platform for 3d integration of optical functionalities," Opt. Express **22**, 16767–16777 (2014).
15. S. Zhu and G.-Q. Lo, "Vertically-stacked multilayer photonics on bulk silicon toward three-dimensional integration," J. Lightwave Technol. **34**, 386–392 (2015).
16. T. Lipka, L. Moldenhauer, J. Müller, and H. K. Trieu, "Athermal and wavelength-trimmable photonic filters based on tio2-cladded amorphous-soi," Opt. Express **23**, 20075–20088 (2015).
17. T. Shindo, T. Okumura, H. Ito, T. Koguchi, D. Takahashi, Y. Atsumi, J. Kang, R. Osabe, T. Amemiya, N. Nishiyama, and S. Arai, "Lateral-current-injection distributed feedback laser with surface grating structure," IEEE J. Sel. Top. Quantum Electron. **17**, 1175–1182 (2011).
18. H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, and H. Riel, "Template-assisted selective epitaxy of IIIV nanoscale devices for co-planar heterogeneous integration with Si," Appl. Phys. Lett. **106**, 233101 (2015).
19. D.-M. Geum, M.-S. Park, J. Y. Lim, H.-D. Yang, J. D. Song, C. Z. Kim, E. Yoon, S. Kim, and W. J. Choi, "Ultra-high-throughput production of III-V/Si wafer for electronic and photonic applications," Sci. Rep. **6**, 20610 (2016).
20. C.-H. Hsieh, Y.-T. Chu, M.-J. Huang, C.-M. Kuo, and K.-C. Leou, "Design of a low loss silicon based hybrid dielectric loaded plasmonic waveguide and a compact high performance optical resonator," Prog. Electromagn. Res. **42**, 135–144 (2015).
21. J. Cheng and N. Yan, "Three-step lithography to the fabrication of vertically coupled micro-ring resonators in amorphous silicon-on-insulator," Chin. Opt. Lett. **13**, 082201 (2015).
22. W. Heni, C. Haffner, B. Baeuerle, Y. Fedoryshyn, A. Josten, D. Hillerkuss, J. Niegemann, A. Melikyan, M. Kohl, D. Elder, L. Dalton, C. Hafner, and J. Leuthold, "108 Gbit/s plasmonic Mach-Zehnder modulator with 70-ghz electrical bandwidth," J. Lightwave Technol. **34**, 393–400 (2016).
23. T. Lipka, O. Horn, J. Amthor, and J. Müller, "Low-loss multilayer compatible a-si:h optical thin films for photonic applications," J. Eur. Opt. Soc. **7**, 12033 (2012).
24. M. Antelius, K. B. Gylfason, and H. Sohlström, "An apodized soi waveguide-to-fiber surface grating coupler for single lithography silicon photonics," Opt. Express **19**, 3592–3598 (2011).
25. P. Bienstman and R. Baets, "Optical modelling of photonic crystals and vcsels using eigenmode expansion and perfectly matched layers," Opt. Quantum Electron. **33**, 327–341 (2001).
26. D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform," Opt. Express **18**, 18278–18283 (2010).
27. G. Roelkens, D. Vermeulen, S. Selvaraja, R. Halir, W. Bogaerts, and D. Van Thourhout, "Grating-based optical fiber interfaces for silicon-on-insulator photonic integrated circuits," IEEE J. Sel. Top. Quantum Electron. **17**, 571–580 (2011).
28. L. Carroll, D. Gerace, I. Cristiani, and L. C. Andreani, "Optimizing polarization-diversity couplers for si-photonics: reaching the -1db coupling efficiency threshold," Opt. Express **22**, 14769–14781 (2014).
29. W. S. Zaoui, A. Kunze, W. Vogel, M. Berroth, J. Butschke, F. Letzkus, and J. Burghartz, "Bridging the gap between optical fibers and silicon photonic integrated circuits," Opt. Express **22**, 1277–1286 (2014).
30. G. Fan, R. Orobtchouk, B. Han, Y. Li, C. Hu, L. Lei, H. Li, L. Xu, and Q. Wang, "Optical waveguides on three material platforms of silicon-on-insulator, amorphous silicon an d silicon nitride," IEEE J. Sel. Top. Quantum Electron. (2015), doi: 10.1109/JSTQE.2015.2494681.
31. M. Gnan, S. Thoms, D. Macintyre, R. De La Rue, and M. Sorel, "Fabrication of low-loss photonic wires in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist," Electron. Lett. **44**, 115–116 (2008).
32. K. Furuya, K. Nakanishi, R. Takei, E. Omoda, M. Suzuki, M. Okano, T. Kamei, M. Mori, and Y. Sakakibara, "Nanometer-scale thickness control of amorphous silicon using isotropic wet-etching and low loss wire waveguide fabrication with the etched material," Appl. Phys. Lett. **100**, 251108 (2012).
33. L. Y. M. Tobing, L. Tjahjana, S. Darmawan, and D. H. Zhang, "Numerical and experimental studies of coupling-induced phase shift in resonator and interferometric integrated optics devices," Opt. Express **20**, 5789–5801 (2012).
34. M. Soltani, S. Yegnanarayanan, Q. Li, and A. Adibi, "Systematic engineering of waveguide-resonator coupling for silicon microring/microdisk/racetrack resonators: Theory and experiment," IEEE J. Quantum Electron. **46**, 1158–1169 (2010).
35. W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. K. Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," Laser Photon. Rev. **6**, 47–73 (2012).
36. T. Lipka, L. Wahn, H. K. Trieu, L. Hilterhaus, and J. Müller, "Label-free photonic biosensors fabricated with low-loss hydrogenated amorphous silicon resonators," J. Nanophoton. **7**, 073793 (2013).

37. T. Lipka, L. Moldenhauer, J. Müller, and H. K. Trieu, "Energy-efficient wavelength multiplexers based on hydrogenated amorphous silicon resonators," IEEE Photon. J. **7**, 1–11 (2015).
38. M. R. Watts, M. Qi, T. Barwicz, L. Socci, P. T. Rakich, E. P. Ippen, H. I. Smith, and H. A. Haus, "Towards integrated polarization diversity: Design, fabrication and characterization of integrated polarization splitters and rotators," in *Optical Fiber Communications Conference Technical Digest* (March 6, 2005), paper PDP11.
39. Y. Xiong, D.-X. Xu, J. Schmid, P. Cheben, S. Janz, and W. Ye, "Robust silicon waveguide polarization rotator with an amorphous silicon overlayer," IEEE Photon. J. **6**, 1–8 (2014).
40. D. Dai and J. E. Bowers, "Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires," Opt. Express **19**, 10940–10949 (2011).
41. M. Watts, W. Zortman, D. Trotter, G. Nielson, D. Luck, and R. Young, "Adiabatic resonant microrings (arms) with directly integrated thermal microphotonics," in *Conference on Lasers and Electro-Optics*, Baltimore, Maryland (2009), paper CPDB10.
42. A. H. Atabaki, E. Shah Hosseini, A. A. Eftekhar, S. Yegnanarayanan, and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," Opt. Express **18**, 18312–18323 (2010).
43. J. E. Cunningham, I. Shubin, X. Zheng, T. Pinguet, A. Mekis, Y. Luo, H. Thacker, G. Li, J. Yao, K. Raj, and A. V. Krishnamoorthy, "Highly-efficient thermally-tuned resonant optical filters," Opt. Express **18**, 19055–19063 (2010).
44. J. Amthor, O. Horn, T. Lipka, A. Savov, and J. Müller, "Fabrication of freestanding sio2-membrane systems for thermo-optic adjusting of soi photonic wires," IEEE Photon. Technol. Lett. **23**, 1142–1144 (2011).
45. Q. Fang, J. Song, X. Luo, L. Jia, M. Yu, G. Lo, and Y. Liu, "High efficiency ring-resonator filter with nisi heater," IEEE Photon. Technol. Lett. **24**, 350–352 (2012).
46. J. Ahn, M. Fiorentino, R. Beausoleil, N. Binkert, A. Davis, D. Fattal, N. Jouppi, M. McLaren, C. Santori, R. Schreiber, S. Spillane, D. Vantrease, and Q. Xu, "Devices and architectures for photonic chip-scale integration," Appl. Phys. A **95**, 989–997 (2009).
47. W. A. Zortman, D. C. Trotter, and M. R. Watts, "Silicon photonics manufacturing," Opt. Express **18**, 23598–23607 (2010).
48. Z. Zhou, B. Yin, Q. Deng, X. Li, and J. Cui, "Lowering the energy consumption in silicon photonic devices and systems [invited]," Photon. Res. **3**, B28–B46 (2015).
49. T. Lipka, M. Kiepsch, H. K. Trieu, and J. Müller, "Hydrogenated amorphous silicon photonic device trimming by uv-irradiation," Opt. Express **22**, 12122–12132 (2014).
50. N. Sherwood-Droz, H. Wang, L. Chen, B. G. Lee, A. Biberman, K. Bergman, and M. Lipson, "Optical 4×4 hitless silicon router for optical networks-on-chip (noc)," Opt. Express **16**, 15915–15922 (2008).
51. M. Taubenblatt, "Optical interconnects for high-performance computing," J. Lightwave Technol. **30**, 448–457 (2012).
52. Y. Li, Y. Zhang, L. Zhang, and A. W. Poon, "Silicon and hybrid silicon photonic devices for intra-datacenter applications: state of the art and perspectives [invited]," Photon. Res. **3**, B10–B27 (2015).
53. X. Chen, M. Mohamed, Z. Li, L. Shang, and A. R. Mickelson, "Process variation in silicon photonic devices," Appl. Opt. **52**, 7638–7647 (2013).
54. T. Lipka, J. Müller, and H. K. Trieu, "Systematic non-uniformity analysis of amorphous silicon-on-insulator photonic microring resonators," J. Lightwave Technol. (2016), doi: 10.1109/JLT.2016.2549738.
55. M. Mohamed, Z. Li, X. Chen, L. Shang, and A. Mickelson, "Reliability-aware design flow for silicon photonics on-chip interconnect," IEEE Trans. Very Large Scale Integr. Syst. **22**, 1763–1776 (2014).