Bulk-Si photonics technology for DRAM interface [Invited]

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We present photonics technology based on a bulk-Si substrate for cost-sensitive dynamic random-access memory (DRAM) optical interface application. We summarize the progress on passive and active photonic devices using a local-crystallized Si waveguide fabricated by solid phase epitaxy or laser-induced epitaxial growth on bulk-Si substrate. The process of integration of a photonic integrated circuit (IC) with an electronic IC is demonstrated using a 65 nm DRAM periphery process on 300 mm wafers to prove the possibility of seamless integration with various complementary metal-oxide-semiconductor devices. Using the bulk-Si photonic devices, we show the feasibility of high-speed multidrop interface: the Mach–Zehnder interferometer modulators and commercial photodetectors are used to demonstrate four-drop link operation at 10 Gb/s, and the transceiver chips with photonic die and electronic die work for the DDR3 DRAM interface at 1.6 Gb/s under a 1:4 multidrop configuration. © 2014 Chinese Laser Press

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1. INTRODUCTION

A. Need for Optical Interconnect for Memory Interface

As the demand continues for higher performance servers or PCs, the bandwidth and capacity requirements of the main memory system is correspondingly growing [1–3]. The industry has been relying on the multidrop bus topology to connect multiple memory modules to one memory controller channel. The multidrop approach allows higher capacity with the advantages of lower latency and lower cost. However, as the per-pin data rate increases, the undesired reflections from the stub of multidrop degrade the signal integrity (SI) more severely. Figure 1 shows eye-diagram simulation results of an electrical memory channel having four memory modules per channel. In the simulation, the SI of the electrical signals intolerably degrades for data rates over 2 Gb/s due to the impedance mismatch. Consequently, the number of supported memory modules per controller channel should decrease as data rates goes up.

A registered dual in-line memory module (RDIMM) reduces the loading of command/address signals to improve SI, and a load reduced in-line memory module (LRDIMM) [4] extends the same approach to all signals by retransmitting both data and command/address signals. However, both RDIMM and LRDIMM do not address the essential limit of a multidrop bus, because they maintain a multidrop bus topology. Point-to-point channels to individual memory modules can mitigate the signal integrity issue, but the limited number of pins from the memory controller or processor and limited printed circuit board (PCB) routing area will be significant obstacles to support as many memory modules as conventional multidrop bus topology. The advanced memory buffers (AMBs) in fully buffered DIMM [5–7] concatenate original signals into multiple point-to-point high-speed differential signals, and they function as an interface hub connecting the memory controller to each DIMM in a daisy-chain. However, they suffer from increased latency (linearly increasing with the number of hops through multiple AMBs) and power consumption problems from signal repeating and high-speed serialization/deserialization.

An impedance-matched bidirectional multidrop bus was suggested [8] to entirely remove the unwanted reflections, but signal swing becomes much smaller and a termination module is required on unused slots. An equalization technique can be used to cancel the reflective intersymbol interference, but the achievable operation frequency is limited [9].

Optical interconnect technology is a promising candidate to scale up dynamic random-access memory (DRAM) interface over 10 Gb/s for the per-pin data rate without compromising the per-channel capacity, because optical channels are intrinsically free from impedance mismatch [10].

B. Need for Bulk-Si-Based Optical Interconnect

Silicon photonics can provide a cost-efficient optical channel by fabricating the photonic devices on a silicon substrate

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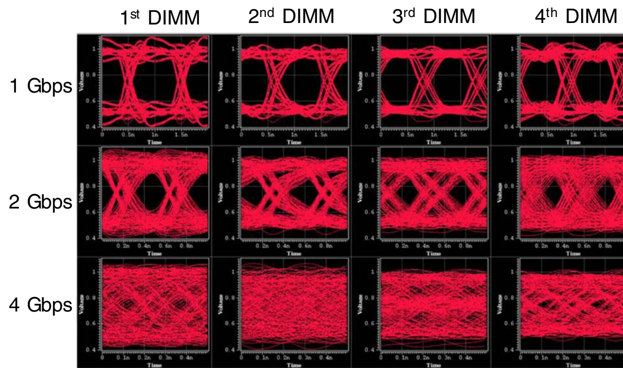

Fig. 1. Simulated eye diagrams of memory bus with 4 DIMMs in one DDR3 memory channel.

using already-mature complementary metal-oxide semiconductor (CMOS) technology and can also be one of the most viable technologies for central processing unit (CPU)–memory optical interconnects. Over the past decades, there have been great achievements in silicon photonics [11–13]. Most of previous photonic devices were fabricated on silicon-on-insulator (SOI) substrates. SOI platform is well suited for implementing the optical devices thanks to enough thickness of the bottom cladding layer and good crystal quality of the silicon core layer. However, most legacy electronic integrated circuits (ICs) are still made on bulk-Si substrates, and it may not be cost-efficient to use relatively expensive SOI substrate for cost-sensitive DRAM modules or devices. The price of SOI substrate is found to be about 10 times more expensive than that of bulk-Si substrates in the range of 4–8 in. diameter [14,15].

Thus, we propose to implement photonic devices on a bulk-Si platform for lower material cost and capability of integrating photonic devices with electronic circuits on bulk-Si substrate. There are several related works for bulk-Si approaches, where optical waveguides are defined with the poly-Si core layer on the oxide undercladding [16] or with crystal Si on the air undercladding [17]. However, the optical propagation loss of the poly-Si waveguide is still relatively high, and the effects of an air void during successive processes are not validated yet.

In this paper, we introduce bulk-Si photonics technology using local-crystallized Si-core waveguides on oxide for the interface between CPU and DRAMs. In Section 2, the progress in process technology and photonic devices is explained. Then, in Section 3, we show how the process is used to fabricate electronic and photonic ICs and construct a bidirectional optical interconnect. Last, in Section 4, read/write transactions are verified with a DDR3 DRAM device through the bulk-Si optical interconnect.

2. BULK-SI PHOTONICS PLATFORM

A. Local Crystallization of Amorphous Silicon (Waveguide and Coupler)

The most basic building block of silicon photonics is the waveguide through which light propagates from one point to another point. In order to fabricate the waveguide and other optical devices on the bulk-Si substrate, a lower-refractive-index cladding for optical confinement is required under the crystalline silicon layer.

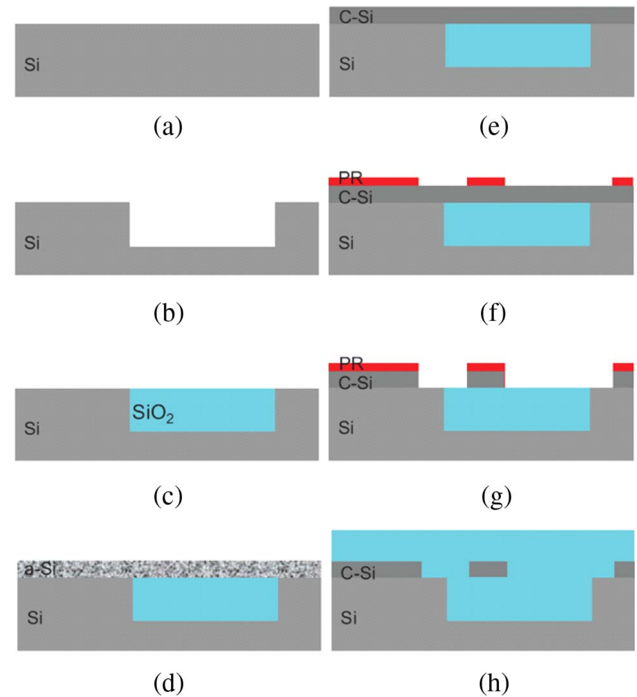

Fig. 2. Process steps for fabricating the waveguide on a bulk-Si substrate. C-Si: crystallized silicon, PR: photoresist.

Figure 2 shows the process steps to fabricate the waveguide on a bulk-Si substrate [18]. First, a 1 μm-deep, 6 μm-wide trench was formed along the light propagation direction in the bulk-Si substrate and filled with silicon oxide, which serves as the bottom cladding for the waveguide. At each end of the waveguide, the trench widened to 16 μm width (see Fig. 3) to accommodate vertical grating couplers (VGCs) with a 10 μm adiabatic taper for the coupling with optical fiber. The amorphous silicon (a-Si) was then deposited by low-pressure chemical vapor deposition (LPCVD) at low temperature to form the core layer, with a thickness of 255 nm to support single mode propagation. The deposited a-Si was crystallized by a solid phase epitaxy (SPE) process [19]. After crystallization, the Si thickness slightly reduced to 250 nm. The crystal seed was the top surface of the bulk-Si substrate adjacent to the trench edges, and the crystal growth laterally proceeds from both edges toward the center of the trench. The channel waveguide with a width of 500 nm and a height of 250 nm was patterned using dry etching on the crystallized core layer. The waveguide was repeated with lengths of 1, 2, 4, 6, and 8 mm to measure the insertion loss per unit length and attached with VGCs on both ends of each length. The VGCs were fabricated to operate around the wavelength of 1.55 μm by designing the period, etch depth, and duty ratio as 610 nm, 95 nm, and 50%, respectively.

Figure 3 shows the crystal growth of a-Si for different annealing conditions using the scanning electron microscope (SEM) images [18]. The annealing temperature and time were set to minimize the simultaneous growth of poly-Si from the center area of the trench, which resulted in maximizing the crystallized area from the crystal seed (i.e., trench edge) in both the waveguide and VGC regions. Nevertheless, since there were two crystal seeds in the trench, the coalescent boundary at the center of the trench was inevitable. After

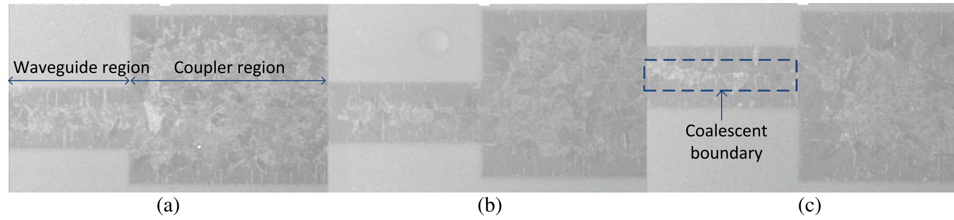

Fig. 3. SEM images after crystallization of deposited a-Si depending on annealing condition: (a) low, (b) medium, and (c) high temperature.

the completion of the epitaxial growth, the Si layer is patterned for the coupler or waveguide structure. The position of the waveguide needs to be determined carefully, because the crystalline quality degrades near the coalescent boundary, and the region near the trench edge increases the leakage into nearby silicon. Thus, we located the waveguide by separating it 1.5 μm away from the one of the trench edges, as shown in Fig. 4.

We measured the propagation loss of fabricated waveguides (more than five samples at each length) by using a cut-back method. The average and standard deviation of the waveguide loss were measured to be 6.1 dB and 0.55 dB/cm, respectively [18]. The waveguide loss was improved later to 3 dB/cm by SPE process optimization [19]. The coupling loss of the VGC was measured to be 7.1 dB/coupler, which was higher than the simulated value that did not include the additional loss of poly-Si in the 16 μm-wide trenches. The coupler loss was also improved to about 2.5 dB/port later through the insertion of a distributed Bragg reflector (DBR) in the bottom cladding [20,21]. The DBR layer reflected back the downward optical field toward the top surface and assisted more efficient coupling.

Another approach to crystallize amorphous silicon is the laser induced epitaxial growth (LEG). In this the liquid phase epitaxy method, a huge amount of radiation energy is absorbed by an amorphous Si layer during several tens to several hundreds of nanoseconds. As a result, the Si layer is melted and then recrystallized during the solidification [22].

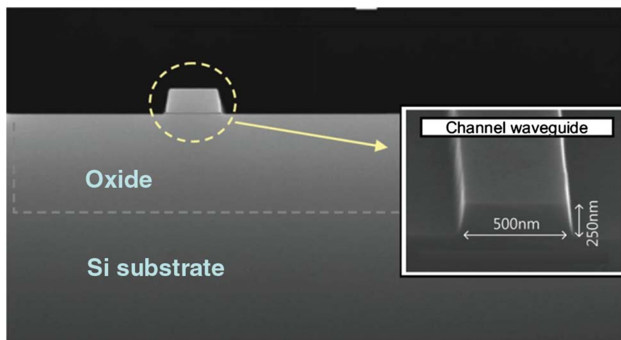

Fig. 4. VSEM images of fabricated waveguide on the bulk-Si substrate.

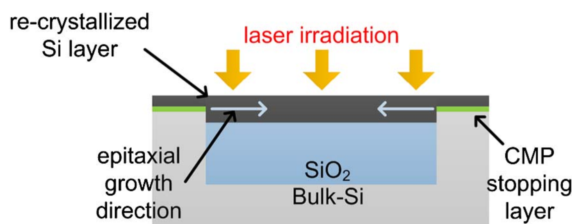

Fig. 5. Cross section of inlaid structure for LEG process.

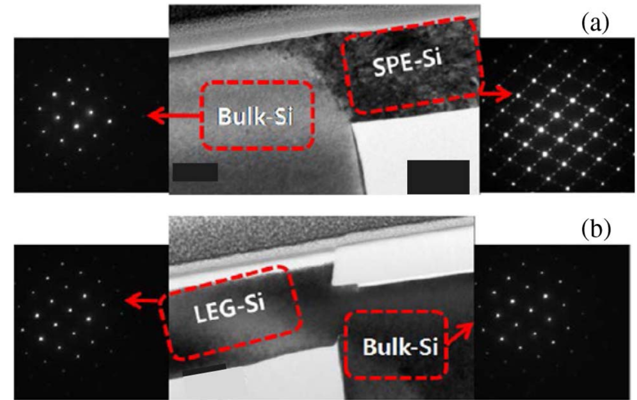

Fig. 6. High resolution TEM image and diffraction pattern: (a) SPE-Si and (b) LEG-Si.

Figure 5 shows an inlaid structure applied to the LEG process [23]. After the trench is formed and filled with silicon oxide, the a-Si is deposited by the LPCVD process. Unlike the SPE process, the lower boundary of the a-Si layer starts from below the top of the trench because the upper region of the a-Si generates a protrusive area during the melting process and is removed by chemical–mechanical polishing (CMP) later on. The LEG process is implemented by a frequency-doubled ($\lambda = 532$ nm) high-power pulsed Nd:YAG laser. During the LEG process, the epitaxial growth of a Si layer starts from the interface between the bulk-Si and a-Si and propagates laterally along the buried SiO_2 toward the center of the layer.

Figure 6 shows transmission electron microscopy (TEM) images at the cross section of the crystallized Si layer by SPE and LEG. The diffraction pattern at the SPE grown layer is revealed to be different from that of single crystal bulk-Si due to crystalline defects. In contrast, the TEM image of the LEG-Si is nearly the same as that of the bulk-Si substrate. The LEG process is expected to improve the waveguide loss and other performance of photonic devices.

B. Active Components: Modulator

The modulator is a device that converts the voltage or current change of an electrical signal to the change of output light intensity. Depending on the type of electron–photon interaction, modulators can be either electro-optical (EO) modulators or electroabsorption (EA) modulators. EO modulators are based on the index change caused by the carrier density change, while EA modulators are based on the field-induced absorption change. In terms of how the index change is related to the intensity change, EO modulators can be implemented by a

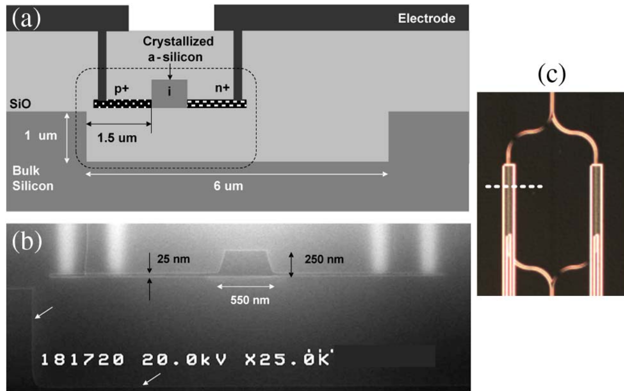

Fig. 7. (a) Cross-sectional diagram of the active part of the bulk-Si MZI modulator. (b) SEM image of the dotted region in (a). The inclined arrows indicate the boundary of the local oxide undercladding formed underneath the active part. (c) Microscope image. Dotted line indicates the location of (a) and (b).

Mach–Zehnder interferometer (MZI) type or by microring resonator (MRR) type. We describe the progress of both MZI modulators and MRR modulators.

The bulk-Si MZI modulator design follows that of typical carrier-injection-type p–i–n diodes except that the oxide undercladding is locally formed under the modulator [24]. A schematic diagram of the active part and an SEM image of the fabricated structure are shown in Figs. 7(a) and 7(b). The 500 nm × 250 nm waveguide cores were patterned from the SPE-Si area in the same way as in Section 2.A, except that the 25 nm-thick slabs are connected for carrier injection. The rest of the fabrication process followed the sequence of ion implantation (1×10^{20} cm^{-3} for $p+$ and $n+$ regions), upper cladding deposition, CMP, ohmic contact formation, and metallization. The p–i–n diode section length was 200 μm on both arms, shown in Fig. 7(c). Grating couplers were used for vertical light coupling between the modulator and cleaved optical fibers.

The forward on-resistance was measured to be ~60 Ω including the series resistance of the electrode. The optical on-chip loss was measured to be ~13 dB. The loss was presumably attributable to the ions laterally diffused into the waveguide core, imperfect crystallization in the SPE, and unwanted fabrication errors. The voltage for pi phase shift, $V\pi$, was 2.3 V with the 200 μm-long phase shifter section.

For AC measurements, a non-return-to-zero (NRZ) pseudo-random binary sequence (PRBS) signal from a pulse pattern generator (PPG) was applied to one arm of the MZI modulator. A 1550 nm laser light source was coupled to the modulator via the grating coupler. The modulated optical signal was amplified by an erbium-doped fiber amplifier and bandpass-filtered to remove the amplified spontaneous emission. Then, the eye diagram was observed by a digital communication analyzer (DCA) with a 20 GHz bandwidth.

Figure 8 compares the measured eye diagrams without [24] and with [25] de-emphasis of the PPG signal. For Fig. 8(a) without de-emphasis, the AC amplitude and DC bias were 1.8 V_{pp} and 0.8 V, respectively, corresponding to an energy efficiency of 2 pJ/bit. A clear eye diagram at 5 Gb/s was obtained with a PRBS length of 2^{31}–1. The same device can be driven using a de-emphasized signal to reduce intersymbol interference at the expensed of increased power consumption

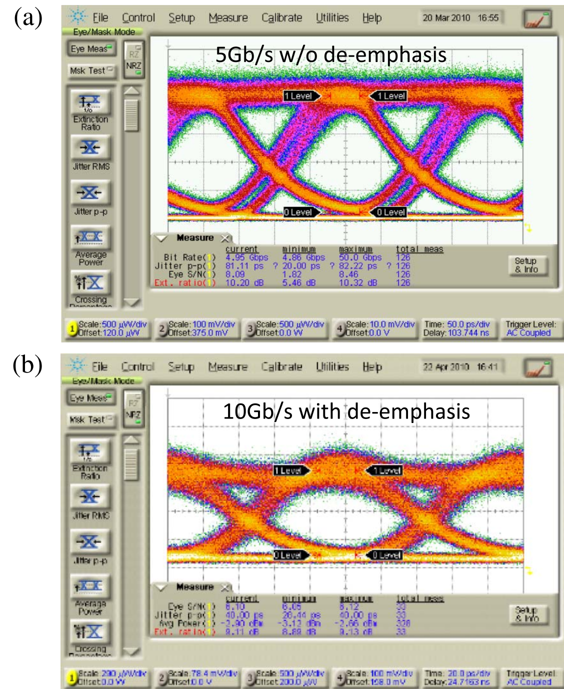

Fig. 8. Optical eye diagrams at NRZ 2^{31}–1 PRBS signal at (a) 5 Gb/s without de-emphasis and (b) 10 Gb/s with de-emphasis.

of driving circuitry. We achieved a 10 Gb/s eye diagram with the extinction ratio of >9 dB using 12 dB de-emphasis over a 4.2 V_{pp} driving signal, shown in Fig. 8(b) [25].

The bulk-Si MRR modulator is described in Fig. 9 with the lateral and vertical structure, which consist of the racetrack resonator and the phase shifter. The racetrack resonator has curved sections of 10 μm diameter and straight sections of 25 μm length as shown in Fig. 9(a). The gap and coupling length between the straight waveguide and the upper straight section of the racetrack were 400 nm and 25 μm, respectively. For modulating the refractive index of the racetrack resonator, the 10 μm-long straight phase shifter was embedded in the lower straight section of the racetrack with the 5 μm tapers in both ends. The cross-sectional structure of the phase shifter is

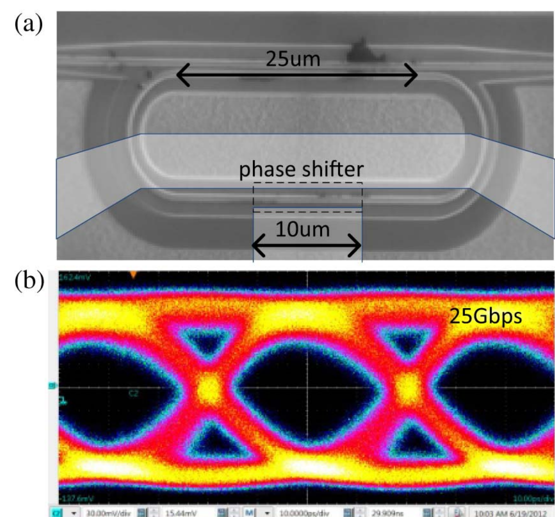

Fig. 9. (a) Lateral design of racetrack modulator with metal boundary illustrated. (b) Eye diagram at 1559.24 nm with 2.5 V_{pp} driving.

identical to that in MZI modulators. The measured eye diagram in Fig. 9(b) shows a clear open eye at 25 Gb/s when a de-emphasized 2.5 V_{pp} signal is applied to modulate the light input at a wavelength of 1559.24 nm [20]. The MRR modulator's small dimension enables modulating the light intensity with much smaller energy compared to the MZI modulator, although it may incur extra power consumption to fine-tune the resonance wavelength against process variation and temperature fluctuation.

C. Active Components: Photodetector

The photodetector is a device that converts input light intensity to electrical current. We introduce two different types of photodetector depending on how the light reaches the Ge: a surface-type photodetector and a waveguide-type photodetector. The surface-type photodetector can allow simpler process steps and larger alignment tolerance with fibers, while the waveguide-type photodetector is a mandatory component for wavelength division multiplexing or integration with electronics.

The surface-type photodetector accepts input light vertically from outside the device and generates photocurrent using a reverse-biased p–i–n junction, shown in Figs. 10(a) and 10(b) [26]. In the photodiode, a 1 μm-thick high-crystalline Ge layer was selectively grown on the 10^{20} cm^{-3} boron-doped bulk-Si substrate, and in turn, the 10^{20} cm^{-3} phosphorus-doped silicon capping layer was added. The diameter of the light-capturing region of the photodiode was 20 μm. The 1550 nm responsivity and dark current at −1 V were measured to be 0.3 A/W and 1 uA, respectively. At a reverse bias voltage of −1 V, a clean 25 Gb/s eye diagram was achieved [20], shown in Fig. 10(c).

The waveguide-type photodetector receives the optical signal from the Si waveguide that is laterally butt-coupled to the Ge region, as illustrated in Figs. 11(a) and 11(b). The light in the Si waveguide is coupled from the outside of the device through a VGC and propagates until it reaches the attached Ge region. The Ge region is grown directly on high-crystalline Si substrate after etching out the SPE-crystallized Si by a selective epitaxial growth (SEG) process. The Ge SEG starts about 200 nm below the bulk-Si top surface to make a good mode overlap between the Si waveguide and Ge and continues until the thickness becomes 600 or 800 nm [Fig. 11(c)].

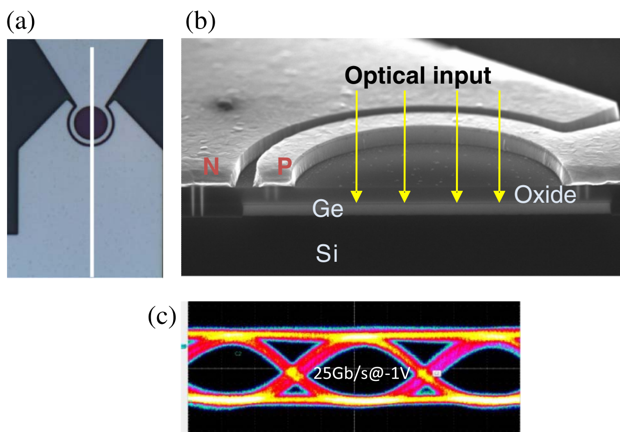

Fig. 10. (a) Microscope photography, (b) SEM image, and (c) 25 Gbp/s eye diagram of Ge/Si surface photodetector.

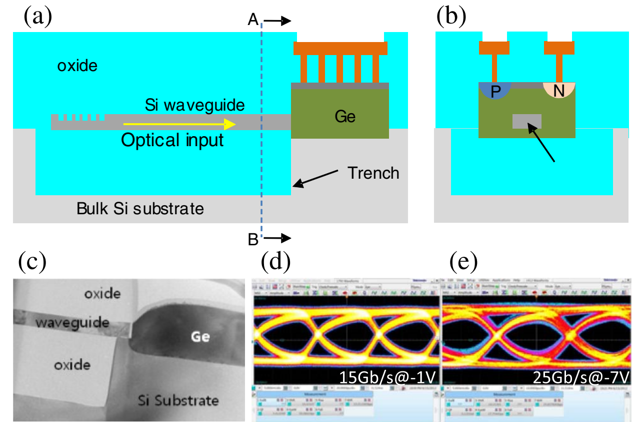

Fig. 11. Schematic diagram of waveguide-type photodetector (a) along the light propagation, and (b) perpendicular to the light propagation. (c) VSEM image, (d) 15 Gb/s eye diagram at −1 V bias, and (e) 25 Gb/s eye diagram at −7 V bias.

The Ge region measures 20 μm in length and 3 μm in width, which resulted in the responsivity of 1.05 A/W at 1550 nm and the dark current of 350 nA at −1 V bias. High-speed operation is characterized with eye diagrams in Figs. 11(d) and 11(e). At −1 V bias [Fig. 11(d)], a clear eye opening at 15 Gb/s was obtained, while at −7 V bias [Fig. 11(e)], the bit rate extended to 25 Gb/s with partial help of avalanche mechanism [27].

D. Integration with Electronics

Monolithically integrating photonics with electronics can provide invaluable advantages for lower cost and lower power consumption for many applications.

Figure 12 shows the lateral and vertical structures of the electronic photonic integrated circuits (EPICs) embedded in the DRAM periphery process, which is a DRAM process without a capacitor process. In order to minimize process perturbation, the DRAM cell section that takes most of wafer area remained unchanged, and only the periphery area was replaced with the EPIC. The fabricated 2.28 mm × 0.7 mm

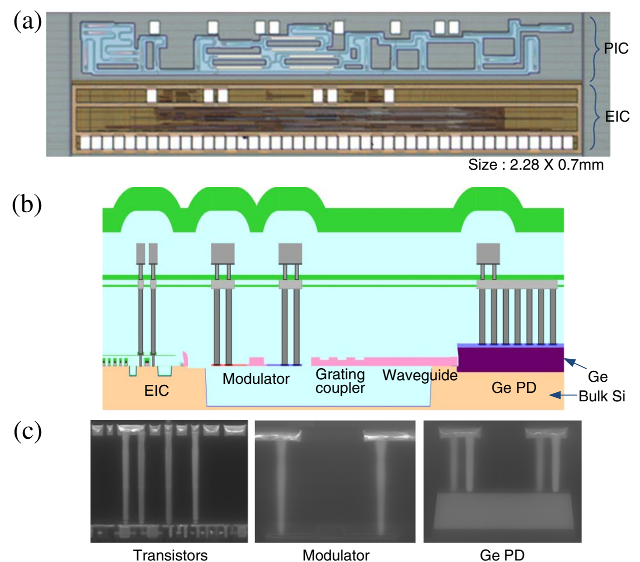

Fig. 12. (a) Optical microscope image of EPIC, (b) schematic of EPIC vertical structure, and (c) SEM images of transistors, modulator, and Ge photodiode.

EPIC section is shown in Fig. 12(a). The EPIC had the photonic IC (PIC) in the upper area and the electrical IC (EIC) in the lower area separately to avoid the design rule conflict between the PIC and EIC. It should be noted that the EPIC has very low pattern density, and its size can be substantially reduced later, for example by removing most electrical pads associated with testing and tuning circuits. Figure 12(b) schematically illustrates how photonic devices were integrated into the established DRAM vertical structure. While the waveguide, grating coupler, and modulator were fitted within the height of the DRAM periphery transistor gate stack, the Ge layer was temporarily thicker than the gate stack to facilitate optical coupling between the Si waveguide and Ge photodiode. The EPIC required two key process steps in addition to the DRAM process. The first step was the SPE process to fabricate the crystallized silicon layer on top of the oxide undercladding (Section 2.A.). The second step was the Ge SEG that grows a high-crystalline Ge layer on top of the bulk-Si surface. The EPIC was fabricated in a 300 mm DRAM line with a 65 nm technology node [20,28].

Figure 13 summarizes the performances of the bulk-Si photonic devices embedded in the EPIC. Compared to the PIC performances shown in Sections 2.A through 2.C, the EPIC photonic performances degraded, mainly due to the EIC process steps. The propagation loss of the EPIC waveguide increased from 0.3 to 2 dB/mm. Further research is in progress to explain the degradation, and we expect that the propagation loss can be reduced by process optimization. The coupling loss of the EPIC grating coupler increased from 2.5 dB/port to 7 dB/port mainly because the DBR structure was skipped for process simplicity at the moment. The EPIC modulator was the carrier-injection-type MZI modulator with de-emphasized driving [25]. This EPIC modulator performance was nearly equivalent to the PIC modulator performance, showing an open eye diagram at 10 Gb/s. The EPIC Ge photodiode was a reverse-biased p–i–n diode with a butt-coupled waveguide. The photodiode speed degraded down to 7 Gb/s in the EPIC, presumably due to unoptimized implantation processes. The electrical characteristics of the DRAM periphery transistors were verified by measuring threshold voltage (Vth), on-current (Ion), and on/off current ratio. At the first trial, the p-type metal-oxide-semiconductor degraded mainly due to dopant diffusion, which was later solved by optimizing implant scheme and heat budget to allow the three above-mentioned properties to be in the target window of the electronics-only process [28].

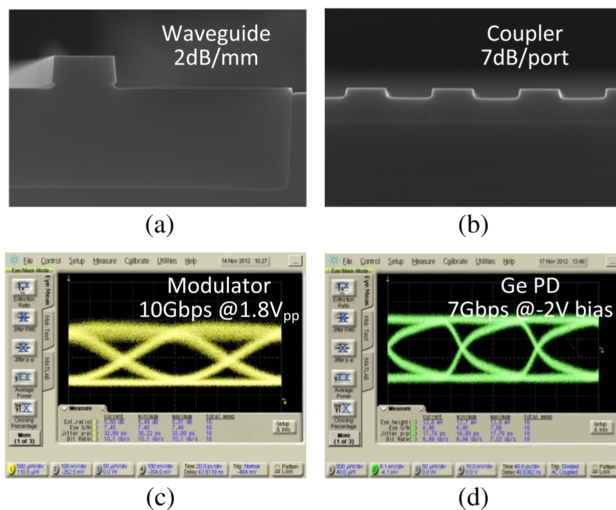

Fig. 13. Performance of the bulk-Si photonic devices integrated into the DRAM process.

3. OPTICAL LINK VERIFICATION

A. Possibility of Multidrop Bus Topology at 10 Gb/s

We tested a 1×4 optical link incorporating the bulk-Si MZI modulator operating up to 10 Gb/s on a die and 5 Gb/s in a quad flat package (QFP) [29]. Figure 14 shows the optical link constructed with the bulk silicon modulator and commercial photodetectors. The modulator was packaged in a 80-pin QFP with two vertically bonded fibers connecting to the external light source and the input port of the 1×4 fiber splitter. The packaged modulator was mounted on the Tx board with two modulator driver ICs. The outputs of the two driver ICs were combined with a 1 bit relative delay to provide a de-emphasized RF signal to the modulator up to 10 Gb/s [25]. The four-way split optical signals were received by four commercial avalanche photodetectors (APDs), and the electrical signals were monitored by a DCA.

Figure 15 shows the electrical eye diagram measured at the output of the APDs at 5 Gb/s with the modulator in the QFP

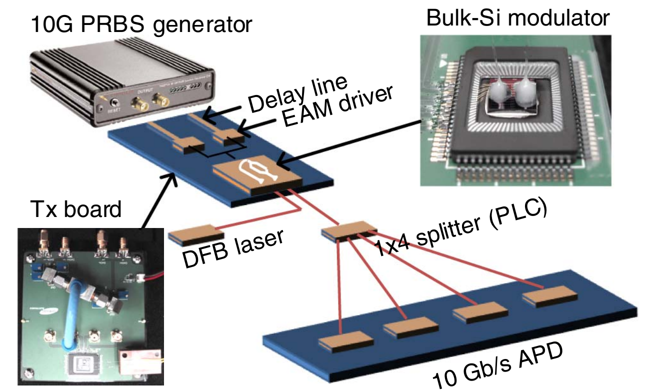

Fig. 14. 1×4 optical link configuration for multidrop memory bus.

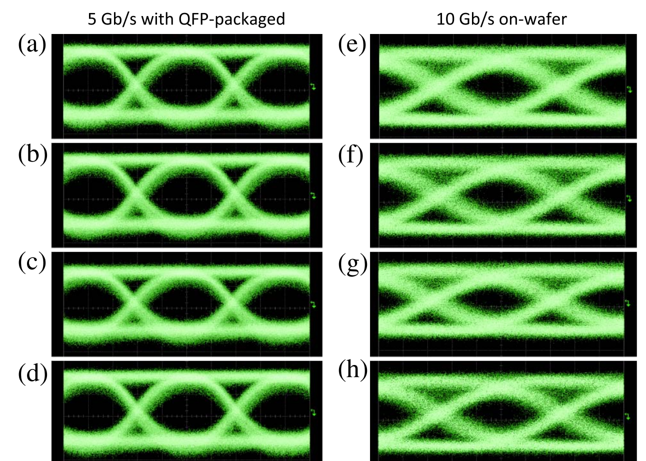

Fig. 15. Electrical eye diagram measured at channel 1–4 receiver: (a) through (d) with the transmitter in a QFP package, (e) through (h) on a bare die.

package {(a), (b), (c), (d)} and 10 Gb/s with the modulator on a bare die {(e), (f), (g), (h)}. The 10 Gb/s eyes with the packaged modulator were closed due to the limited bandwidth of the QFP package. The result clearly shows that the optical memory bus can support multiple memory modules up to, but not limited to, 10 Gb/s, which is in sharp contrast to the simulation result of the electrical memory bus as shown in Fig. 1.

B. Link Demonstration with Integrated PICs

We fabricated a PIC integrating the photonic devices introduced in Section 2 and verified the optical link operation [30]. Since the electronic and photonic integration technology was not available at the moment, the EIC die and PIC die were copackaged after going through separate process steps.

Figure 16 shows the block diagram of the transceiver module. The transceiver targets to transmit 8 bit data (DQ) signals, which are the fastest signals in the DRAM interface and are becoming a bottleneck to increase the number of multidrops at increased bandwidth. The transmitter circuit (Tx1 or Tx2) serializes four data signals from DRAM to generate one temporally multiplexed signal. External four-phase clocks provide the timing for the multiplexing. The serialized signal modulates the input light source through the modulator (MOD1 or MOD2). The modulated optical signal is coupled into a single-mode fiber through a grating coupler. The coupled light in the fiber propagates into a photodetector (PD1 or PD2) of another transceiver and converts it to electrical current through the photodetector. The receiver circuit (Rx1 or Rx2) senses the small current swing and restores it into four full-swing CMOS logic signals [31], which are transferred to DRAM data ports. The deserializer uses the four-phase clocks with adjustable delay to align with the first bit out of four bits. The transceiver contains two sets of Tx and Rx, and therefore transmits or receives eight data lanes in total. Tx and Rx in each channel share bidirectional DQ pads arbitrated by an externally controlled bidirectional switch.

Die photographs and a packaged transceiver chip are shown in Fig. 17. Both the PIC die and EIC die, measuring 4.5 mm × 4.5 mm and 2.3 mm × 0.4 mm, respectively, are fabricated using a 65 nm CMOS two-metal process. The PIC and EIC are copackaged onto a single 23 mm × 23 mm PCB and connected through bond-wires. The PCB top surface is covered with a detachable heat slug to attach 497 balls (100 balls populated) on the bottom side, and then the slug is removed to attach a 12-fiber array block to the PIC by active alignment for light coupling.

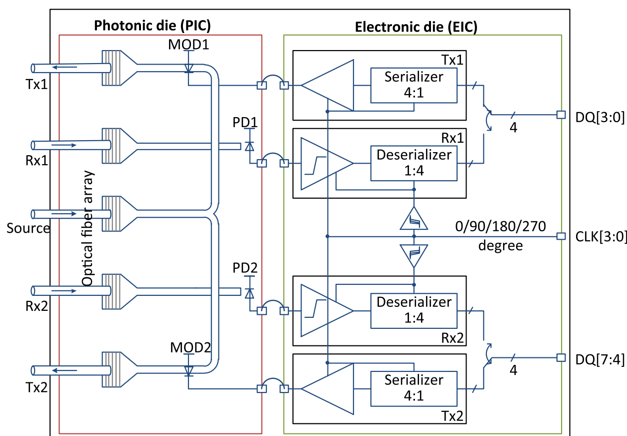

Fig. 16. Block diagram of an optical interconnect transceiver. PD: photodiode, MOD: modulator.

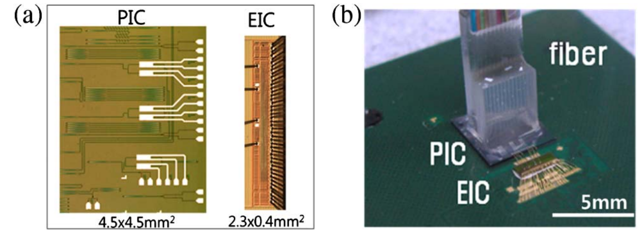

Fig. 17. (a) Photograph of dies for PIC and EIC. (b) Photograph of copackaged optical transceiver chip.

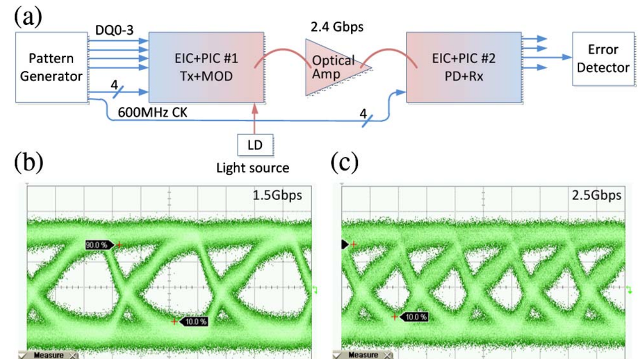

Fig. 18. (a) Experiment setup to verify link operation using two optical transceivers. (b) and (c) Eye diagram at the output of optical amplifier at data rate of 1.5 and 2.5 Gb/s.

The optical link is verified at various data rates using the setup in Fig. 18(a). A pattern generator provides four-channel data input to the first transceiver, and the serialized optical data output is converted to deserialized electrical signals by the second transceiver. To guarantee the DC balance of the optical signal, two channels' data are set to the inverse of the other two channels' data, which is equivalent to the Manchester line coding [32]. Bit error rate $<10^{-12}$ was confirmed using PRBS 2^{31}–1 pattern at a data rate of 2.4 Gb/s. We skipped the de-emphasis in order to increase the extinction ratio, and consequently the highest data rate was limited to about 3 Gb/s. The link introduces latency of about 180 ns, most of which is attributed to the propagation delay of the optical amplifier that was used to compensate the photonic device loss. Eye diagrams of optical signals at 1.5 and 2.5 Gb/s are also shown in Figs. 18(b) and 18(c), respectively.

4. DDR3 MEMORY ACCESS TEST

To verify memory read/write operation through the optical interface, two transceiver chips are inserted between the memory control board and the DRAM—one at the controller side and the other at the DRAM side, shown in Fig. 19. Optical amplifiers and splitters are inserted for both read/write paths to achieve enough optical power level at the receivers and to emulate a 1:4 multidrop bus, respectively. One DDR3 DRAM device is accessed through optically interconnected four data lanes and electrically interconnected signals including data strobe (DQS), command and address, and others. The timing

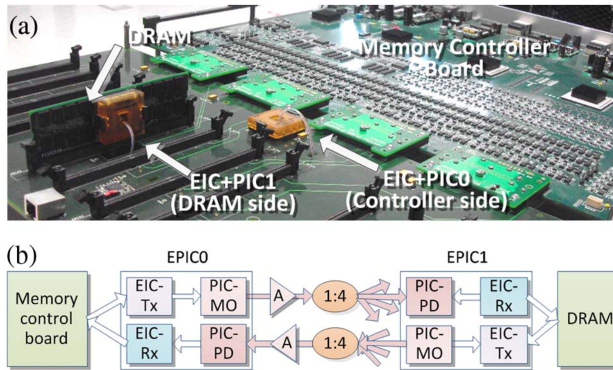

Fig. 19. (a) Photograph and (b) block diagram of the experiment setup to verify optically interconnected DRAM interface. A: optical amplifier.

skew between the optical signal path and the electrical signal path is removed by adjusting the path delay of the electrical signals through memory controller setting.

A 32 bit sequential data pattern, for each of four data lanes, is written to the DRAM over an optical channel through four consecutive eight-burst write commands synchronized to a 400 MHz control clock signal. Then, four consecutive eight-burst read commands are given to the DRAM at the same address, and the output data is verified to be same as written at the corresponding DQ pin.

Oscilloscope traces for DQ0 operation are shown in Fig. 20 with bidirectional control timing signals. Write and read operation sequences are indicated by numbers in yellow circles and green circles, respectively, shown in Fig. 20(a). Figure 20(b) illustrates the oscilloscope traces for DQ0, DQS, and output enable signal at both the memory controller side (upper graph) and DRAM side (lower graph). Over the sequence "1" through "2," the 32 bit data pattern is transferred from the controller to the DRAM, while the same data pattern is transferred back to the controller over the sequence "3" through "4." The fastest data transition per each data lane is 400 Mb/s, and the corresponding serialized data rate over the optical interconnect is 1.6 Gb/s. The read data of the four data lanes was verified to be exactly the same as the original pattern. First, the latencies from "1" to "2" and from "3" to "4" are 180 and 189 ns, respectively. The optical amplifier mostly

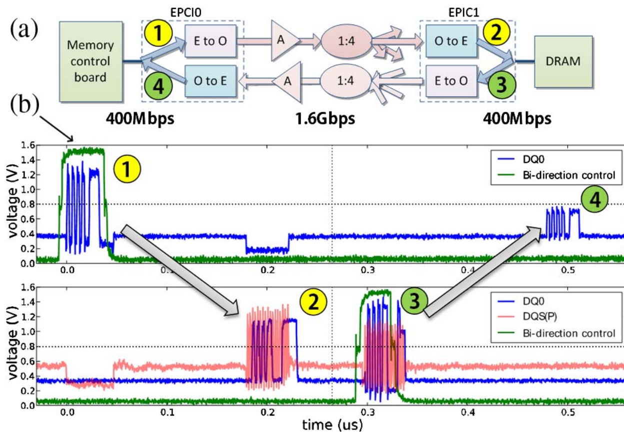

Fig. 20. (a) Block diagram of the experiment setup and (b) oscilloscope traces for DQ0 (blue) and DQS signals (red) at controller side and DRAM side with output enable signals (green).

contributes to the latency, while the latency of the transceiver circuit is estimated to be 3–4 ns. Second, the polarities of the data pattern in "2" and "3" are inverted from that in "1" and "4" because the modulator output power is blocked when the input data is logic high. The inversion of modulators does not affect the controller side operation because the inversion occurs two times and is cancelled out.

5. SUMMARY AND FUTURE DIRECTION

We presented photonics technology based on bulk-Si substrate for Si photonics applications including DRAM optical interface. Two different approaches, SPE and LEG, were addressed to implement the local-crystallized Si waveguide on bulk-Si substrate. Starting from the passive elements such as the waveguide and coupler, the progress on active devices including the modulator and photodetector was summarized. As the performance gap between the bulk-Si devices and the conventional SOI devices is gradually narrowing, the cost efficiency of the bulk-Si platform is becoming a larger advantage. The process of integration of PIC with EIC was demonstrated using a 65 nm DRAM periphery process on 300 mm wafers, which proved the possibility of being seamlessly integrated with various CMOS devices thanks to the homogeneous substrate. We used the bulk-Si photonic devices to show the feasibility of a high-speed multidrop interface, especially for CPU-DRAM interface. The MZI modulators and commercial APDs demonstrated four-drop operation at 10 Gb/s, and the optical transceivers using a DRAM-compatible process were fabricated and measured for 2.4 Gb/s serialized transmission. Finally, the transceiver chips were verified to work for a DDR3 DRAM interface at 1.6 Gb/s under a 1:4 multidrop configuration.

For a future research direction, we can consider the following three issues: first, in order to further reduce the optical link latency, supporting uncoded data is desired to remove the time for line coding such as 8b10b or 64b66b and to reduce the power consumption of transceivers that are always on. For this purpose, the photonic devices are expected to work over a broad frequency range for DC-coupled links. Second, we need to lower the loss of photonic devices to remove the optical amplifier in the link and, accordingly, reduce the latency and power consumption. Third, a cost-efficient way to align the fiber to the VGC should be devised, because otherwise expensive active alignment can delay the adoption of optical interconnects for the cost-sensitive memory interface application.

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