High-density and wide-bandwidth optical interconnects with silicon optical interposers [Invited]

Yutaka Urino,[1,2,*] Tatsuya Usuki,[1,2] Junichi Fujikata,[1,2] Masashige Ishizaka,[1,2] Koji Yamada,[1,2] Tsuyoshi Horikawa,[1,3] Takahiro Nakamura,[1,2] and Yasuhiko Arakawa[1,4]

[1]Institute for Photonics-Electronics Convergence System Technology (PECST), Japan
[2]Photonics Electronics Technology Research Association (PETRA), West 7 SCR, 16-1 Onogawa, Tsukuba, Ibaraki, Japan
[3]National Institute of Advanced Industrial Science and Technology, West 7 SCR, 16-1 Onogawa, Tsukuba, Ibaraki, Japan
[4]Institute of Industrial Science, The University of Tokyo, 4-6-1, Komaba, Meguro, Tokyo, Japan
*Corresponding author: y-urino@petra-jp.org

Received January 14, 2014; revised February 26, 2014; accepted February 27, 2014; posted February 27, 2014 (Doc. ID 204759); published April 11, 2014

One of the most serious challenges facing exponential performance growth in the information industry is the bandwidth bottleneck in interchip interconnects. We propose a photonics–electronics convergence system in response to this issue. To demonstrate the feasibility of the system, we fabricated a silicon optical interposer integrated with arrayed laser diodes, spot-size converters, optical splitters, optical modulators, photodetectors, and optical waveguides on a single silicon substrate. Using this system, 20 Gbps error-free data links and a 30 Tbps/cm^2 bandwidth density were achieved. This bandwidth density is sufficient to meet the interchip interconnect requirements for the late 2010s. © 2014 Chinese Laser Press

OCIS codes: (130.3120) Integrated optics devices; (200.4650) Optical interconnects; (230.0250) Optoelectronics.
http://dx.doi.org/10.1364/PRJ.2.0000A1

1. INTRODUCTION

The interchip bandwidths in personal computers and servers are doubling every two years [1]. Since, CPUs used for high-end servers currently have an overall interchip bandwidth of about 1.5 Tbps, which consists of 0.5 Tbps for the CPU–CPU interconnects, 0.4 Tbps for the memory, and 0.6 Tbps for the peripherals, the overall interchip bandwidth is expected to reach the 10-Tbps level by the late 2010s. Although the wiring pitches in logic circuits are expected to shrink exponentially in accordance with Moore's law, LSI I/O pad pitches, such as flip-chip pad pitches, are presently expected to remain large scale [2]. This is why the line speed for interchip interconnects in the future needs to be much higher than that for intrachip ones. The required line speed is estimated to exceed 40 Gbps by the late 2010s, and currently there are no known solutions for manufacturing electrical interconnects that can supply this speed [2]. Optical interconnects with silicon photonics are potential candidates for solving the bandwidth bottleneck problem [1,3–7] due to both the intrinsic properties of optical signals and the industrial advantages of silicon for use as resources in the electronics industry.

In this paper, in order to solve the bandwidth bottleneck problem in interchip interconnects by using silicon photonics, we examine photonics–electronics integration and light source integration for interchip optical interconnects, propose a photonics–electronics convergence system with a silicon optical interposer fully integrated with optical components on a single silicon substrate, investigate optical components for the optical interposers, and demonstrate the feasibility of our system through data link experiments with the silicon optical interposers.

2. PHOTONICS–ELECTRONICS CONVERGENCE SYSTEM FOR INTERCHIP INTERCONNECTS

A. Integration between Photonics and Electronics

Because the performance of electrical interconnects generally declines with their distance more rapidly than does that of optical interconnects, it is important to place optical transceivers (E/O and O/E signal converters) as close to LSIs as possible for wide-bandwidth interchip interconnects with photonic wiring. Silicon photonics is the most suitable technology for these applications because of its compactness and compatibility with LSIs.

Generally, there are three types of integration between photonic and electronic circuits with silicon photonics as shown in Fig. 1: front-end integration, back-end integration, and flip-chip bonding. In front-end integration, both electronic and photonic circuits are integrated near the surface of a silicon substrate by a front-end process. In back-end integration, photonic circuits are integrated on the wiring layer by a back-end process. In flip-chip bonding, electronics and photonics chips are fabricated separately and then stacked by flip-chip bonding. The first two are monolithic integrations and the last is a hybrid integration. Monolithic integration, especially front-end integration, is expected to provide higher speed and lower assembling cost than hybrid integration, but it requires very strict CMOS compatibilities in terms of design, fabrication, and testing. We think that it will be a long time before the technology is mature enough. In contrast, hybrid integration enables us to individually choose the most suitable technology nodes for photonics and electronics circuits, to design, fabricate, and test them separately and then combine

 © 2014 Chinese Laser Press

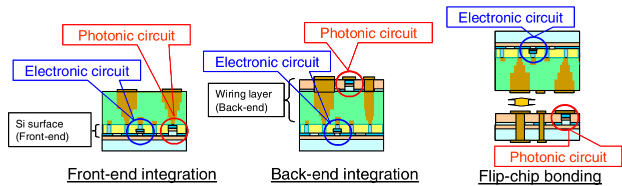

Fig. 1. Schematic cross sections of integration between photonics and electronics.

their good dies. This scheme can improve product yields and stimulate horizontal specialization between electronics and photonics or between LSI chips and their interchip interconnects. Therefore, since we think that the hybrid integration is the most practical choice both now and in the near future, we have taken the hybrid-integration route to photonic–electronic integration for interchip interconnects.

B. Light Source Integration

First, when considering the light source arrangement in our interchip optical interconnects, we had to choose between off-chip or on-chip sources. Although off-chip light sources are the more flexible of the two, they require highly precise optical connectors and care for polarization dependence to obtain optical power from the off-chip light sources into the substrate via optical fibers. Because we think that this is not practical for large scale interconnects, we have chosen on-chip light sources, which require neither optical connecters nor special care for polarization dependence. There are two types of integrations for on-chip light sources: monolithic integration with silicon or germanium lasers and hybrid integration with compound semiconductor lasers. Because the efficiency and output power of monolithically integrated Ge-on-Si lasers are still low for interchip interconnect applications [8], we have chosen hybridly integrated lasers. There are two types of compound semiconductor lasers for optical interconnects: edge emitting lasers and vertical cavity surface emitting lasers (VCSELs). Because VCSELs cannot maintain single mode operation when the optical output is high, we have chosen edge-emitting lasers. There are also two types of hybrid lasers in terms of optical coupling structures between the active waveguide and the silicon waveguide: evanescent-coupled lasers [9] and butt-coupled lasers [10]. The evanescent-coupled lasers have higher tolerance against alignment error when the compound semiconductor chips are mounted on the silicon substrate than the butt-coupled ones. However, we have found that the bandwidth density and power consumption per channel in laser diodes (LDs) can be improved by using a branching configuration, in which the light from a single LD is divided and distributed to many channels [11], and we think the efficiency and output optical power of the evanescent-coupled lasers are not high enough for the branching configuration. We have therefore chosen to use butt-coupled hybrid lasers for interchip interconnect applications and have developed spot-size converters (SSCs) between LDs and silicon optical waveguides to relax the alignment tolerance as will be mentioned later.

C. Conceptual Model

Based on the above examinations, we previously proposed a photonics–electronics convergence system for interchip interconnects [6,12]. A conceptual model of the system is shown in Fig. 2. The upper-left LSI chip on the silicon substrate has been removed to enable the substrate surface area that it covered to be seen. Optical modulators and photodetectors (PDs) are monolithically integrated on a silicon substrate, arrayed LDs are hybridly integrated on the substrate, and these optical components are optically linked to each other by silicon optical waveguides and splitters. LSI bare chips are mounted on the substrate using flip-chip bonding and are electrically connected to the optical modulators and PDs. We call the silicon substrate a “silicon optical interposer.” The interchip interconnects with the silicon optical interposers operate as follows. Arrayed LDs are driven simultaneously by DC current. The CW light from each LD is divided by an optical splitter and launched into an optical modulator. The optical modulators are directly driven by transmitter circuits in one LSI. The modulated optical signals propagate along interchip optical waveguides and are the input for PDs under another LSI. The electrical signals from those PDs are the input for receiver circuits in the LSI that the PDs are under. The hybridly integrated LDs are capable of high optical output power and a multiple-channel distribution. The hybrid integration between photonics and electronics allows us to individually choose the most suitable technology nodes for the photonics and electronics, respectively.

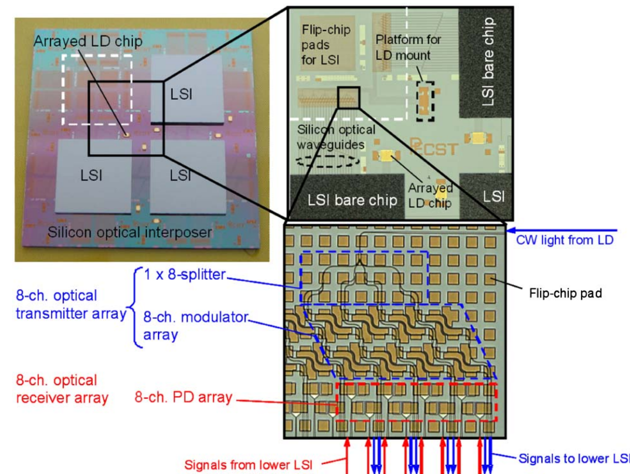

Fig. 2. Conceptual model of photonics–electronics convergence system for interchip interconnects.

This system enables us to replace the conventional electronic wires on a printed circuit board (PCB) with the optical interconnects on a silicon substrate one hundredth the size of a PCB. This silicon optical interposer has wide bandwidth capabilities due to the properties of its optical signals. Since the silicon substrates can be fabricated using a CMOS-compatible process, they have quite high density and are low in cost. Furthermore, users do not have to worry about any optical issues (such as optical coupling, optical reflection, or polarization dependence) because this system is optically complete and closed without needing any optical inputs or outputs.

3. CONFIGURATION AND CHARACTERISTICS OF OPTICAL COMPONENTS

To demonstrate the feasibility of the photonics–electronics convergence system, we fabricated a high-density silicon optical interposer that mainly consisted of silicon optical

waveguides, silicon optical modulators, germanium PDs, LDs, and SSCs. The configurations and characteristics of these optical components were investigated as follows.

A. Silicon Optical Waveguides

Generally, there are two types of silicon optical waveguides in terms of their core cross section shapes: rib-shaped and rectangular. The propagation loss of the rib-shaped waveguides is lower than that of the rectangular ones, but the rib-shaped waveguides pose difficulties in the fabrication process in that we have to stop etching the silicon layer to leave a precisely thin silicon slab. We think this issue is critical in terms of yields in mass production, especially (as will be explained later) for the yields of optical modulators. We have therefore chosen rectangular core waveguides for our silicon optical interposers and have developed fine processes for low-loss rectangular core waveguides. The developed processes mainly consist of multiple exposure technique in variable-shaped-beam (VSB) electron beam (EB) lithography and optimization of EB resist and etching processes. By applying these techniques, the field stitching error and line edge roughness (LER) were drastically reduced to 7.9 and 1.9 nm, respectively [13].

Figure 3 shows the core width dependence of the propagation loss for TE modes at the 1550 nm wavelength. The core height was 220 nm. The propagation losses were nearly constant and less than 2 dB/cm regardless of their core width. Such small core width dependence implies that scattering loss caused by the side-wall roughness is negligible in our rectangular core waveguides.

B. Silicon Optical Modulators

There has been a lot of research on silicon optical modulators using the carrier plasma effect in PIN or PN diodes, most of it focused on using a doped silicon slab in the rib-shaped waveguides to make electric contact between the waveguide core and metal electrodes [14–16]. In these cases, the gap between P- and N-doping areas should be wider than the width of the optical mode profile to prevent optical absorption loss due to the highly doped carriers. The optical mode profile in these rib-shaped waveguides extended to the slab area, and a thicker slab caused a wider mode profile and P-N gap. The wider P-N gap made the resistivity higher and the modulation efficiency and modulation speed lower. Because optical modulator characteristics such as optical loss, modulation efficiency, and speed are sensitive to the slab thickness in this way, we had to stop etching the silicon layer to leave a precisely thin silicon slab. To overcome these design and fabrication difficulties, we have proposed a structure for the electric contact between the waveguide core and electrodes to be used instead of the silicon slab. Figure 4(a) is a schematic of the structure of our proposed optical modulator [17], which is a Mach–Zehnder interferometer (MZI) composed of phase shifters and multimode interference (MMI) couplers. The phase shifters, which have side-wall gratings on both sides of the waveguide core in order to enable electric contact between the core and metal electrodes, can change their refractive indices by the carrier plasma effect in lateral PIN diode structures. Figure 4(b) shows microscope and SEM images of the fabricated modulator. Because the waveguides and side-wall gratings had a uniform thickness of silicon over the entire modulator, the etching process was much easier than that with rib-shaped waveguides. Moreover, this structure enabled stronger lateral optical mode confinement, a narrower optical mode profile, a narrower P-N gap, lower resistivity, higher efficiency, and higher speed than the modulators with rib-shaped waveguides. The pitch of the side-wall grating was designed so that the stop-band wavelength was much shorter than the operation wavelength to prevent the diffraction by the gratings. The interaction length of the phase shifter (L) was 200 μm.

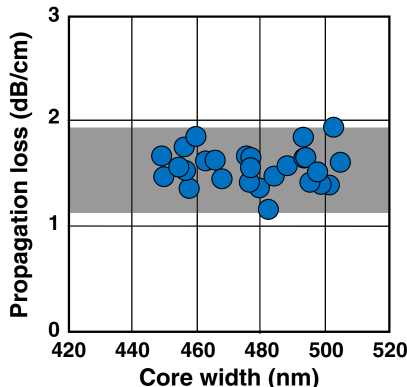

Fig. 3. Core width dependence of the waveguide propagation loss.

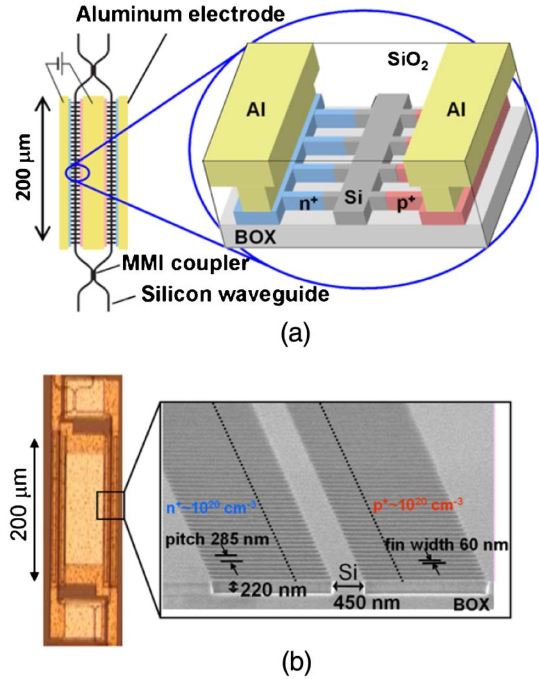

Fig. 4. Schematic structure and images of the optical modulator.

The measured DC response of the optical modulator is plotted in Fig. 5. The π-phase shift voltage ($V\pi$) was 0.30 V and the modulation efficiency ($V\pi * L$) was 0.006 Vcm, which is twice as high as the efficiency of our previous modulator with rib-shaped waveguides [6]. The extinction ratio was 12.4 dB. Since the frequency response of the modulator is similar to that of a series resistor–capacitor (RC) circuit, we used pre-emphasis to compensate for the frequency response. The 3 dB bandwidth with the pre-emphasis was estimated to be 12.5 GHz [17].

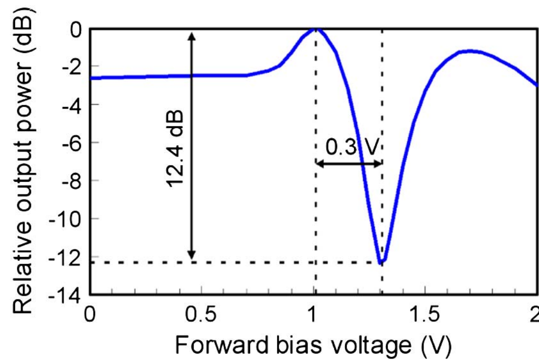

Fig. 5. DC response of the optical modulator.

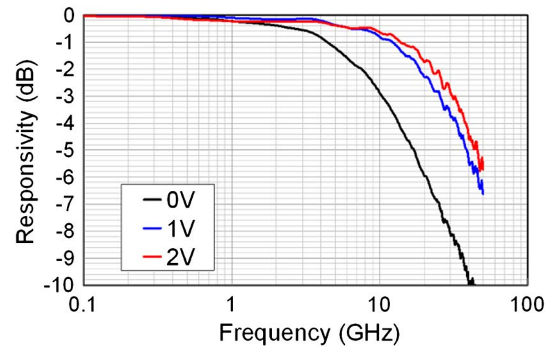

Fig. 7. Frequency responses of the PDs.

C. Germanium Photodetectors

There are generally two types of germanium PDs that we can monolithically integrate on a silicon substrate: PIN-PDs and metal-semiconductor-metal (MSM) PDs. MSM-PDs require fewer fabrication steps but finer patterning and alignment than PIN-PDs. In this work we fabricated PIN-PDs for the silicon optical interposers [18]. Figure 6(a) shows the schematic structure of our germanium PIN-PD, and Fig. 6(b) shows its SEM image. The measured frequency responses of PDs with 0-, 1-, and 2-V biases are plotted in Fig. 7. The 3-dB cutoff frequencies were 10 GHz with a 0 V bias voltage and 26 GHz with a 1 V bias voltage. The dark current was 1 μA with a 1 V bias voltage.

D. Arrayed Laser Diodes

Figure 8 shows the microscope image of a 13-channel arrayed LD chip (bottom side) to be mounted on the silicon optical interposer. It was an InGaAsP LD array with a 30 μm channel pitch. Each channel was a Fabry–Perot type LD with a SSC [10]. The cavity length was 400 μm. The chip had a single pair of electrodes for all 13 channels, each of which simultaneously emitted 1530 nm light. The chip also had a pair of alignment marks for a passive alignment technique [19]. The near field pattern and output intensity of the 13-channel arrayed LD are shown in Fig. 9. The output power uniformity across all channels was better than 0.7 dB.

Fig. 8. Microscope image of the 13-channel arrayed LD.

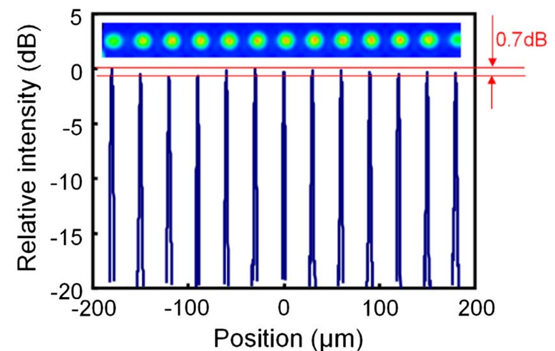

Fig. 9. Near field pattern and output intensity of the LD array.

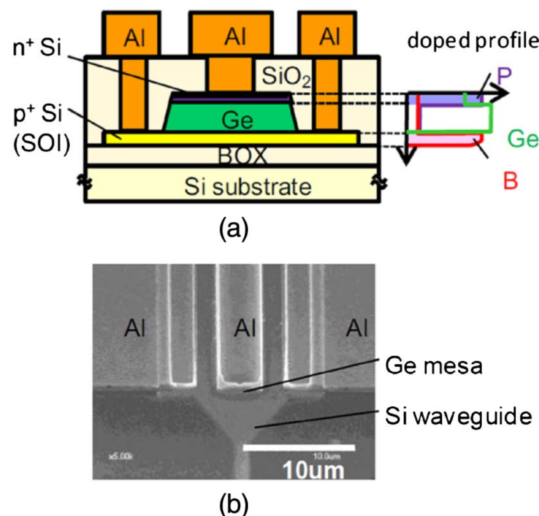

Fig. 6. Schematic structure and SEM image of the PIN-PD.

E. Spot-Size Converters

SSCs between the LDs and silicon optical waveguides are key components for the silicon optical interposers in terms of their optical power budget and fabrication process simplicity. We previously used three types of SSC: tapered silicon waveguide; inversed taper silicon waveguide; and SiON waveguide. Although the first two did not need additional processes, the first had a large coupling loss [6] and the second had a very small process margin, as will be shown later. The third type had a low coupling loss but needed additional processes [10]. We subsequently introduced a SSC called a trident [20], the schematic structure and SEM images of which are shown in Fig. 10. It consists of only three narrow silicon waveguides fabricated without additional processes.

Figure 11 shows the measured coupling losses of the trident SSC and an inversed taper SSC with various silicon core tip widths (w). The coupling loss of the trident SSC was low and

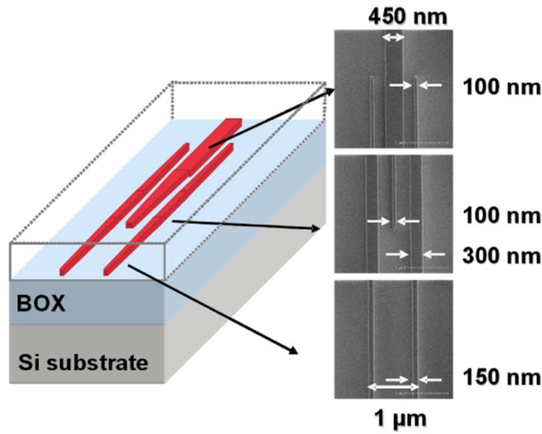

Fig. 10. Schematic structure and SEM images of the trident SSC.

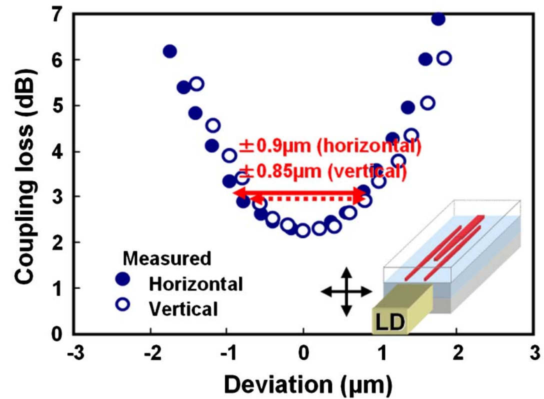

Fig. 12. Coupling losses between the LD and the trident SSC with various alignment deviations in the horizontal and vertical directions.

insensitive to its tip width unlike the inversed taper SSC. The sensitivity difference can be explained as follows. The spot size of the inversed taper SSC is quite sensitive to its tip core width due to its weak optical mode confinement. Such narrow core width is usually difficult to pattern precisely due to side etching. In contrast, the spot-size of the trident SSC is not so sensitive to its core width but mainly sensitive to its core pitch near the tip. This pitch is not changed by side etching. Therefore, the trident SSC is quite tolerant to the patterning errors of the core.

Measured coupling losses between the LD and the trident SSC with various alignment deviations in the horizontal and vertical directions are plotted in Fig. 12. The minimum coupling loss was as low as 2.3 dB, and the alignment error tolerance up to a 1 dB loss increase was about ±0.9 μm in both directions, which was large enough for our alignment precision (±0.5 μm) with passive alignment technique [19].

4. DESIGN AND FABRICATION OF SILICON OPTICAL INTERPOSERS

As mentioned earlier, LSI bare chips are supposed to be mounted on the interposer using flip-chip bonding. ITRS projections have indicated that the pitches of flip-chip pad arrays should stop shrinking at around 100 μm [2]. Therefore, we designed our silicon optical interposers so that the pad pitches of our optical modulators and PDs were 100 μm. We used 1×4 MMI couplers as the optical splitters for the branching configuration.

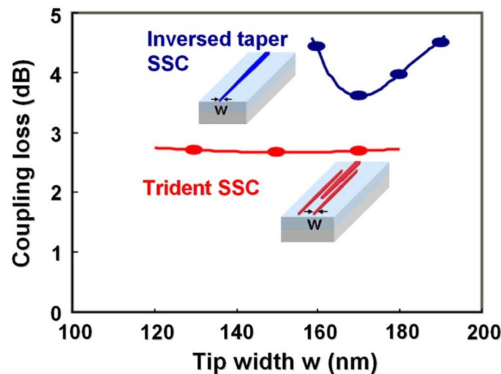

Fig. 11. Coupling losses of the trident SSC and an inversed taper SSC with various silicon core tip widths.

The silicon optical interposers were fabricated from 4 in. (100 mm) silicon-on-insulator (SOI) wafers in the Super Clean Room at AIST Tsukuba West by CMOS process technology. The thicknesses of the buried oxide layer and the SOI layer were 3 μm and 220 nm, respectively. The silicon optical waveguide cores, as well as trident SSCs, 1×4 MMI couplers, MZIs, and side-wall gratings for the modulators were formed by VSB-EB lithography and dry etching. Lateral PIN junctions for the modulators and the vertical PIN junctions for the PDs were formed by B and P ion implantations. Epitaxial germanium mesas for the PDs were selectively grown on the silicon cores by chemical vapor deposition (CVD). All of the components were covered with a SiO_2 upper cladding layer by CVD. Contact holes and metal electrodes were formed by dry etching. The waveguide end-faces, pedestals, and alignment marks for LD mounting were formed by dry etching. Finally, the arrayed LD chips were mounted on the pedestals using a passive alignment technique [19]. As a result, the LD array was butt-coupled to the silicon waveguide array via the trident SSC array.

The I-L characteristics of the LDs measured without temperature control are plotted in Fig. 13, where the blue solid line indicates the I-L characteristics of the 13-ch. arrayed LD hybridly integrated on the interposer and the red broken line indicates those of a 1-ch. LD mounted on a heat sink. Since all 13 channels were driven simultaneously, the actual current injected into the arrayed LD chip was 13 times the value in the horizontal axis. Although the heat generation in the 13-ch. LD was 13 times as high as that in the 1-ch.

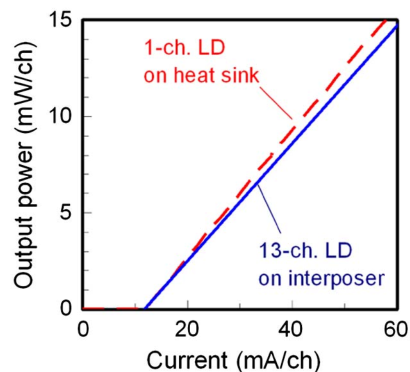

Fig. 13. I-L characteristics measured without temperature control.

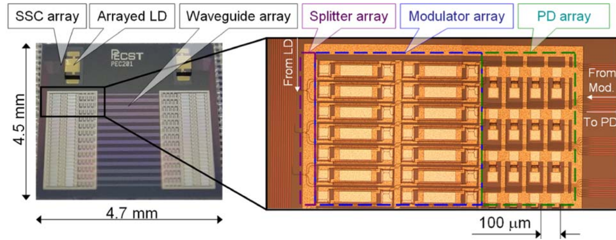

Fig. 14. Fabricated silicon optical interposer.

LD, both I-L characteristics had about the same threshold currents and slope efficiencies, and there were no output power saturations up to 15 mW or more per channel. This suggests that the hybridly integrated arrayed LD has quite a high heat dissipation capability. We consider these high output power and high heat dissipation capabilities to indicate the superiority of our butt-coupled hybrid lasers over evanescent-coupled ones.

A photograph of one of our fabricated silicon optical interposers is shown in Fig. 14. The substrate was 4.7×4.5 mm. Two 13-ch. arrayed LD chips were hybridly integrated on the silicon substrate, and 26 trident SSCs, 26 1×4 optical splitters, 104 optical modulators, 104 interchip optical waveguides, and 104 PDs were monolithically integrated on the substrate. The unit cells of the modulator and PD were 400×100 μm and 200×100 μm, respectively. They were tiled so that their pad pitches were 100 μm. Two LSI bare chips are supposed to be mounted on the right and left sides of the substrate using flip-chip bonding to optically connect them to each other.

5. DATA LINK EXPERIMENTS USING SILICON OPTICAL INTERPOSERS

We performed data link experiments as follows. All 13 channels of the arrayed LD were simultaneously driven by a single DC current. The CW light from the LD was a wavelength of 1530 nm and a TE-like mode. It was coupled to the silicon optical waveguide by the trident SSC and then divided into four by the 1×4 optical splitter, and each of them was launched into the optical modulator. RF input signals were pre-emphasized by a differentiator composed of passive RC circuits and drove the modulator. The voltage amplitude after pre-emphasis was 3.5 V peak to peak. The modulated optical signals propagated along the interchip optical waveguides and were then input to the PD and converted into electrical signals.

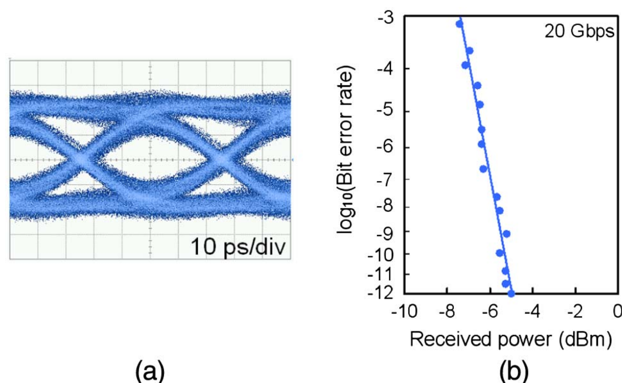

Fig. 15. Eye diagram and BERs of PD output at 20 Gbps.

Table 1. Per-Channel Footprints of Optical Components.

Component	Footprint
Laser diode	0.0077 mm^2
Optical modulator	0.0400 mm^2
Photodetector	0.0200 mm^2
Total	0.0677 mm^2

The measured eye diagram of the PD output at 20-Gbps NRZ with a $2^7 - 1$ pseudorandom binary sequence (PRBS) is shown in Fig. 15(a). The clear eye opening indicates that the optical links were capable of a 20-Gbps data transmission. The measured bit error rates (BERs) for the 20-Gbps PRBS are plotted in Fig. 15(b). We confirmed that the BER was less than 10^{-12} when the received power of the PD was larger than −5 dBm. An error-free data link at 20 Gbps via the 1×4 optical splitter was achieved. These results demonstrate that this silicon optical interposer is capable of a 2.1-Tbps bandwidth for interchip optical interconnects.

The footprints of the optical components per link channel are listed in Table 1. The total footprint was 0.0677 mm^2 per channel, meaning we could achieve a bandwidth density of 30 Tbps/cm^2 with a channel line rate of 20 Gbps. To our knowledge, this is the highest bandwidth density for an interchip optical interconnect in the world. Since the typical CPU die is about 2 cm^2 in area, we can obtain an overall interchip bandwidth at the level of several tens of Tbps by using the silicon optical interposers, which is sufficient for the required bandwidth in the late 2010s.

Since this system is optically complete and closed and no temperature sensitive components are used, we did not need to align the fibers, control the polarization, or control the temperature throughout the experiments.

6. CONCLUSIONS

We developed a photonics–electronics convergence system with a silicon optical interposer in order to solve the bandwidth bottleneck problem facing interchip interconnects. We examined integration between photonics and electronics and integration between light sources and silicon substrates and then fabricated a conceptual model of the proposed system based on the results of these examinations. We also investigated the configurations and characteristics of the optical components of the silicon optical interposer, including silicon optical waveguides, silicon optical modulators, germanium PDs, arrayed LDs, and SSCs. We then demonstrated the feasibility of the system with a high-density optical interposer fabricated by using silicon photonics integrated with these optical components on a single silicon substrate. Using this silicon optical interposer enabled us to achieve error-free data links at a 20-Gbps line rate and a high bandwidth density of 30 Tbps/cm^2. We believe this technology will solve the bandwidth bottleneck problem because the bandwidth density is sufficient to meet the interchip interconnect requirements for the late 2010s.

For practical applications, the interposers should be usable under high temperature conditions so that they can cope with the heat generated by the mounted LSIs. Since the LSI bare chips are mounted near the LDs, the LDs are expected to suffer from the heat. To overcome the heat problem, we

are also developing temperature insensitive light source with quantum dot lasers for the system [21]. We plan to demonstrate silicon optical interposers with quantum dot lasers in the near future.

Although we used 4 in. (100 mm) wafers and EB lithography for fabricating the prototypes of the interposers in this work, we are also developing fabrication processes and devices using 300 mm wafers and ArF immersion lithography for future mass production and higher performance [22–24].

ACKNOWLEDGMENTS

This research is supported by the Japan Society for the Promotion of Science (JSPS) through its "Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program)." A part of the fabrication was conducted at the Nano-Processing Facility, AIST.

REFERENCES

1. I. A. Young, E. M. Mohammed, J. T. S. Liao, A. M. Palermo, B. A. Block, M. R. Reshotko, and P. L. D. Chang, "Optical technology for energy efficient I/O in high performance computing," IEEE Commun. Mag. **48**(10), 184–191 (2010).
2. International Technology Roadmap for Semiconductors 2009 Edition, Assembly and Packaging, Table AP2 and AP3, http://www.itrs.net/Links/2009ITRS/2009Chapters_2009Tables/2009Tables_FOCUS_E_ITRS.xls.
3. L. Chen, K. Preston, S. Manipatruni, and M. Lipson, "Integrated GHz silicon photonic interconnect with micrometer-scale modulators and detectors," Opt. Express **17**, 15248–15256 (2009).
4. K. Raj, J. E. Cunningham, R. Ho, X. Zheng, H. Schwetman, P. Koka, M. McCracken, J. Lexau, G. Li, H. Thacker, I. Shubin, Y. Luo, J. Yao, M. Asghari, T. Pinguet, J. Mitchell, and A. V. Krishnamoorthy, "'Macrochip' computer systems enabled by silicon photonic interconnects," Proc. SPIE **7607**, 760702 (2010).
5. G. Kim, J. W. Park, I. G. Kim, S. Kim, S. Kim, J. M. Lee, G. S. Park, J. Joo, K. S. Jang, J. H. Oh, S. A. Kim, J. H. Kim, J. Y. Lee, J. M. Park, D. W. Kim, D. K. Jeong, M. S. Hwang, J. K. Kim, K. S. Park, H. K. Chi, H. C. Kim, D. W. Kim, and M. H. Cho, "Low-voltage high-performance silicon photonic devices and photonic integrated circuits operating up to 30 Gb/s," Opt. Express **19**, 26936–26947 (2011).
6. Y. Urino, T. Shimizu, M. Okano, N. Hatori, M. Ishizaka, T. Yamamoto, T. Baba, T. Akagawa, S. Akiyama, T. Usuki, D. Okamoto, M. Miura, M. Noguchi, J. Fujikata, D. Shimura, H. Okayama, T. Tsuchizawa, T. Watanabe, K. Yamada, S. Itabashi, E. Saito, T. Nakamura, and Y. Arakawa, "First demonstration of high density optical interconnects integrated with lasers, optical modulators and photodetectors on single silicon substrate," Opt. Express **19**, B159–B165 (2011).
7. X. Zheng, Y. Luo, J. Lexau, F. Liu, G. Li, H. Thacker, I. Shubin, J. Yao, R. Ho, J. E. Cunningham, and A. V. Krishnamoorthy, "2-pJ/bit (On-Chip) 10-Gb/s digital CMOS silicon photonic link," IEEE Photon. Technol. Lett. **24**, 1260–1262 (2012).
8. R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, "An electrically pumped germanium laser," Opt. Express **20**, 11316–11320 (2012).
9. A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," Opt. Express **14**, 9203–9210 (2006).
10. T. Shimizu, N. Hatori, M. Okano, M. Ishizaka, Y. Urino, T. Yamamoto, M. Mori, T. Nakamura, and Y. Arakawa, "High density hybrid integrated light source with a laser diode array on a silicon optical waveguide platform for inter-chip optical interconnection," in *Proceedings of IEEE International Conference on Group IV Photonics* (IEEE, 2011), pp. 181–183.
11. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, and Y. Arakawa, "2.2 pJ/bit operation of hybrid integrated light source on a silicon optical interposer for optical interconnection," in *Proceedings of IEEE Photonic Conference* (IEEE, 2013), pp. 254–255.
12. Y. Arakawa, T. Nakamura, Y. Urino, and T. Fujita, "Silicon photonics for next generation system integration platform," IEEE Commun. Mag. **51**(3), 72–77 (2013).
13. N. Hirayama, H. Takahashi, Y. Noguchi, M. Yamagishi, and T. Horikawa, "Low-loss Si waveguides with variable-shaped-beam EB lithography for large-scaled photonic circuits," in *Extended Abstracts of the International Conference on Solid State Devices and Materials* (JSAP, 2012), pp. 530–531.
14. L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "40 Gbit/s silicon optical modulator for high speed applications," Electron. Lett. **43**, 1196–1197 (2007).
15. D. J. Thomson, F. Y. Gardes, Y. Hu, G. Mashanovich, M. Fournier, P. Grosse, J.-M. Fedeli, and G. T. Reed, "High contrast 40 Gb/s optical modulation in silicon," Opt. Express **19**, 11507–11516 (2011).
16. P. Dong, L. Chen, and Y.-k. Chen, "High-speed low-voltage single-drive push-pull silicon Mach–Zehnder modulators," Opt. Express **20**, 6163–6169 (2012).
17. S. Akiyama, T. Baba, M. Imai, T. Akagawa, M. Takahashi, N. Hirayama, H. Takahashi, Y. Noguchi, H. Okayama, T. Horikawa, and T. Usuki, "12.5-Gb/s operation with 0.29-V•cm VπL using silicon Mach–Zehnder modulator based-on forward-biased pin diode," Opt. Express **20**, 2911–2923 (2012).
18. J. Fujikata, M. Miura, M. Noguchi, D. Okamoto, T. Horikawa, and Y. Arakawa, "Si waveguide-integrated metal–semiconductor–metal and p-i-n-type Ge photodiodes using Si-capping layer," Jpn. J. Appl. Phys. **52**, 04CG10 (2013).
19. N. Fujioka, T. Chu, and M. Ishizaka, "Compact and low power consumption hybrid integrated wavelength tunable laser module using silicon waveguide resonators," J. Lightwave Technol. **28**, 3115–3120 (2010).
20. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, and Y. Arakawa, "A novel spot size convertor for hybrid integrated light sources on photonics-electronics convergence system," in *Proceedings of IEEE International Conference on Group IV Photonics* (IEEE, 2012), pp. 171–173.
21. N. Hatori, T. Shimizu, M. Okano, M. Ishizaka, T. Yamamoto, Y. Urino, M. Mori, T. Nakamura, and Y. Arakawa, "A hybrid integrated light source on a silicon platform using a trident spot-size converter," J. Lightwave Technol. **32**, 1329–1336 (2014).
22. S. Akiyama, M. Imai, T. Baba, T. Akagawa, N. Hirayama, Y. Noguchi, M. Seki, K. Koshino, M. Toyama, T. Horikawa, and T. Usuki, "Compact PIN-diode-based silicon modulator using side-wall-grating waveguide," IEEE J. Sel. Top. Quantum Electron. **19**, 74–84 (2013).
23. H. Okayama, D. Shimura, H. Takahashi, M. Seki, M. Toyama, T. Sano, K. Koshino, N. Yokoyama, M. Ohtsuka, A. Sugiyama, S. Ishitsuka, T. Tsuchizawa, H. Nishi, K. Yamada, H. Yaegashi, T. Horikawa, and H. Sasaki, "Si wire array waveguide grating with parallel star coupler configuration fabricated by ArF excimer immersion lithography," Electron. Lett. **49**, 410–412 (2013).
24. S. H. Jeong, D. Shimura, T. Simoyama, M. Seki, N. Yokoyama, M. Ohtsuka, K. Koshino, T. Horikawa, Y. Tanaka, and K. Morito, "Low-loss, flat-topped and spectrally uniform silicon-nanowire-based 5th-order CROW fabricated by ArF-immersion lithography process on a 300-mm SOI wafer," Opt. Express **21**, 30163–30174 (2013).