Integrated photonics in the 21st century

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We review the emergence and development of integrated photonics and its status today. The treatise is focused on information and communications technology (ICT) applications, but the technology is generically employable for a wealth of other applications, such as sensors. General properties of the waveguides that form the basis of integrated photonics are reviewed, and several examples of integrated photonics based on silicon and plasmonics are presented. The all-important development of integrated low-power nanophotonics is discussed and current challenges and prospects of the field are elucidated. The treatment is focused on the photonic fabric between source and detector. © 2014 Chinese Laser Press

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1. INTRODUCTION

Everybody is in some way or another acquainted with or affected by the enormous impact of integrated electronics and integrated circuits (ICs). They have shaped virtually all aspects of our social, professional, and cultural lives, and this development took its beginnings in the 1960s with the emergence of ICs, work for which the Nobel Prize was awarded in 2000. The material of choice was silicon, existing in abundance on Earth, and the development was hugely aided by the existence of a natural passivating oxide that protects the crystalline circuits.

At the same time in the '60s and maybe inspired by the unfolding of integrated electronics, another concept saw the light—that of integrated optics (today named integrated photonics, describing photonics integrated circuits, PICs), at Bell Labs. Though superficially related, they were in fact very different, an essential feature being that we are physically dealing with fermions in electronics and bosons in photonics. Also, for integrated photonics, one was over the years working with several constituent materials and device structures, in contrast to electronic IC circuits.

Integrated photonics has over the decades developed at a considerably slower pace than integrated electronics, in integration density as well in total number of devices on a chip. As a matter of fact, it was jokingly said "Integrated photonics is the technology of the future and will remain the technology of the future." However, this state of affairs has altogether been changed by progress in material technology in III–V compounds (GaAs, InP systems, etc.), ferroelectrics ($LiNbO_3$), silicon and silica, polymers, and metal optics and has, together with emerging nanotechnology, made integrated photonics solidly entrenched in a growing number of applications.

Photonics in general has over the past decades developed into a key enabling technology, with inroads in information and communications technology (ICT), with the optical fiber as one of the landmarks, awarded the Nobel Prize in 2009, in biotechnology, for a wealth of sensors and in lighting and energy. Most of these fields are more or less amenable to integrated photonics. In addition, we have areas such as medicine (for therapy and diagnosis), manufacturing (e.g., high-power fiber lasers), and security and surveillance, with maybe less use of integrated photonics. This shows the tremendous versatility and impact of photonics and makes photonics a counterpart to integrated electronics, with different but complementary functions.

But there are also basic physical differences between electronics in the shape of electronics ICs and ancillary devices and photonics. In the former case we are, as noted, generally dealing with fermions (electrons), which obey Fermi–Dirac statistics, whereas in the latter case we are employing bosons (photons), obeying Bose–Einstein statistics. This has significant consequences in the sense that it appears all but impossible to create photonics devices that perform digital signal processing and RAM-type memory functions, operations where electronics excel. On the other hand, photonics is the technology of choice for transmission and routing of vast amounts of high-speed data, useful in a wide variety of applications and spanning distances from global dimensions to (near) future photonic interconnect network fabric on multicore architecture chips and maybe eventually intracore. This is in view of the dominating power dissipation being that of interconnects.

Below we focus on the fabric between the sources (primarily lasers) and detectors.

This paper is organized as follows. After a brief treatment of Moore's law for integrated photonics, some general waveguide parameters and propagation properties are discussed. Silicon-on-insulator (SOI) and plasmonics-based integrated photonics are discussed, with several examples. The paper

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is concluded with views on challenges and prospects for integrated photonics in the 21st century.

2. MOORE'S LAW FOR PHOTONICS, FORMULATED IN TERMS OF INTEGRATION DENSITY

While the total number of devices in an integrated photonics chip is still of the order of hundreds depending on how one counts, that of the electronic IC is of the order of a billion transistors with an exponential growth in accordance with the famed Moore's law [1,2], a law that has turned out to be a formidable prediction of the future, or maybe formed the future, and a law that may have more economic than technological ramifications. In some contrast to the development of the number of devices on a photonics chip, the integration *density* has seen exponential growth of the same order as that of electronics [3]. We have thus formulated a photonics version of Moore's law (Fig. 1) based on integration density, which we define in terms of equivalent functions, since we do not have generic components, such as transistors and resistors, in photonics. As an example, we can take an 8×8 arrayed waveguide grating (AWG) [4,5], which in view of its functionality cannot reasonably be regarded as one single element. Difficulties of this nature do not appear in integrated electronics.

Some differences between the two types of integrated circuits might be worthwhile to point out:

(a) Moore's law for electronic ICs pertains to circuits with generic elements (transistors, resistors, capacitors), some fraction of which are operative in the sense that they dissipate power. These elements are fabricated by standard processes, applicable to all elements, basically in *one* material, silicon (though this is somewhat changing), with its natural passivating oxide.

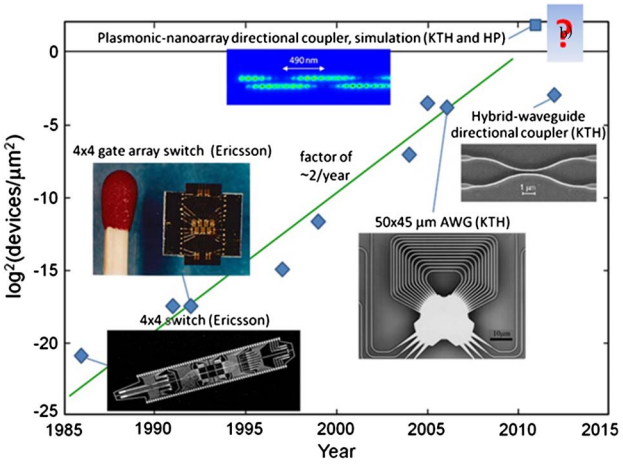

Fig. 1. Moore's law for integration density in terms of equivalent number of elements per square micrometer of integrated photonics devices, showing a growth faster than the IC Moorés law, adapted from [3]. The figure covers, in time order, a lithium niobate 4×4 polarization-independent switch array, a 4×4 InP-based integrated gated amplifier switch array, an SOI AWG, and a hybrid plasmonic (passive) directional coupler. All these are experimentally demonstrated. At the top is a simulation of two coupled metal nanoparticle arrays, forming a directional coupler, each array being a resonantly operated array of silver nanoparticles. If loss requirements of, e.g., 3 dB/cm were invoked, the latter two would occupy significantly lower places in the figure.

(b) A Moore's law for photonics will have to take into account the fact that no generic elements like those in electronics exist; on the contrary, the elements are different, employ differing fabrication processes, and the materials are different (III–V semiconductors, silicon, ferroelectrics, polymers, etc).
(c) There is no or small power dissipation in the passive fabric case [such as the arrayed waveguide gratings (AWGs), switch arrays in ferroelectrics, etc.] and there is "high" power dissipation for active devices (lasers, optical amplifiers. etc.) and intermediate in high-speed modulators.

The exponential development in integration density (Fig. 1) has been made possible by several factors: materials with higher refractive indices, such as going from quartz ($n = 1.5$) to silicon ($n = 3.5$), with III–V compounds of slightly lower index as an intermediate step. High index contrast in optical waveguides allows stronger light confinement and smaller bending radii and, in general, more efficient components [6]. Another issue is increased fabrication precision and improved modeling tools. The relevance of a Moore's law in photonics is discussed in the conclusions.

3. WAVEGUIDE PARAMETERS AND PROPAGATION CHARACTERISTICS OF DIFFERENT KINDS OF WAVEGUIDES

One can classify optical waveguides depending on geometry and light confinement, as well as on materials and guiding principles. Planar or slab dielectric waveguides are built of layers of high and low refractive index materials providing confinement only in vertical direction. Nonplanar waveguides that can have different cross sections, such as circular (fibers), ridge, rib, stripe-loaded, or buried; and slot structures can have different forms of guiding core surrounded by cladding material. Channel dielectric waveguides, similarly to optical fibers, utilize total internal reflection, guiding light in a higher refractive index core surrounded by lower index cladding material. There also exist other methods for guiding electromagnetic waves, such as photonic crystal waveguides, where light is confined by the periodicity of the structure in one or more directions, as well as surface plasmon polariton waveguides that use coupling of the electromagnetic field to the oscillation of electron plasma of a conductor (metal) in a dielectric–conductor interface, where electromagnetic surface waves are excited and propagate along the interface. These surface waves are evanescently confined in the perpendicular direction due to very shallow penetration of the electromagnetic field into the metal, opening possibilities for subwavelength light confinement.

A. SOI Integrated Photonics

Channel dielectric waveguides and waveguide devices based on a silica-on-silicon material structure became a widely used technology for telecom applications and showed the ability to keep high performance even for devices with high levels of integration. The main drawback of this technology is the overall large size of the components, mostly due to the large bending radii of waveguides. This limitation is dictated by a low refractive index difference between the core and the cladding of the device, giving scant light confinement, which generally gives a single multichannel AWG a size of several square centimeters, and the integration of more complex structures can be difficult on a single wafer.

Table 1. Waveguide Parameters for Different Materials

Column	1	2	3	4	5	6
Characteristics	SiO_2 Low Δ	SiO_2 Medium Δ	SiO_2 High Δ	$SiON_x$	III/V	SOI
Index difference Δ (%) $\Delta = \frac{n_{core}-n_{clad}}{n_{core}}$	0.3	0.45	0.75	3.3	7.0 (46)	41 (46)
Core size (μm)	8×8	7×7	6×6	3×2	2.5×0.5 (0.2×0.5)	0.2×0.5 0.3×0.3
Loss (dB/cm)	<0.01	0.02	0.04	0.1	2.5–3.5	1.8–2.0
Coupling loss (dB/point)	<0.1	0.1	0.4	3.7 (2)	5	6.8 (0.8)
Bending radius (mm)	25	15	5	0.8	0.25 (0.005)	0.002–0.005

Technologies based on high index contrast recently became the subject of active research. Much higher light confinement allows for very small core sizes and sharp bends, leading to the shrinkage of component sizes by several orders of magnitude.

Waveguide parameters and propagation characteristics for waveguides fabricated with different material compositions are presented in Table 1.

The first three columns collect characteristics for silica-on-silicon technology with germanium-doped silica core [7] with rising Ge concentration giving increasing core–cladding contrast from low, 0.3%, to high, 0.75%. Stronger light confinement can be realized using silicon oxynitride ($SiON_x$) core and silicon oxide cladding layers (column 4) [7] and even stronger using an InGaAs/InGaAsP material system, as well as other related compounds (column 5). Due to the fact that these compounds allow for fabrication of active devices, in principle, all optical building blocks for telecommunication applications can be integrated in III–V compounds. However, for very small structures, light leaks out of waveguide bends to the substrate because of the low index contrast between the materials. The numbers in brackets in column 5 are related to specially designed devices, where the buffer layer under the waveguide core was removed (membranes) or has been oxidized to lower its refractive index. In general III–V-based waveguides have higher losses, higher material cost, and their fabrication technology is more complex in comparison to the other technologies based on silicon wafers.

Silicon has recently attracted a great deal of attention as a material for highly integrated photonics. It has low losses for the optical communication window, high refractive index of 3.5 at telecommunication wavelengths, and offers an opportunity for low-cost optoelectronic solutions for applications ranging from long distance down to chip-to-chip interconnects. Additionally, silicon photonic devices can be fabricated using standard silicon processing technology. Compatibility with CMOS techniques allows cheap mass production of monolithically integrated optoelectronic structures. Strong light confinement in a silicon core on a silica buffer (SOI) allows for very sharp bends and submicrometer core sizes (see column 6 in Table 1 and Fig. 2), enabling design of submicroscale optical devices and very compact optoelectronic systems. In these submicrometer-sized structures, the fabrication accuracy has a very critical influence on the performance of the devices. The high index contrast makes the waveguide losses very sensitive to scattering at roughness on the core–cladding interface. The sidewall surfaces after etching the waveguide profile are particularly crucial for the final quality of the device. Both lithography and etching itself can have influence on the sidewall roughness, so both these steps should be optimized. The sidewall roughness can also be improved after etching by slight thermal oxidation of the etched silicon profiles.

B. Plasmonics and Hybrid Plasmonics: Selected Reported Results

Many large electronic companies started research and development programs devoted to silicon photonics, identified as a very promising solution for allowing movement of computer interconnects to the optical domain with considerably increased bandwidth and reduced energy consumption. The efforts that have been made still do not cover the mismatch of size between CMOS electronics with a feature size of 20 nm and very compact, but 1 order of magnitude larger, with diffraction limited modal field, silicon photonics. To further increase integration density and compactness of photonic structures for intercore and intracore applications, plasmonic waveguiding has been proposed as it allows breaking the diffraction limit of light. For example, in slot plasmonic waveguides, where a very thin (30–50 nm) dielectric film is situated between two metal layers, light is concentrated in the slot allowing for true nanoscale confinement. Many different geometries of plasmonic waveguide have been investigated in recent years, including strip lines, slot lines [8], v-groves [9], and periodic metal structures [10], but in all cases energy dissipation in closely spaced metal layers causes high losses, limiting the propagation length to a few micrometers for the highest confinement. Methods to decrease these losses have also been investigated. In general, extremely compact plasmonic structures with direct and efficient mode conversion

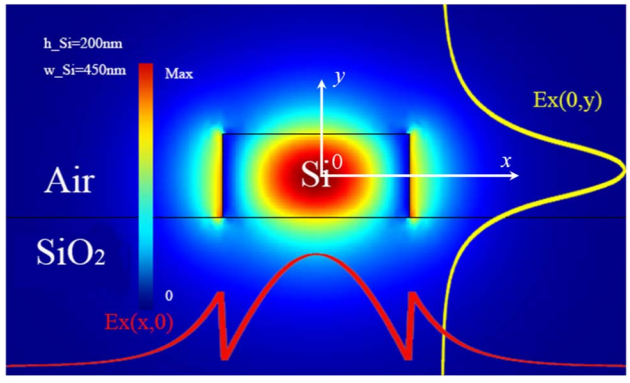

Fig. 2. Electric field distribution of TE mode in a silicon channel dielectric waveguide. The yellow and red curves express the amplitude distribution in the x and y directions, respectively; the substrate material is SiO_2, and the cladding is air. The guiding light core is made of silicon material with the geometry parameters height = 200 nm and width = 450 nm. The operating wavelength is 1550 nm. Channel dielectric waveguides, similarly to optical fibers, utilize total internal reflection, guiding light in higher refractive index core surrounded by lower index cladding material.

to photonic guiding allow for relatively low losses per device. Introducing nanoparticles or quantum dots into a low ε dielectric host to generate negative ε with low loss is another option, or, finally, using gain to compensate losses [11].

Hybrid plasmonic structures, which were proposed for the first time in 2007 [12] and elaborated theoretically in 2008 and 2009 [13,14] appear to be an interesting "compromise" solution. They allow for rather similar light confinement as in a metal–insulator–metal configuration, but with much lower losses and, hence, much longer propagation lengths.

A very thin low refractive index dielectric material, a slot layer (here SiO_2), is situated between a metal layer from one side and a high refractive index dielectric layer from the other side. In this structure light is confined partly in the thin low index material as a plasmonic mode at the boundary of the metal, and partly in the high index material as a highly confined photonic mode. Numerical investigations of the properties of such a hybrid mode show that, depending on the thickness of the slot and its width, one can obtain longer propagation lengths with lower confinement for thicker and wider slots or shorter propagation length (still longer than for a metal–insulator–metal plasmonic waveguide) with higher confinement. Propagation losses as low as 0.01 dB/μm (propagation length over 400 μm) have been experimentally obtained for the less confined mode when the silica layer thickness is 150 nm, and a propagation loss around 0.22 dB/μm (propagation length 19 μm) has been obtained for a highly confined mode with the size in the vertical direction of the order of 30 nm and in the lateral direction of the order of 200 nm. In both cases, subwavelength confinement has been achieved [15].

In our laboratory, a number of different passive components based on hybrid plasmonic waveguides have been simulated and fabricated, including waveguide couplers and splitters [16], disk resonators [17] (Fig. 3), and polarization beam splitters [18]. Using an electro-optic polymer (EOP) material instead of silica in the slot, one can theoretically realize active devices such as switches and modulators [19] (Fig. 4). This provides a way to realize subwavelength functional components for future ultracompact integrated structures for optical interconnects and other applications.

Comparing hybrid plasmonic structures with the similar silicon slot waveguides, where on both sides of a thin low refractive index material there are silicon layers [20], the

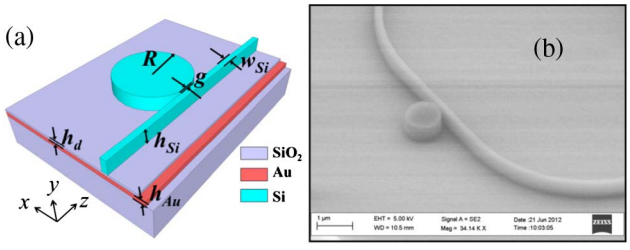

Fig. 3. Ultrasmall subwavelength hybrid plasmonic microdisk. (a) Schematic diagram and (b) SEM image of the fabricated device with radius around 525 nm. At this radius the cavity has a resonance at about 1550 nm and the intrinsic quality factor Q is about 200. The thicknesses of the Au, SiO_2, and Si layers are 100, 56, and 400 nm, respectively. The access waveguide width is 170 nm and the gap between the straight waveguide and the microdisk is 56 nm. The measured propagation losses of the access waveguide are 0.08 dB/μm.

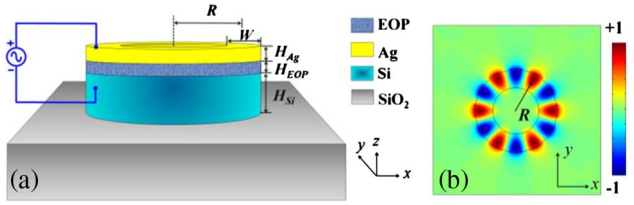

Fig. 4. (a) Schematic diagram of the hybrid plasmonic microring modulator. (b) Cross-sectional view along the x–y plane of the Ez field distributions of a resonant mode at 1550 nm with an azimuthal number of 6. The modulator consists of an EOP ring with radius R and a width W sandwiched between a silver ring and a silicon ring with the same radii and widths. A microwave field is applied between the Ag cap and the bottom Si layer, and the refractive index of the EOP can be changed using the ultrafast EO (Pockels) effect; correspondingly, the cavity can be switched between on- and off-resonance modes at a given frequency, resulting in the modulation of transmission power if an access waveguide is placed aside.

following conclusions can be drawn. The silicon slot waveguide structure allows for much lower propagation loss in comparison to plasmonic ones, but, on the other hand, only plasmonics can break the diffraction limit of light, allowing subwavelength light confinement. The reason is that even if the slot waveguide is comparable in thickness to a plasmonic one, only one-third of total optical power is located in the slot, whereas the rest is leaking out to Si slabs and cladding, considerably increasing the modal field size [21]. We have shown [19] that in extremely small components, for example submicrometer ring resonators, the quality factor Q of a hybrid plasmonic structure can be 8.5 times larger than the Q of a similar silicon slot resonator. When comparing figures of merit (FOMs) characterizing modulation efficiency of modulators based on these structures, the FOM of the hybrid plasmonic microring is 6 times better than that of the corresponding silicon slot structure, both using the same EOP as the active medium.

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4. CURRENT CHALLENGES FOR INTEGRATED PHOTONICS

As is obvious from the photonics Moore's law above, the smallest devices with reasonably low loss can be made in hybrid plasmonics, but even then, one cannot really use these for extended waveguides and large-scale concatenation of devices. The key problem is here the inherently high losses of available metals at room temperature, with electron scattering rates of the order of tens of femtoseconds. Even SOI waveguides have fairly large propagation losses in comparison to optical fibers or planar waveguide components based on well-established silica-on-silicon technology.

For ICT type applications, we could formulate requirements for PICs in photonics fabrics, e.g., as

- Longitudinal size < or ≪1000 nm;
- Transverse size < or ≪10^4 nm^2 (much below the diffraction limit);
- Energy dissipation <1 fJ/time slot;
- Insertion loss <1 dB;
- Bandwidth of transmission or switching control > or ≫10 GHz;
- Transmitted signal power: 100–1000 photons/time slot;
- (Polarization insensitivity);
- Low cost.

Table 2. Comparison of Performance of Some Electronically Controlled Modulators[a,b,c]

	Device and Wavelength λ_0 (A, amplitude; P, phase)	VπL [Vμm]	Vπ [V]	L [μm]	IL [dB] (Attenuation) [dB/μm)]	Confine-ment	Switch Energy [fJ/bit] (Capacitance) [fF]	Comments
1	P, Layered metal/ chalcogenide waveguide [22], $\lambda = 1.55$ μm	0.66	0.33	2	7 (3.5)	0.01 μm × 0.01 μm	0.003 (0.01)	Chalcogenide thickness 4 nm, index change 0.1
2	P, Array of Ag nanoparticles in EOP matrix, $\lambda = 0.680$ μm	3	15	0.2	2.4 (12)	~0.01 μm × 0.01 μm	(Very approxi-mate) 2 (0.01)	200 nm electrode separation. Very rough approximation, real values probably much better. Trading lower voltage for length impeded by loss
3	P, Slotline Si/EOP/Si, $\lambda = 1.55$ μm	160	2	80	0.1 (0.001)	~0.3 μm × 0.7 μm	33 (8)	Doped Si serves as electrodes. 100 nm EOP
4	A, Silicon microring resonant modulator, $\lambda = 1.55$ μm	41	1	41	~5	0.3 μm × 0.38 μm	~50	Depletion mode modulator *Experiment*
5	A, III–V Electroabsorption QCSE [23], $\lambda = 1.55$ μm	400	2	200 active 500 total	3–5	4 μm × 4 μm	300 (n/a)	Traveling-wave type EAM, 50 Ω transmission line *Experiment*

[a]Notes and assumptions: IL, insertion loss; EAM, electroabsorption modulator; QCSE, quantum confined Stark effect. EOP, electro-optic polymer: 500 pm/V or chalcogenide with index change = 0.1; VπL for π phase shift, or >10 dB extinction ratio for cases 4 and 5. Case 1–3, theory (Vπ and L as examples); cases 4 and 5, experiment.

[b]Only one resonant modulator is listed above, modulators with high Q values can of course give lower switch energy, but always at the expense of smaller bandwidth; see, e.g., [24].

[c]Adapted from [6].

Table 2 summarizes some theoretical and experimental results for select modulators, in terms of some of the most important characteristics.

It can be seen that no existing technology meets the requirements stated above, although the array of silver nanoparticles in an EOP matrix comes close. It is also seen that a (much) lower loss plasmonic medium would meet and surpass the requirements. Thus continued progress in the integration density in Fig. 1 is somewhat uncertain at this stage.

Another technology that holds promise and that is not being widely researched at the moment is that based on near field Förster resonant energy transfer (FRET)-coupled quantum dots (QDs) [25–27]. Electronically controlled switches based on such waveguides would actually rival CMOS in terms of footprint and switch energy (for 100 photons per time slot in the QD device), but not in speed for single arrays due to insufficient signal-to-noise ratio, even though the excitation transfer can be of the order of picoseconds.

Intel's state-of-the-art 22 nm feature size gives subpicosecond gate delay time and ~20 aJ dissipated switch energy.

Scant efforts have, surprisingly enough, been made to create lower loss negative-epsilon materials than those available, in spite of the huge possible rewards. In fact, the loss properties of a plasmonic material operating in a near-resonance configuration to achieve high field confinement (for low field confinement, one can always have arbitrary low optical losses) can be assessed by employing a quality factor Q [28]:

$$Q = \frac{\omega \cdot d\varepsilon'_{\text{metal}}/d\omega}{2\varepsilon''_{\text{metal}}}, \tag{2}$$

where ω is plasma frequency, and ε' and ε'' are real and imaginary parts of the metal dielectric constant, respectively. This factor is dependent only on the metal parameters since they determine those of the dielectric in order to have a resonant configuration. The value for silver at 1550 nm wavelength is order 50, short by say 2 orders of magnitude for many ICT applications.

This equation, rather than the somewhat arbitrary quotient between real and imaginary parts of metal epsilon should be used to assess the loss properties of plasmonic media when operating at or close to resonance conditions.

5. CONCLUSIONS AND PROSPECTS

So what can we expect of integrated photonics in the 21st century? The development up to now has certainly been impressive, as shown in Fig. 1, and as is well known, nothing is as difficult to predict as the future. However, it is reasonably certain that material technology research has an important role, such as to come up with better plasmonics materials. A rather new vista for integrated photonics is, as noted above, the use of QDs for waveguides and switches, where some issues are size dispersion and positioning accuracy of QDs. Here DNA technology offers very interesting possibilities and creates a bridge to the biology world.

This focus on material technology does not mean that we will not see new and unique device structures with existing materials, which was what happened, e.g., with AWGs. Another issue that has been very much debated is the relative merits of all-optical integrated photonics switches versus electronically controlled ones. This is treated in some detail in a recent paper [29], and one of the conclusions is that, as long as the control information resides in the electronic domain with

concomitant limited bandwidths, it is difficult to compete with electronically controlled switching systems. Another issue here is the generally weaker interaction light–light versus RF-electronics–light, resulting in generally higher switching energy for the all-optical switch.

An interesting issue concerns the relevance of the Moore's law of Fig. 1. In contrast to the original law, which is about total number of elements, Fig. 1 concerns integration density, implicitly assuming the smallness of photonics devices being used for complex circuitry. However, this is not likely to occur on the scale of electronics, simply since there is no apparent need for such a development at the present time, although not implying that there never will be. An entity missing in Fig. 1 is the impact of insertion and propagation losses, a feature not relevant to electronics due to power regeneration at each active element (transistor). One possibility to include these losses in Fig. 1 is to make the integration density dependent on these insertion and propagation losses. Applying such a scheme, the devices in the right uppermost part of Fig. 1 would exhibit much lower integration density.

Figure 1 should rather be seen as a gauge of development toward nanosized photonics, with consequences for device footprint, power dissipation (being generally coupled to the size of the devices), and cost (also to some extent coupled to the size).

The table of requirements for PICs in photonics fabrics summarizes issues from Fig. 1 and adds data on bandwidth and number of photons per time slot, again clearly aimed at ICT applications. Maybe the major future development in integrated photonics will be in the sensor and bio fields, whence it follows that requirements are somewhat different in comparison to ICT, which has in some way been the implicit focus above and still is in many research laboratories all over the world. However, as noted, the real challenge resides in low-cost, real nanosized, low-power dissipation integratable photonics circuits for ubiquitous applications, and quantum leaps might be needed to pursue the exponential unfolding of Fig. 1.

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