Design and optimization of BCCD in CMOS technology*

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This paper optimizes the buried channel charge-coupled device (BCCD) structure fabricated by complementary metal oxide semiconductor (CMOS) technology. The optimized BCCD has advantages of low noise, high integration and high image quality. The charge transfer process shows that interface traps, weak fringing fields and potential well between adjacent gates all cause the decrease of charge transfer efficiency (*CTE*). *CTE* and well capacity are simulated with different operating voltages and gap sizes. *CTE* can achieve 99.999% and the well capacity reaches up to 25 000 electrons for the gap size of 130 nm and the maximum operating voltage of 3 V.

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Nowadays, there are two main types of image sensors which are charge-coupled device (CCD) and complementary metal oxide semiconductor (CMOS)[1]. CCDs have attractive features of high sensitivity, low noise and high image quality, but they need high power consumption, high cost and complex process due to overlapping gates. On the other hand, CMOS image sensors with standard CMOS processes have advantages of high speed, low power consumption and low cost. However, CMOS image sensors have lower dynamic range and lower image quality compared with CCD. Fabricating CCD in CMOS technology is useful based on the advantages of low noise, high speed and high image quality. Adjacent non-overlapping single gates are separated by a narrow gap, and the maximum operating voltage is 3.3 V in CCD structure implemented in CMOS technology[2,3]. With device feature size shrinking, the gap size is narrowed continually and the performance of CCD fabricated in CMOS technology is comparable with conventional CMOS pixels[4,5]. The buried channel charge-coupled device (BCCD) structure implemented in CMOS technology was reported in Refs.[6]—[8], and the surface channel charge-coupled device (SCCD) in CMOS technology was reported in Refs.[9] and [10]. The BCCD structure has high charge transfer efficiency (*CTE*) of 99.9% and well capacity of 3 550 electrons[6,7]. *CTE* reached 99.99% with 3.3 V operation voltage, and well capacity achieved a few $Ke^-/\mu m^2$ in Ref.[8]. The effects of fixed charge were alleviated by using a large negative voltage, and charge transfer inefficiency (*CTI*) ranged from 5.7×10^{-4} to 7×10^{-3} in Ref.[9]. *CTI* was reduced by passivating the channel stop with p-well implanting in Ref.[10]. The CCD structure achieves high *CTE* and low noise charge accumulation so that it can be applied to X-ray imagers, time delay integration (TDI) image sensors, low-light-level image sensors and so on[6-10].

The paper presents a BCCD structure in CMOS technology. Effects of gap size, the number of stored charge and the operating voltage on CTE are analyzed. The simulation results demonstrate that smaller size of gap and larger potential difference between adjacent gates can help charge transfer completely. In our design, device structure size, doping concentration and operating condition are optimized for getting the higher *CTE* and the larger well capacity.

Fig.1 shows the three dimension (3D) structure of BCCD array. It can be seen from Fig.1 that the array consists of single polysilicon gates, channels and channel stops[11]. We replace overlapping gates with single polysilicon gates separated by narrow gaps, and use p-type channel stops to isolate n-type buried channels. The p-type substrate has the thickness of 3 μm and the concentration of 1×10^{15} cm^{-3}. The n-type buried channel is formed by implanting phosphorus, and it has a peak concentration at 60 nm under the surface. Gate oxide is formed by depositing 8-nm-thick SiO_2. The thickness and width of p^+ doped polysilicon gates are 150 nm and 1 μm, respectively. The width of gap between adjacent gates is 130 nm. We design BCCD structure with the help of technology computer aided design (TCAD). Fig.2 shows the cross sectional view of doping concentration diagram from the simulation structure of BCCD.

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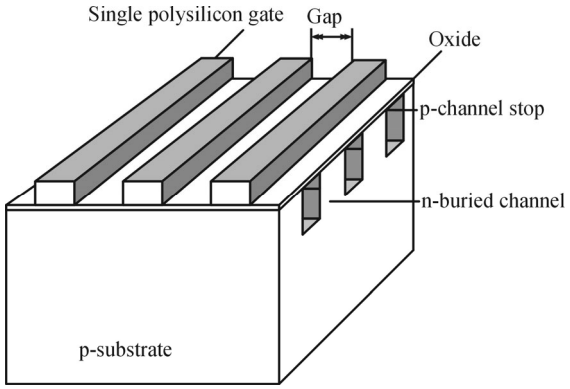


Fig.1 Schematic diagram of 3D structure of BCCD array

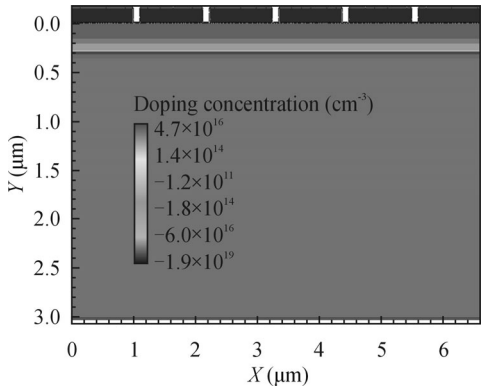


Fig.2 Cross sectional view of doping concentration diagram from the simulation structure of BCCD

Fig.3 shows the electrostatic potential profile in the bulk. The maximum potential well appears in the bulk, and charges are stored under the surface. The electrostatic potential is determined by gate voltage and the number of charge stored in the potential well. The electrostatic potential increases with raising the gate voltage and decreases with growing the number of charge stored in the potential well.

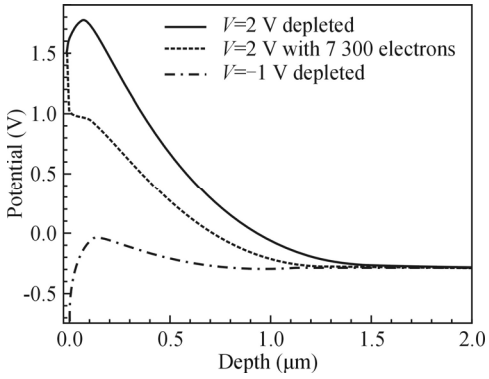
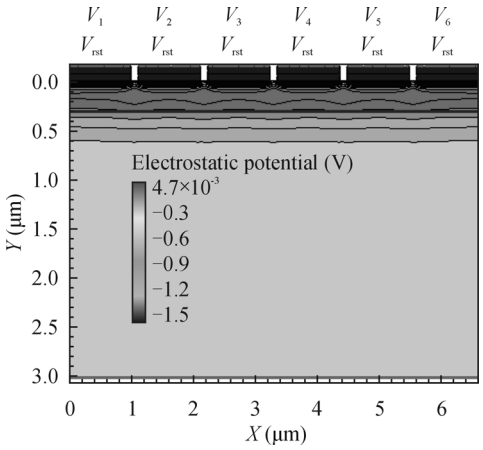
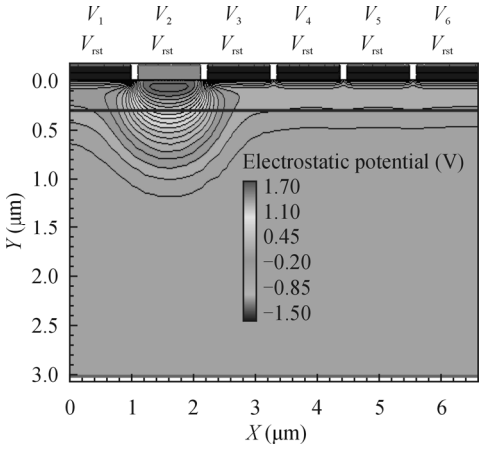


Fig.3 Electrostatic potential profile below one gate with gate voltage of −1 V, 2 V depleted or 2 V with 7 300 electrons stored in potential well

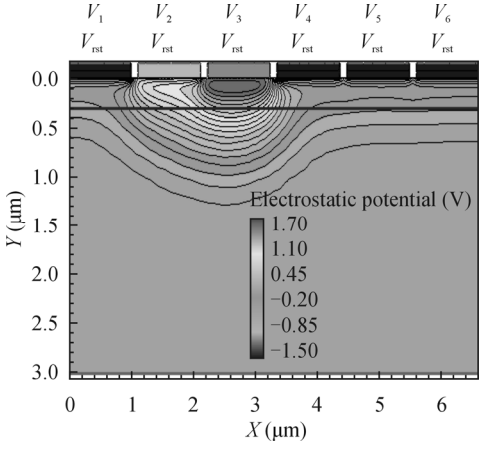
In the initial state of working process, all electrodes are set to be V_{rst}. The buried channel is depleted completely, and the electrostatic potential distribution diagram is shown in Fig.4(a). And then V_{max} is applied to V_2, which creates a potential well. Photogenerated charges are stored in the potential well as shown in Fig.4(b). Next, V_2 is set to be $V_{max}/2$, and V_3 is set to be V_{max}. Potential difference is formed between V_2 and V_3, which drives the charges from V_2 to V_3 as shown in Fig.4(c). Finally, V_2 is driven back to V_{rst}, and V_3 remains V_{max} as shown in Fig.4(d). The charges are transferred from V_2 to V_3 fully. All of the charge transfers are completed according to the above sequence.



(a)



(b)



(c)

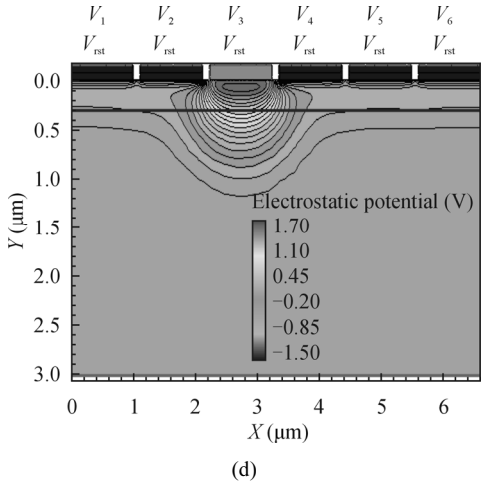


Fig.4 Electrostatic potential distribution diagrams during charge transfer: (a) All electrodes are set to be V_{rst} and the buried channel is depleted completely; (b) Charges are stored in potential well created by V_2; (c) Charges under V_2 are transferred to V_3; (d) Charges are transferred from V_2 to V_3 fully

Charges are stored in the potential well in form of charge packet. Charge packets are transferred by three mechanisms which are thermal diffusion, self-induced drift and fringing field drift. Self-induced drift field is caused by charge gradient distribution. Charges in the same type repel each other and then redistributes. When the number of stored charge is small, transfer process is determined by thermal diffusion. The driving force provided by thermal diffusion is small which can lead to less *CTE*. Fringing field produced by the gate voltage is impacted by impurity doping concentration, the gap size and the different voltage between adjacent gates. Increasing gap size between adjacent gates is capable of weakening fringing field and enlarging potential pocket to stop charge transfer. Decreasing operating voltage also reduce fringing field and charge handling capability. Therefore, increasing operating voltage and shrinking gap size both have an effect on improving charge handling capability and *CTE*. In addition, the presence of interface traps is also the main factor of charge transfer failure. We use BCCD structure to transfer charge under surface which can avoid interface traps effectively.

CTE is the most important performance factor for evaluating the characterization of CCD. *CTE* between adjacent gates can be expressed as

$$CTE = \left(\frac{Q_N}{Q_0}\right)^{\frac{1}{n}}, \tag{1}$$

where n is the transfer times, Q_0 is the number of stored charge, and Q_N is the number of transferred charge. In addition, charge handling capability is also an important factor in CCD structure which is decided by maximum well capacity. The higher gate voltage creates deeper potential well where more charges can be stored.

We evaluate *CTE* and charge handling capability with different gap sizes, different operating voltages and different numbers of stored electrons. Fig.5 shows the estimated *CTE* as a function of the number of stored electrons for gap sizes of 130 nm, 180 nm and 250 nm. It is obtained with V_{max}=3 V and V_{rst}=−1 V. From Fig.5 we can see that *CTE* is higher with smaller gap size. *CTE* reaches 99.999% when the gap size is 130 nm. With the increase of the number of stored electrons, *CTE* has an increasing trend for less than 10 000 stored electrons, and has a downward trend for more than 10 000 stored electrons. Weak self-induced drift field and potential pocket between adjacent gates are the main factors affecting *CTE* for less number of stored charges. With increasing the number of stored charge, the charge packet is closer to the Si/SiO_2 interface and is easier to be captured by interface traps. The presence of interface traps is the main factor affecting *CTE* for a large number of stored charges. Fig.6 shows simulated well capacity versus different maximum operating voltages. The well capacity is enhanced with higher maximum operating voltage. It reaches 25 000 electrons when maximum operating voltage V_{max} is 3 V and the width of gate is 0.5 μm. Fig.7 describes the estimated *CTE* as a function of the number of stored electrons with gap size of 130 nm for maximum operating voltage varying between 1.5 V and 3 V. Different operating voltages corresponds to different well capacities. The higher the maximum operating voltage, the greater the *CTE*.

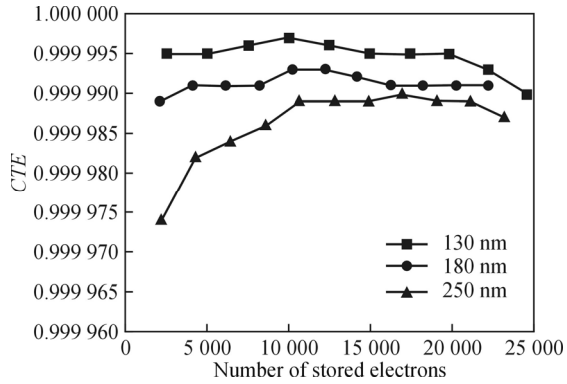


Fig.5 *CTE* as a function of the number of stored electrons for different gap sizes

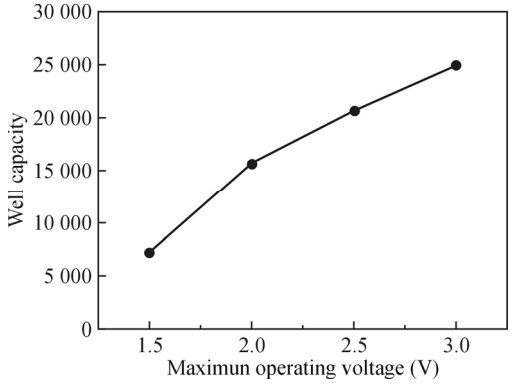


Fig.6 Well capacity as a function of different operating voltages

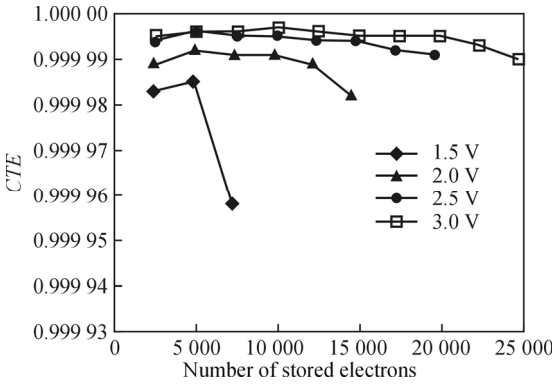


Fig.7 *CTE* as a function of stored electrons for different operating voltages

Detailed design and operation about the structure of BCCD fabricated by CMOS technology are presented. The analysis of charge transfer describes that weak fringing fields, potential pocket between adjacent gates and interface traps all lead to charge transfer failure. The simulation results demonstrate that *CTE* can be enhanced by narrowing the gap size and increasing the maximum operating voltage. The BCCD structure has *CTE* of 99.999% and well capacity of 25 000 electrons for gap size of 130 nm and maximum operating voltage of 3 V.

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