A high performance all-optical set-reset flip-flop based on SOA-MZI

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A set-reset all-optical flip-flop (SR-AOFF) based on semiconductor optical amplifier Mach-Zehnder interferometer (SOA-MZI) is proposed. Simulation results show that low switching energy in the femto joule range, the transition time of less than 20 ps, high stability and high extinction ratio (ER) of 30 dB can be achieved, while AOFF output is power insensitive approximately.

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An all-optical flip-flop (AOFF) is a key building block in the next generation photonic transmission and computation systems. AOFF also has the potential to be used as a fundamental module for more advanced functionalities, like optical random access memory (RAM) cells[1,2], clock generation[3] and optical packet switching[4,5]. Since AOFFs are sequential circuits, their outputs depend on not only the information at the inputs but also the information in the previous state. The output of AOFF must have two states at least. These states can be distinguished by different output power in conventional reset-set flip-flop or different output wavelengths in optical memories[6]. Several researches have been carried out to implement AOFF[7-10]. The ring laser can be extended to other AOFF schemes, where the coupled nonlinear optical elements are semiconductor optical amplifier (SOA) Mach-Zehnder interferometers (MZIs)[11]. Other AOFF implementations incorporate the adjustment of the lasing threshold in a distributed feedback (DFB) laser[12] or the polarization bistability in a cylindrical-shaped single-mode vertical-cavity surface emitting laser (VCSEL)[13]. Among the interferometric structures, SOA-MZI which uses cross-phase modulation (XPM) effect is the most promising candidate due to its attractive features of low energy requirement, simplicity, stability and compactness[14]. Clavero et al[15] presented a set-reset AOFF (SR-AOFF) based on SOA-MZI and passive feedback loop, which has an extinction ratio (ER) more than 20 dB and transition time less than 100 ps, while the required energy for set and reset pulses is less than 2 pJ. The basic structure of this configuration with some changes was used to make a T-flip-flop[16] and a D-flip-flop[17]. The frequency domain transfer function of this structure was analyzed in Ref.[18]. It is very power sensitive, so the precise power adjustments for set and reset pulses are necessary by proper operation.

In this paper, an SR-AOFF based on SOA-MZI is reported with operation bit rates at 10 Gbit/s and 40 Gbit/s, rejected forbidden state (set=1, reset=1), transition time less than 20 ps, ER about 30 dB and very low power sensitivity. Also the output of AOFF is stable against the changes of the SOAs' parameters.

The schematic diagram of the proposed architecture for SR-AOFF is shown in Fig.1.

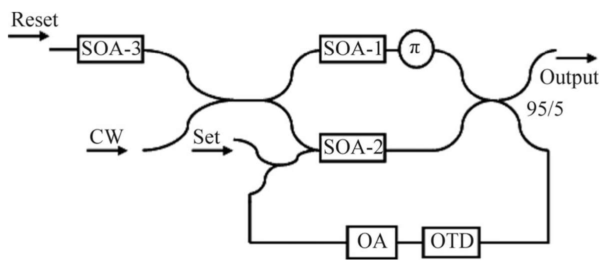

Fig.1 Schematic diagram of the architecture for SR-AOFF

A continues wave (CW) optical signal with wavelength of λ_{cw} is launched into the input port of SOA-MZI via input coupler. The set signal at wavelength of λ_{set} is launched into the lower arm of the MZI. Because of the existing phase shift of π between the interferometer branches, in absence of the set signal, the destructive interference takes place, so no CW signal is obtained at the interferometer output. When a set pulse is injected into the lower arm of the MZI, it enters SOA-2, and

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reduces its carrier density, refractive index and differential gain. But the operation condition of SOA-1 remains unchanged at the same time. Consequently, the phase difference between the two splitting parts of CW signal respectively passing through SOA-1 and SOA-2 changes according to[19]

$$\Delta\phi = -\frac{\alpha}{2}\ln\left(\frac{G_1}{G_2}\right), \tag{1}$$

where α is the line-width enhancement factor, and G_1 and G_2 are the gains of SOA-1 and SOA-2, respectively. By properly selecting the set signal power, the injected set pulse introduces π phase shift to the part of the CW signal which passes through SOA-2. So the constructive interference occurs, the CW signal is obtained at the output port of the interferometer, and the state of AOFF changes to "1". Feedback loop holds the state of AOFF by returning a fraction of the amplified set signal through the output 95/5 coupler, an optical time delay (OTD) and an optical attenuator (OA), for adjusting the feedback signal. In this structure, OTD is adjusted to 7 ps, which corresponds to the waveguide length of about 1.5 mm. OA is used to reduce the feedback power level for desired operation. Reset pulses pass through SOA-3 and are amplified before being injected into the interferometer. So they prevent SOA-1 and SOA-2 from amplification by the CW and set signals by cross-gain modulation (XGM) effect. Therefore, the state of AOFF goes to zero. In this situation, the feedback signal is omitted too. So the state of AOFF remains zero, even if the reset signal is removed. When the set and reset pulses are injected simultaneously into the structure, the reset pulse gets higher priority by setting SOA-1 and SOA-2 into high saturation region and preventing them from amplification. Therefore, in this situation, the state of AOFF is forced to zero. The truth table of this SR-AOFF is shown in Tab.1.

Tab.1 The truth table of SR-AOFF

Set	Reset	Output
0	0	Hold state
0	1	0
1	0	1
1	1	0

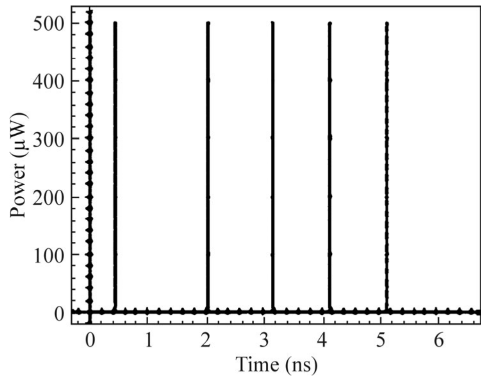
Three SOAs used in this structure have the same parameters as given in Tab.2. Two important parameters of the SOAs can be extracted from this table, which are the unsaturated single-pass amplifier gain G_0≈28 dB and the saturation energy of the SOA E_{sat}≈600 fJ.

The CW signal is from a 0.2 mW laser source with λ_{cw} of 1 550 nm. Feedback loop returns only a portion of set signal. For resetting the AOFF by omitting feedback signal, set and reset signals must have different wavelengths. Their wavelengths are λ_{set}=1 540 nm and λ_{reset}=1 530 nm. The minimum required energy for the reset pulses is 2 fJ, and that of the set pulses depends on the operation bit rate and varies from 1.6 fJ in 10 Gbit/s to 4 fJ in 40 Gbit/s. The attenuation factor of optical attenuator is equal to 9 dB. The optical time delay is 7 ps.

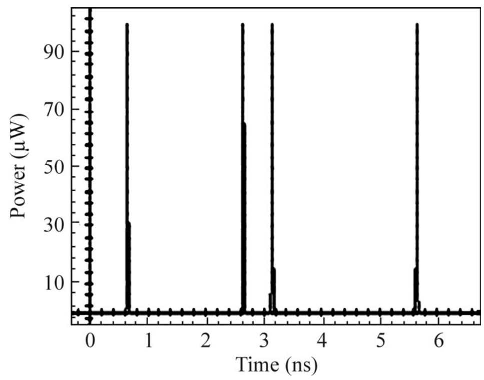
Tab.2 Parameters of SOAs

Parameter	Symbol	Value
Injection current	I	SOA-1 and SOA-2: 150 mA SOA-3: 200 mA
Confinement factor	Γ	0.3
Differential gain	a_N	2.78×10^{-20} m^2
Line-width enhancement factor	α	5
Carrier density at transparency	N_{tr}	1.4×10^{24} m^{-3}
Initial carrier density	N	3×10^{24} m^{-3}
Width of active region	w	3 μm
Depth of active region	d	0.08 μm
Length of active region	L	500 μm

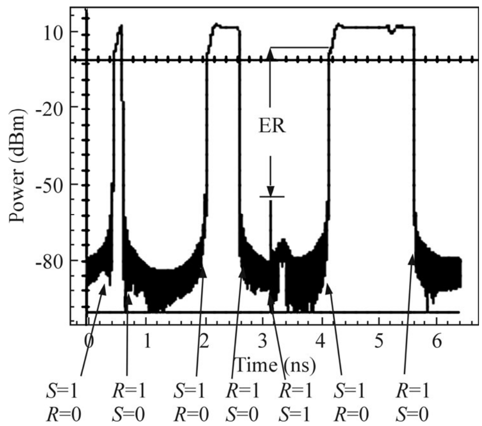
We simulate the proposed architecture for SR-AOFF by using OptiSystem software at 10 Gbit/s and 40 Gbit/s, and the simulation results are shown in Figs.2 and 3, respectively. The set and reset bit sequences are marked in Fig.2(c), where S and R represent the states of set and reset signals, respectively.



(a) Set pulses

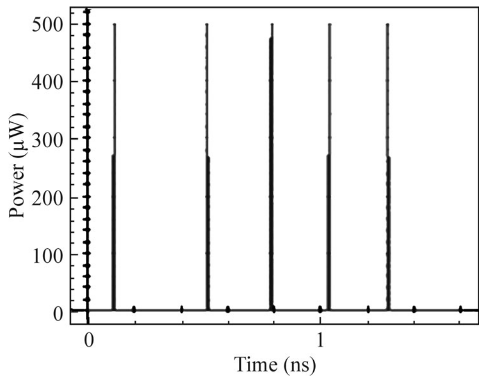


(b) Reset pulses

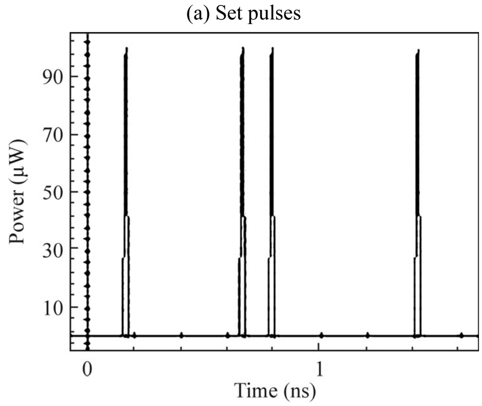


(c) AOFF output

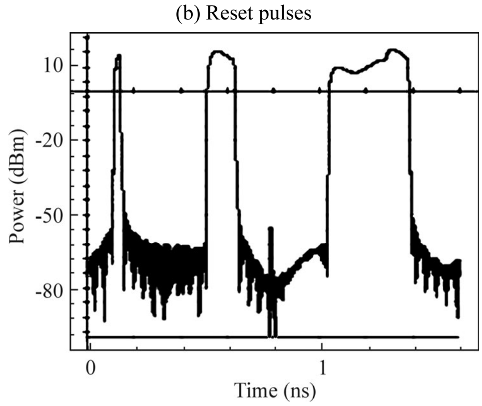
Fig.2 Simulation results of SR-AOFF operating at 10 Gbit/s



(a) Set pulses



(b) Reset pulses



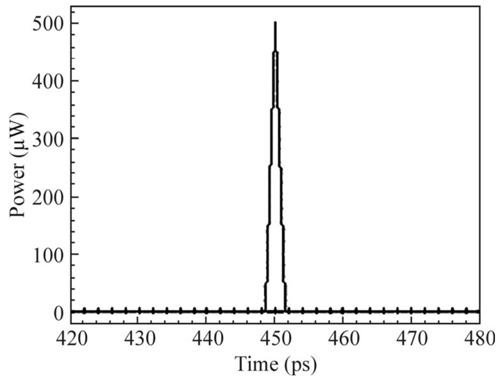
(c) AOFF output

Fig.3 Simulation results of SR-AOFF operating at 40 Gbit/s

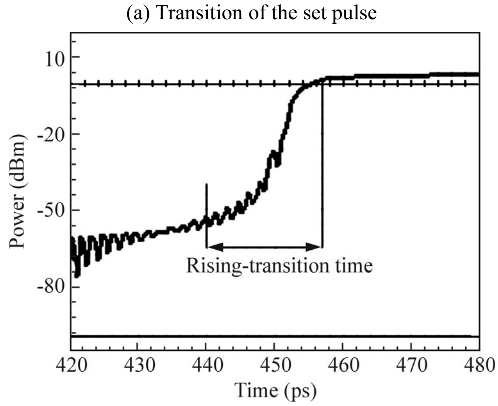
As shown in Figs.2 and 3, when the set signal goes to the state "1", while the reset signal goes to the state "0", the output becomes "1" and holds at this state until the reset signal goes to "1". When the reset signal goes to "1", output becomes "0" and latches this state until the set signal goes to "1" again. When both the set and reset signals go to the state "1" simultaneously, the output is forced to be "0".

ER is indicated in Fig.2(c), which is defined as the ratio of the minimum required energy (power) used to transmit a bit "1" to the maximum required energy (power) used to transmit a bit "0".

In order to calculate the rising and falling transition time of AOFF output, the transitions of the set and reset pulses and the rising and falling transitions of AOFF output are shown in Figs.4 and 5. As shown in Figs.4 and 5, the falling and rising transition time is less than 20 ps.

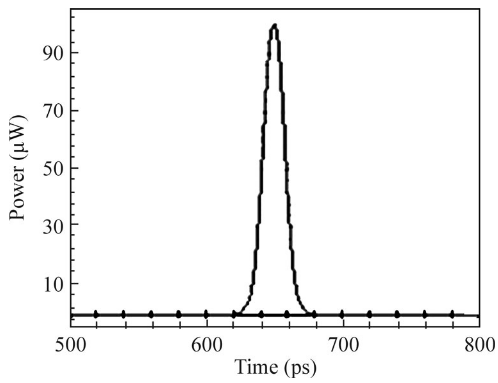


(a) Transition of the set pulse

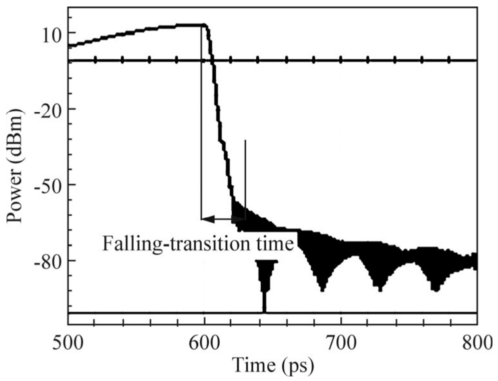


(b) Rising transition of AOFF output

Fig.4 Calculation of the rising transition time of AOFF output at 10 Gbit/s



(a) Transition of the reset pulse



(b) Falling transition of AOFF output

Fig.5 Calculation of the falling transition time of AOFF output at 10 Gbit/s

In this paper, we propose an SR-AOFF based on SOA-MZI, and simulate the operation of this AOFF at bit rates of 10 Gbit/s and 40 Gbit/s. The calculated ER is about 30 dB, while the minimum required set and reset pulse energies are in the femto joule range, and the AOFF output transition time is less than 20 ps. Simulation results show that the characteristics of the proposed AOFF are better than those presented in Ref.[15]. Also, our AOFF has the advantage that it is stable against the change of the SOAs' parameters and nearly insensitive to the energy of the set and reset pulses

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