Design and implementation of the optical fiber control and transmission module in multi-channel broadband digital receiver

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An optical fiber control and transmission module is designed and realized based on Virtex-7 field programmable gata array (FPGA), which can be applied in multi-channel broadband digital receivers. The module consists of sampling data transfer submodule and multi-channel synchronous sampling control submodule. The sampling data transmission in 4× fiber link channel is realized with the self-defined transfer protocol. The measured maximum data rate is 4.97 Gbyte/s. By connecting coherent clocks to the transmitter and receiver endpoints and using the self-defined transfer protocol, multi-channel sampling control signals transferred in optical fibers can be received synchronously by each analog-to-digital converter (ADC) with high accuracy and strong anti-interference ability. The module designed in this paper has certain reference value in increasing the transmission bandwidth and the synchronous sampling accuracy of multi-channel broadband digital receivers.

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In terms of high-speed sampling data transmission, analog-to-digital converter (ADC) data is usually forwarded by field programmable gate array (FPGA) in high-speed serial bus (HSSB)[1]. Normally, HSSB for electrical signal transmission uses a differential pair to avoid noise jamming, but it may cause signal attenuation, crosstalk or other problems[2,3] with the increase of transfer distance and data rate. Currently, optical fiber is usually used to transfer ADC sampling data[4-6], which can frequently adjust the layout of FPGA and optical modules to shorten the distance of electrical signal transmission, reduce the design difficulty and improve the signal quality. However, limited by the performance of the selected serial transceiver of FPGAs, their optical fiber line rate is less than 6.25 Gbit/s. Besides, the bandwidth utilization ratio is not high enough in physical layer 8B/10B encoding. In terms of the realization of the multi-channel synchronous sampling control, some papers[7,8] only use electric signals to transfer synchronous sampling control command, which can cause signal attenuation or distortion and have an adverse effect on the timing accuracy of sampling control and the stability of the whole system.

To solve these problems, we design an optical fiber control and transmission module applied in multi-channel broadband digital receivers for realizing high-speed sampling data transmission and multi-channel synchronous sampling control. In this module, Virtex-7 FPGA introduced by Xilinx is used, and the optical fiber line rate can reach 10.31 Gbit/s, improving the bandwidth of sampling data transmission significantly. Physical layer 64B/66B encoding is used, which has higher bandwidth utilization ratio than traditional 8B/10B encoding. What's more, adopting coherent clock and self-designed protocol, the module can realize the optical fiber transmission of synchronous sampling control signals, whose anti-interference ability and control precision are improved.

The structure of the optical fiber control and transmission module designed in this paper is shown in Fig.1.

The optical fiber control and transmission module consists of sampling data transfer submodule and multi-channel synchronous sampling control submodule. Sampling data is transferred from each analog-to-digital (AD) sampling board to the data reception and synchronous control board by 4× optical fiber channel which constitutes the sampling data transfer submodule together with the related logic in FPGA. Synchronous sampling control signal is transferred in the inverse direction by 1× optical fiber channel which constitutes multi-channel synchronous sampling control submodule together with the related logic in FPGA. Virtex-7 xc7vx690t FPGA is selected in this design. It can provide 36 GTH transceivers, whose total I/O bandwidth is 943.2 Gbit/s, in accordance with the requirement of multi-

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channel high-speed sampling data transmission. AFBR-703SDZ is selected as optical transceiver module, whose fiber link rate can reach the magnitude order of 10 Gbit/s. In specific engineering implementation, the number of lanes in the optical fiber link channel and the number of AD sampling boards can be adjusted according to actual requirement.

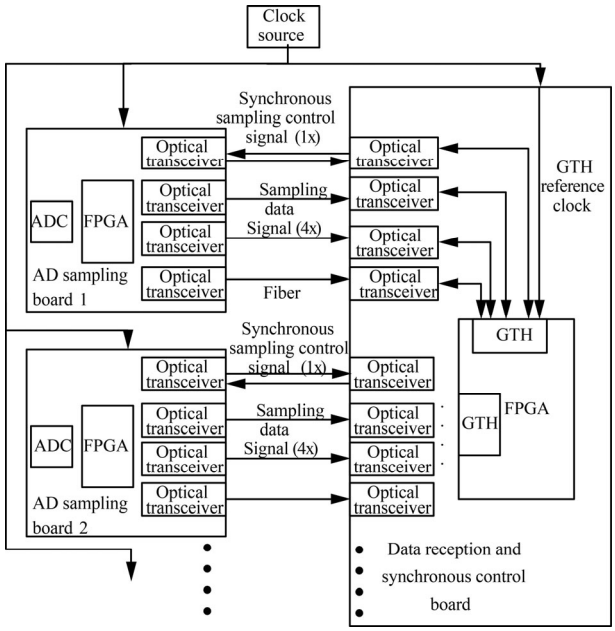


Fig.1 The structure of the optical fiber control and transmission module

To ensure the correctness of data transmission, firstly, the optical fiber link should be adjusted to a stable state. However, as the line rate increases, the instabilities in the fiber link are apt to occur[9], which are shown as follows. Firstly, because the stability of optical fiber link is sensitive to the optical transceiver modules, for different models with parameters meeting the requirements, the link quality may change. Secondly, the quality of the optical fiber link is sensitive to the optical fiber. Thirdly, the error rate is high.

The proper FPGA GTH parameters can improve the quality of optical fiber link effectively. The factors affecting the stability of optical fiber link and the related GTH parameter configuration are as follows. First is the quality of clocks driving GTH modules. In this test, we choose quad-based LC tank phase locked loop (QPLL) instead of ring-based channel phase locked loop (CPLL) for optimal jitter performance. Second is the quality of electrical signals from FPGA to optical transceiver modules. We need to adjust the transmitter (TX) differential output voltage swing to the specified range of selected optical transceiver modules and control the TX pre-emphasis by adjusting TX pre-cursor and TX post-cursor[10]. In this test, we set TX differential output voltage swing as 400 mV, TX pre-cursor as 0.45 dB and TX post-cursor as 0 dB. Third is the effective reception of electrical signals from optical transceiver modules. Good reception performance can be acquired by adjusting the termination voltage and the GTH receiver (RX) equalizer mode. GTH RX equalizer can work in power-efficient and adaptive linear equalizer mode, called the low-power mode (LPM), for long-distance optical fiber transmission or high-performance and adaptive decision feedback equalization (DFE) mode for short-distance optical fiber transmission. For continuous incoming data, the auto-adaptation of equalizer parameters in both LPM and DFE modes can improve the reception performance. Auto-adaptation of DFE mode is used in this test, and the termination voltage is set to MGTAVTT.

This design uses integrated bit error ratio tester (IBERT) IP core to adjust GTH parameters dynamically and to display the link state and error rate in real time. As the IBERT interface shown in Fig.2, by GTH parameter configuration according to the setup mentioned above, all of the optical fiber links are established with line rate of 10.31 Gbit/s, and the error rate is less than 2.6×10^{-14} with 0 data error after transmission for about 1 h. To further test the quality of the optical fiber link, the eye patterns of electrical signals to or from the optical transceiver modules are obtained by the SDA 816Z2-A oscilloscope, which are shown in Fig.3. As shown in Fig.3, the opening states of the eye patterns are both good, and the signal distortion after electro-optic and optoelectronic conversion is small. Jitters in Fig.3(a) and (b) are 5.3 ps and 8.5 ps, respectively, which are in the acceptable range. The test results show that the fiber link after GTH parameter adjustment is reliable and stable.

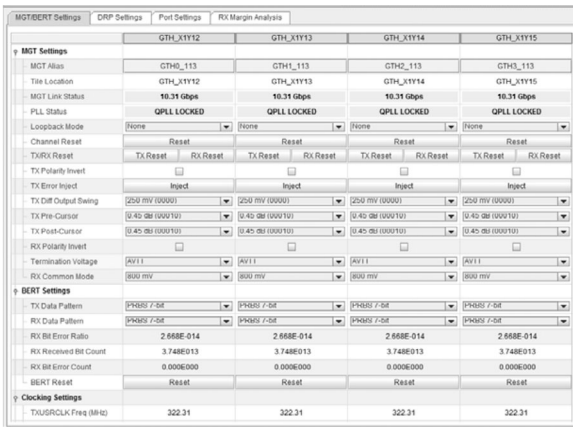
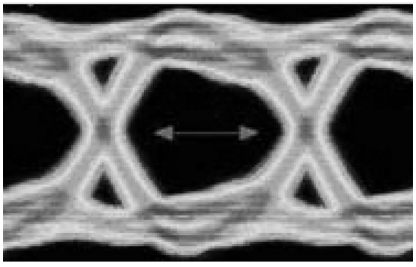
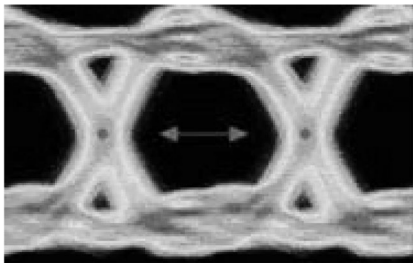


Fig.2 IBERT test results after GTH parameter adjustment



(a)

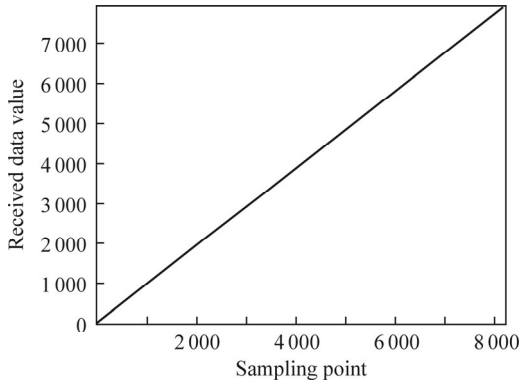


(b)

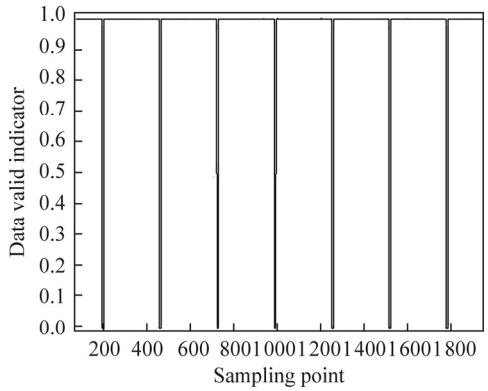
Fig.3 Eye patterns of eletrical signals (a) to and (b) from the optical transceiver module

After getting the proper configuration of related GTH parameters, a self-defined protocol is used to transmit sampling data. The protocol uses 64B/66B encoding in physical layer, and realizes channel bonding of 4 fiber link lanes. To verify the correctness of data transmission and measure the maximum data rate, a data source which sends a series of increasing natural numbers is added to the TX endpoint FPGA. When the data is transferred in 4× fiber link channel with the self-defined protocol at maximum speed, we use ChipScope software to capture the related signals in RX endpoint FPGA and export them, which is shown as Fig.4. In Fig.4(a), the received data is also a series of increasing natural numbers, indicating the data transmission is correct. In Fig.4(b), the valid indicator of received data shows that the high level duty ratio is about 96.5%, so the actual maximum data transfer rate in the submodule is 10.31 Gbit/s×4×96.5%=39.80 Gbit/s, which can meet the data transfer rate requirement of high-performance ADC.

In the design and implementation of multi-channel data receiver, accurate synchronous sampling control is necessary. If multi-channel synchronous sampling is not accurate enough, the start time of sampling will shift in different channels, which will cause the change of phase relationship among those channels and badly affect the quality of subsequent sampling data processing. If sampling control signals are transferred in electric wires or cables, attenuation and distortion reaching AD sampling boards asynchronously and affected by electromagnetic interference may take place, especially for numerous sampling channels or long cables.



(a) Received data



(b) Valid indicator of received data

Fig.4 Related data exported from the RX endpoint FPGA of sampling data transfer submodule

For these problems, this submodule allocates 1× fiber link channel for each AD sampling board to transfer synchronous sampling control signal. On one hand, it can overcome the distortion, attenuation and electromagnetic interference in signal transmission and improve the timing precision. On the other hand, it reduces the difficulty of project implementation, because we can use the fiber link of sampling data transfer submodule in the inverse direction for control signal transmission (as shown in Fig.1) and needn't add extra cables or ports.

Using optical fibers to transfer synchronous sampling control signals, we must ensure that the control signals are received by the FPGA of each AD sampling board synchronously. If non-coherent clocks are connected to TX and RX endpoints, clock compensation sequences are usually inserted in data transmission to overcome the overrun of receiver due to the differences in clock frequency and jitter, which can cause the asynchronism in data reception[11].

Here we use the test circuit in Fig.5 to verify the asynchronism in optical fiber data transmission with non-coherent clocks. The data source in TX endpoint (FPGA1) sends a series of increasing natural numbers. Aurora 64B/66B is used as the data transmission protocol. When data begins to transfer, we use ChipScope to capture the related signals in RX endpoint (FPGA2) and export them, which are shown as Fig.6. From Fig.6, we can find that the received data and the data valid indicators from two channels are not coincident, so there is time delay between data reception in different channels. So synchronous optical fiber signal transmission can't be realized when non-coherent clocks are connected to TX and RX endpoints.

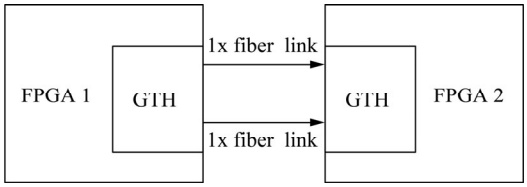
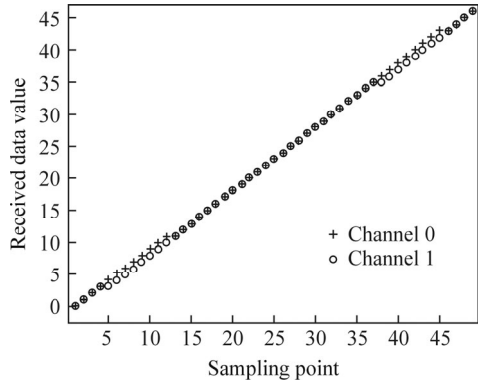
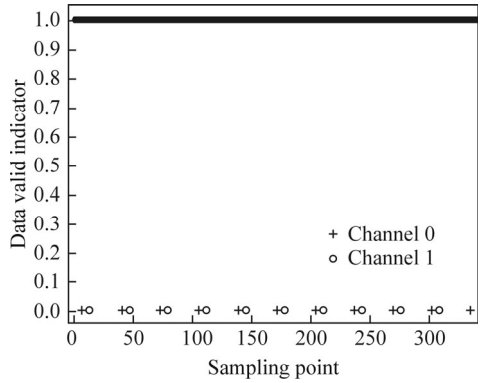


Fig.5 The synchronism test circuit for multi-channel optical fiber transmission



(a) Received data from different channels



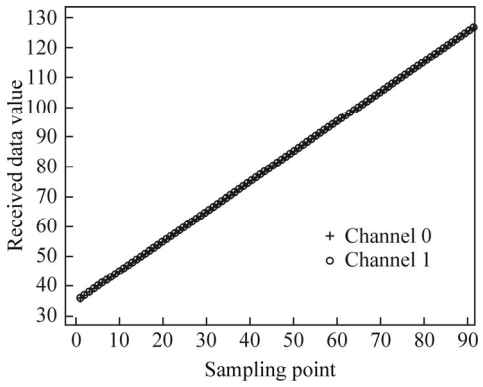
(b) Valid indicators of received data from different channels

Fig.6 Related data exported by ChipScope from the RX endpoint FPGA with non-coherent clocks

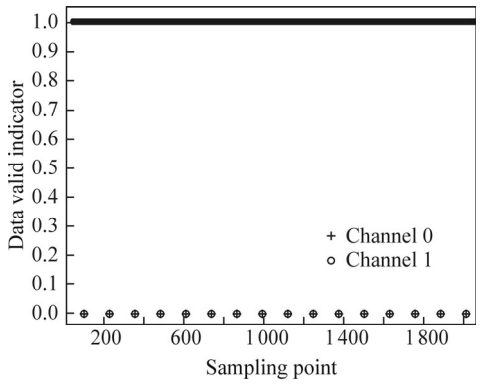
To overcome the asynchronism of multi-channel optical fiber transmission, the coherent clocks are connected to TX endpoint FPGA and RX endpoint FPGA, and the self-defined protocol is used without clock compensation sequences in data transmission. Using the same test circuit in Fig.5 with coherent clocks, the related signals in RX FPGA captured and exported by ChipScope are shown in Fig.7. From Fig.7, we can find that the received data and the data valid indicators from two channels are completely coincident. By comparing Figs.6 and 7, we conclude that synchronous data reception in different fiber channels can be realized with coherent clocks connected to TX and RX FPGAs.

After ensuring synchronous data transmission in different fiber channels, we encode the synchronous sampling control instruction as 0xAABBCCDD and send it to the FPGA in each AD sampling board. Then the FPGA decodes the sampling control instruction, outputs synchronous reset signal to each ADC, and enables the sampling data reception of first input and first output (FIFO) in FPGA. The waveforms of synchronous reset signals received by different ADCs are shown in Fig.8.

In Fig.8, synchronous reset signals received by different ADCs are aligned with each other on the whole, so the output clocks of different channels can be aligned, and the phase congruency of multi-channel sampling data can be ensured. The submodule realizes the synchronous control of multi-channel ADC sampling successfully.



(a) Received data from different channels



(b) Valid indicators of received data from different channels

Fig.7 Related data exported by ChipScope from the RX endpoint FPGA with coherent clocks

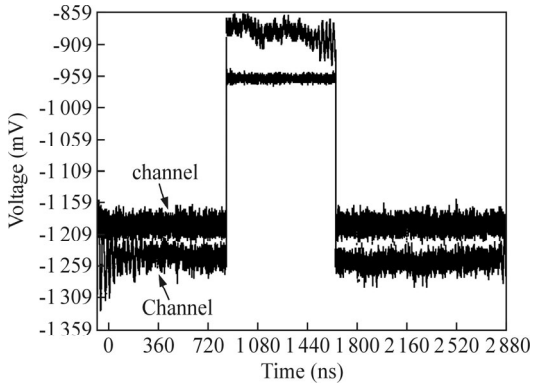


Fig.8 Waveforms of synchronous reset signals received by different ADCs

In this paper, the optical fiber control and transmission module is designed and realized based on Virtex-7 FPGA, which is applied in multi-channel broadband digital receiver. The module achieves high-speed sampling data transmission and multi-channel synchronous sampling control. The measured sampling data transfer rate can reach 39.80 Gbit/s with optical fiber line rate of 10.31 Gbit/s. Using optical fibers to transfer sampling data and synchronous sampling control signals, the module has prominent advantages, such as high bandwidth, strong anti-interference ability and high control precision.

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