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Fabrication of large-area nano-scale patterned sapphire substrate with laser interference lithography*

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Periodic triangle truncated pyramid arrays are successfully fabricated on the sapphire substrate by a low-cost and high-efficiency laser interference lithography (LIL) system. Through the combination of dry etching and wet etching techniques, the nano-scale patterned sapphire substrate (NPSS) with uniform size is prepared. The period of the patterns is 460 nm as designed to match the wavelength of blue light emitting diode (LED). By improving the stability of the LIL system and optimizing the process parameters, well-defined triangle truncated pyramid arrays can be achieved on the sapphire substrate with diameter of 50.8 mm. The deviation of the bottom width of the triangle truncated pyramid arrays is 6.8%, which is close to the industrial production level of 3%.

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Gallium-nitride (GaN) based light emitting diodes (LEDs) have been widely used[1]. Many techniques have been introduced for improving internal quantum efficiency and light extraction efficiency of the GaN-based LEDs, such as epitaxial lateral overgrowth (ELOG)[2], surface roughening[3,4], metal mirror reflect layer[5] and patterned sapphire substrate (PSS). Among them, the PSS technique has attracted much more attention, because it can improve both crystalline quality[6,7] and light extraction efficiency of LEDs[8,9].

Compared with micro-scale patterned sapphire substrate (MPSS), nano-scale patterned sapphire substrate (NPSS) has better performance in improving the light extraction efficiency of LEDs[10-12], because NPSS has higher pattern structure density than MPSS, and those pattern structures can increase the probability of light scattering. Therefore, NPSS has become a new focus of the PSS research. Large-area, low-cost and high-efficiency nanolithography technology is the key in the production of NPSS.

The traditional nanolithography technologies, such as electron beam lithography (EBL)[13], focused-ion beam lithography (FIBL)[14] and nanoimprint (NI)[15,16], are not scalable in the manufacturing industry due to the high cost and low throughput. Therefore, the laser interference lithography (LIL) has been adopted to prepare nano-patterns over a large area in recent years[17-19]. LIL is very flexible to change the period and line width of the nano-patterns. Furthermore, it meets the large area, high efficiency and economy requirements of the industrial NPSS production.

In this paper, uniform triangle truncated pyramid arrays with period of 460 nm are successfully fabricated on the sapphire substrate with diameter of 50.8 mm by LIL using a 325 nm He-Cd continuous wave laser as a light source. And dry etching and wet etching techniques are ingeniously combined to ensure patterns are transferred precisely without damaging or contaminating the sapphire substrate. The process parameters, pattern morphology and feature sizes are also systematically investigated. The deviation is 6.8% for the bottom width of the triangle truncated pyramid arrays on the sapphire substrate with diameter of 50.8 mm.

The fabrication process for triangle truncated pyramid arrays is illustrated in Fig.1. First, a 50 nm SiO_2 layer was deposited on a sapphire substrate by plasma-enhanced chemical vapour deposition (PECVD). Then the diluted resist of all resist 3840 (1:5.5) was spin-coated at 4000 r/min for 30 s to form a photoresist (PR) layer with thickness of about 100 nm. Before exposure, the samples were pre-baked at 90 °C for 2 min. The sample was subsequently exposed twice in Lloyd-mirror LIL system with a 325 nm light source at incident angle of 19.8°, as shown in Fig.2. The sample was rotated 90° between the two exposures. Each exposure was 5 mJ/cm^2. After exposure, photoresist development was carried out in a 2.5% tetra methyl ammonium hydroxide (TMAH) solution for 20 s, followed by rinsing in isopropyl alcohol (IPA) and deionized water, respectively. Then dot array patterns with period of 460 nm were fabricated on the

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photoresist. A descum process using O_2 plasma was then performed to ensure that no resist residue was left in the exposed region. The dot array was transferred from photoresist onto the SiO_2 layer by reactive-ion etching (RIE), using gas combination of CHF_3 and Ar. The substrate was etched with mixture solution of H_3PO_4 and H_2SO_4 (3:1) at 190 °C for 60 min, and the etching rate was 3 nm/min. Finally, the residual SiO_2 was removed by diluted hydrofluoric acid solution, and the NPSS with patterns of triangle truncated pyramid arrays was obtained after being rinsed with deionized water and dried with nitrogen.

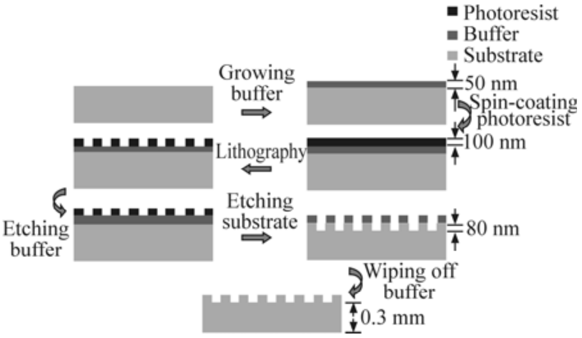


Fig.1 Schematic diagram of the experimental process

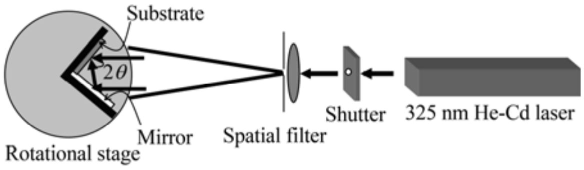
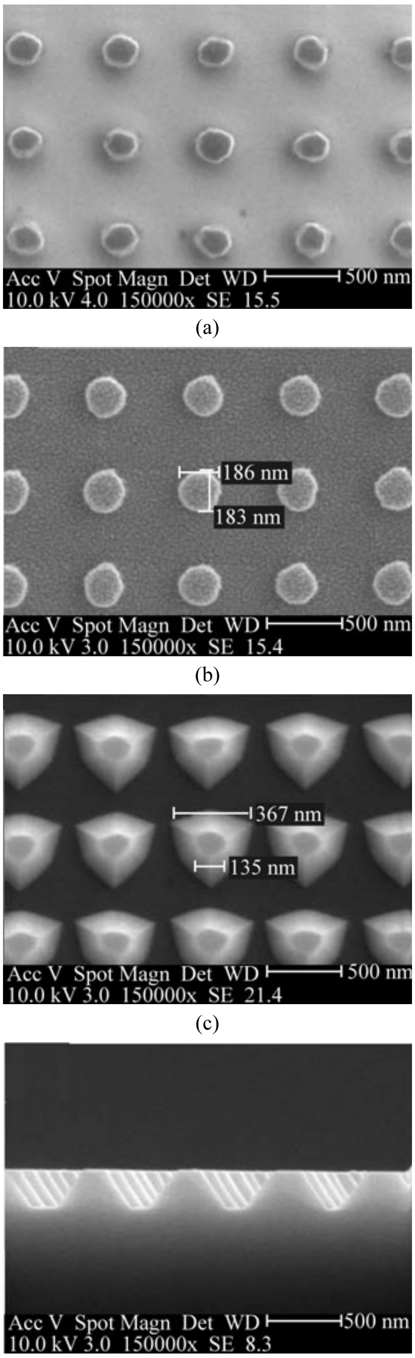


Fig.2 Lloyd-mirror LIL system

The morphology and feature sizes of the patterns are investigated by using scanning electron microscope (SEM). Fig.3 shows the SEM images of patterns in different process steps prepared by LIL. The dot array with period of 460 nm was fabricated on the photoresist as shown in Fig.3(a). The diameters of the dots in array are approximately 180–200 nm. The dot array was transferred from photoresist onto the SiO_2 layer by RIE as shown in Fig.3(b). The morphology and feature sizes of the SiO_2 dot array shown in Fig.3(b) are nearly the same as the photoresist dot array shown in Fig.3(a). Fig.3(c) and (d) show planar and cross-sectional SEM images of the triangle truncated pyramid arrays after wet etching, respectively. The NPSS has uniform sizes and smooth facets, and the period is 460 nm as designed. The heights of triangle truncated pyramid patterns are about 200 nm, and the up mesa width is about 135 nm, while the down mesa width is about 370 nm.



(a)

(b)

(c)

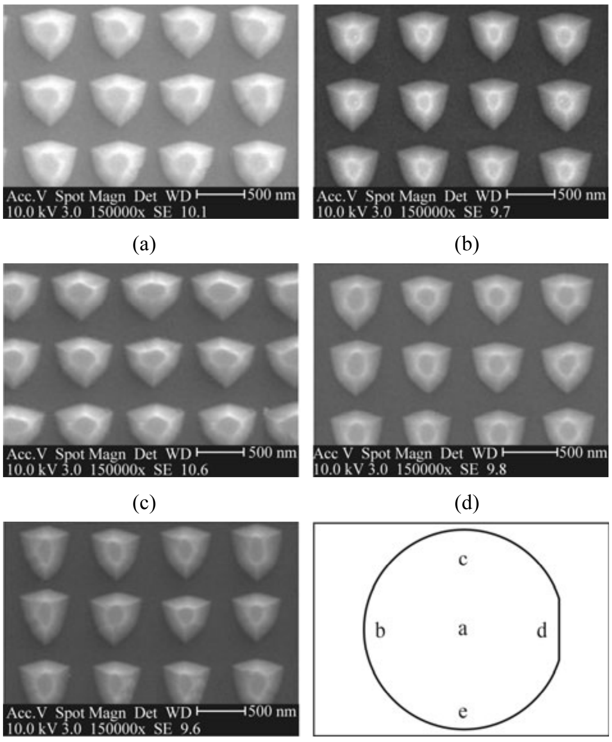
(d)

Fig.3 SEM images of (a) photoresist dot array and (b) SiO_2 dot array; (c) Planar SEM and (d) cross-sectional images of triangle truncated pyramid array

PSSs are commonly fabricated by dry etching techniques, such as RIE and inductively coupled plasma (ICP) in industrial production. These techniques can transfer the nano-patterns from photoresist onto sapphire substrate precisely. However, the surface of sapphire substrate can be easily contaminated and damaged during the dry etching process, which can prejudice the growth of high-quality GaN epilayer. Jing Wang et al[20] firstly adopted the wet etching technique to fabricate MPSS in 2006. The wet etching technique has the advantages of high etching efficiency along special crystal orientation, convenient process, cost-effective equipment and high productivity. Especially, the surface contamination and damage can be avoided during the wet etching process. So we combine dry etching and wet etching techniques to fabricate the NPSS, so the advantages of dry etching and wet etching are both retained. The dry etching process ensures that the dot array remains intact when it is transferred from photoresist to the SiO_2 mask. The wet etching process guarantees the triangle truncated pyramid arrays have clean and smooth facets, without damaging the substrate. As a result, the triangle truncated pyramid arrays NPSSs with uniform size are prepared.

In order to further promote the size uniformity of the triangle truncated pyramid arrays over large area, the stability of the LIL system is improved. For reducing the vibration disturbance to the LIL system, a series of measurements are adopted in this paper. By improving the stability of the LIL system and properly selecting the process parameters, well-defined triangle truncated pyramid arrays are achieved on the sapphire substrate with diameter of 50.8 mm.

Fig.4 shows SEM images of the triangle truncated pyramid array NPSSs prepared by LIL. Fig.4(a) shows the SEM image of the center of sapphire substrate with diameter of 50.8 mm denoted as a region in Fig.4(f), whose bottom width of the triangle truncated pyramid is about 365 nm. Fig.4(b)–(e) show the SEM images of the triangle truncated pyramid arrays in 5 different regions of the sapphire substrate denoted as regions b–e in Fig.4(f), respectively. Regions b–e are all 2 mm away from the edge of the sapphire substrate with diameter of 50.8 mm, and the bottom widths of the triangle truncated pyramid are about 335 nm, 367 nm, 333 nm and 320 nm, respectively.



(a) (b)

(c) (d)

(e) (f)

Fig.4 SEM images of 5 different regions of the triangle truncated pyramid array NPSSs

Fig.5 shows the bottom widths of the triangle truncated pyramid in 5 different regions of the sapphire substrate with diameter of 50.8 mm. The deviation is 6.8% for the bottom widths of the triangle truncated pyramid arrays on the sapphire substrate, which is calculated by

$$\delta = \frac{x_{\max} - x_{\min}}{2\bar{x}} , \tag{1}$$

where

$$\bar{x} = \frac{\sum_{1}^{n} x_i}{n} . \tag{2}$$

The deviation is close to the industrial production level of 3%. It means that the feature sizes of triangle truncated pyramid arrays on the sapphire substrate with diameter of 50.8 mm are highly uniform, which is important for the application in the NPSS industrial production. Future works for further improving the size uniformity of the NPSS will be continued. The safety of the wet etching process will also be considered for practical industrial production.

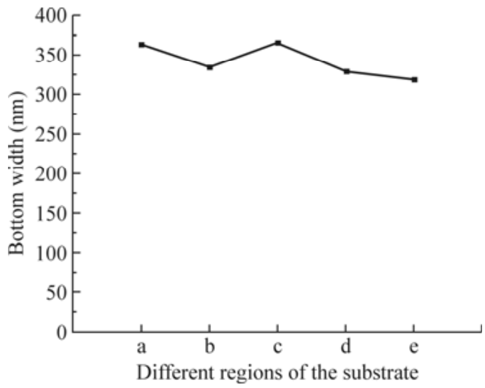


Fig.5 The bottom widths of the triangle truncated pyramid arrays in 5 different regions of the sapphire substrate with diameter of 50.8 mm

In summary, NPSSs with uniform patterns of triangle truncated pyramid arrays are successfully fabricated by low-cost and high-efficiency LIL system. During the process, dry etching and wet etching technologies are adopted in sequence. The period of the patterns is designed at 460 nm to match the wavelength of blue light LED. The process parameters, pattern morphology and feature sizes are systematically investigated. By improving the stability of the LIL system and optimizing the process parameters, well-defined patterns of triangle truncated pyramid arrays are achieved on the sapphire substrate with diameter of 50.8 mm. The deviation is 6.8% for the bottom widths of the triangle truncated pyramid arrays on the sapphire substrate with diameter of 50.8 mm. The patterns prepared by LIL have uniform sizes, which is important for the application in the NPSS industrial production.

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