NAND gate with quantum dot-semiconductor optical amplifiers-based Mach-Zehnder interferometer

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The NAND operation at 250 Gbit/s based on quantum dot-semiconductor optical amplifiers (QD-SOAs) is modeled. By solving the rate equations of SOAs in the form of a Mach-Zehnder interferometer (MZI), the performance of NAND gate is numerically investigated. The model takes the effects of amplified spontaneous emission (ASE) and the input pulse energy on the system's quality factor into account. Results show that NAND gate in QD-SOA-MZI based structure is feasible at 250 Gbit/s with a proper quality factor. The decrease in quality factor is predicted for high spontaneous emission factor (N_{SP}). For an ideal amplifier (N_{SP} = 2), the Q-factor is 17.8 for 30 dB gain.

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The all-optical logic technology is important for a wide range of applications in all optical networks, including high speed all-optical packet routing and optical encryption, etc[1]. An important unit in the technology is the optical logic element. In recent years, the high speed all-optical logic XOR gates using different schemes were reported, including the use of semiconductor laser amplifier loop mirror (SLALOM)[2], ultrafast nonlinear interferometer (UNI)[3] and the semiconductor optical amplifier (SOA) based Mach-Zehnder interferometer (MZI)[4,5]. Among these approaches, SOA is believed to be a key component for all-optical logic gates, because it has a stronger nonlinearity than optical fibers and is easier for integration. The speed of conventional bulk SOA operation is limited by the temporal response of gain and phase recovery. The typical value for phase-recovery time is several hundreds of pico-seconds, which limits the optical logic speed to lower than 100 Gbit/s[6].

NAND gate is very important because other Boolean logic elements and circuits can be realized by using NAND gates as basic building blocks. The demonstration of quantum-dot (QD) SOA provides an opportunity for ultra-high speed all optical switching. For a QD-SOA, the gain recovery response is significantly faster (i.e., 300 fs–10 ps)[7] than that for bulk SOA, which can lead to considerably improved high-speed performance for QD-SOA based logic systems. All-optical logic performance and high speed of QD-SOA based devices are studied[8,9]. Effect of amplified spontaneous emission (ASE) on bulk SOA based all-optical logic gate is studied[10,11]. All-optical logic NAND based on two-photon absorption (TPA) in bulk SOAs is presented[12]. The ultrafast all-optical XNOR gate using a single QD-SOA-based MZI is presented[13]. Tbit/s optical logic gate based on QD-SOAs is theoretically analyzed[14]. In this work, the high-speed performance of QD-SOA-based NAND gate is simulated. All simulations are performed at a repetition rate of ~ 250 Gbit/s. Effects of ASE and the input pulse energy on the system's quality factor (Q-factor) are studied. On undertaking the nonlinear effects, the results exhibit that the gates can have high Q-factor at high speed operation. The Q-factor obtained in this work is higher compared with that under the same operation conditions as reported in Refs.[8, 9]. The used device is an MZI each arm of which has a QD-SOA. The primary noise in this calculation in the absence of the ASE noise is pattern effect resulting from long recovery time of gain and gain-induced phase change. The ASE causes additional output noise through spontaneous-spontaneous beat noise and signal-spontaneous beat noise. In addition, the dark current of the photodiode, shot noise and thermal noise have to be considered when the SOA is used as a pre-amplifier[1]. The ASE related noise depends on the spontaneous emission factor (N_{SP}) of the amplifier.

The operation of a QD-SOA can be studied using a rate-equation model. In this model, a wetting layer and an active QD region are included. The optical gain and carrier transfer between the wetting layers, the QD excited state (ES) and the QD ground state (GS) are schematically shown in Fig.1. The carriers are injected into the wetting layers from which it makes a fast transfer to the QDs. The dots are assumed to be uniform and identical. The device gain is determined by the carrier density

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of the QD ground state. As the wetting layer serves as the only recipient of the pump current, while QD excited state serves as a carrier reservoir for the ground state with ultra fast carrier relaxation to the latter, their carrier densities and transition rates can affect the device gain. The rate equation for carriers in wetting layer and a single QD is described in Ref.[8].

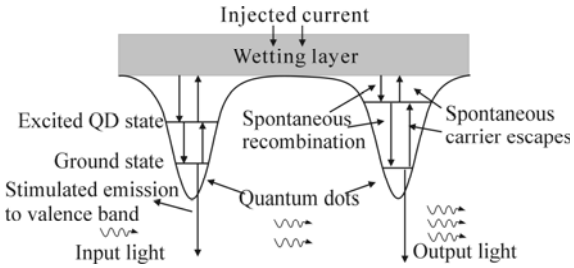


Fig.1 Schematic diagram of QD states and carrier transition of QD-SOA

The device used is the commonly discussed InAs/GaAs QD-SOA with InAs QDs embedded in GaAs layer. The active layer of the device consists of alternately stacked InAs island layers and GaAs intermediate layers. In this work, the two-level QD model to simulate the carrier transitions in the device is used. The schematic diagram of QD-SOA-MZI for NAND output is shown in Fig.2.

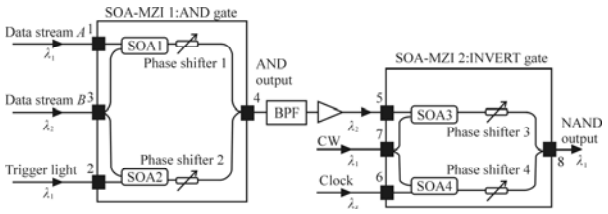


Fig.2 Schematic diagram of an NAND logic gate using two MZIs in series combination

The operation of QD-SOA-MZI can be studied using a rate equation model. The carrier heating results from a thermalization of carriers in the entire energy band following the pulse. This is a fast process occurring in time scale of 0.1 ps to 0.7 ps. The injected pulse reduces the gain at the photon energy of this pulse, i.e., in the gain spectrum it burns a hole. This process is known as spectral hole burning. By taking both carrier heating and spectral hole-burning effects into consideration, the time-dependent gain for each QD-SOA is given by[8]:

$$\frac{\mathrm{d}h_\mathrm{d}}{\mathrm{d}t}=\frac{h_\mathrm{w}}{\tau_{\mathrm{d}\to\mathrm{w}}}\left(1-\frac{h_\mathrm{d}}{h_0}\right)-\frac{h_\mathrm{d}}{\tau_\mathrm{dr}}-\left[\exp(h_\mathrm{d}+h_\mathrm{CH}+h_\mathrm{SHB})-1\right]S(t,0)\,, \tag{1}$$

$$\frac{\mathrm{d}h_\mathrm{w}}{\mathrm{d}t}=\frac{h_\mathrm{in}}{\tau_\mathrm{wr}}\left(1-\frac{h_\mathrm{w}}{h_0}\right)-\frac{h_\mathrm{w}}{\tau_\mathrm{wr}}-\frac{h_\mathrm{w}}{\tau_{\mathrm{w}\to\mathrm{d}}}\left(1-\frac{h_\mathrm{d}}{h_0}\right), \tag{2}$$

$$\frac{\mathrm{d}h_\mathrm{CH}}{\mathrm{d}t}=-\frac{h_\mathrm{CH}}{\tau_\mathrm{CH}}-\frac{\varepsilon_\mathrm{CH}}{\tau_\mathrm{CH}}\times\left[\exp(h_\mathrm{d}+h_\mathrm{SHB}+h_\mathrm{CH})-1\right]S(t,0)\,, \tag{3}$$

$$\frac{\mathrm{d}h_\mathrm{SHB}}{\mathrm{d}t}=-\frac{h_\mathrm{SHB}}{\tau_\mathrm{SHB}}-\frac{\varepsilon_\mathrm{SHB}}{\tau_\mathrm{SHB}}\left[\exp(h_\mathrm{d}+h_\mathrm{SHB}+h_\mathrm{CH})-1\right]S(t,0)-\frac{\mathrm{d}h_\mathrm{d}}{\mathrm{d}t}-\frac{\mathrm{d}h_\mathrm{CH}}{\mathrm{d}t}\,, \tag{4}$$

$$h_\mathrm{in}=\int_0^z\frac{a\,J\tau_\mathrm{wr}}{ed}\mathrm{d}z'\,. \tag{5}$$

The total gain is given by:

$$G(t,z)=\exp\left[h_\mathrm{d}(t)+h_\mathrm{CH}(t)+h_\mathrm{SHB}(t)\right], \tag{6}$$

where $h(t)$ is an integral of optical gain per unit length over the length of QD-SOA and h_total equals the sum of h_d, h_CH and h_SHB. $S(t, 0)$ is the instantaneous input optical intensity inside the QD-SOA and h_d, h_w, h_CH and h_SHB are the h-factor values for carriers recombination between the wetting layers and the QDs, carrier heating and spectral hole burning, respectively. h_0 is the maximum value of integrated gain and G_0 = exp(h_0) is the unsaturated power gain. $\tau_{\mathrm{w}\to\mathrm{d}}$ is the transition rate between wetting layer and ground state in quantum dot, τ_wr is the carrier recombination rate in wetting layer, $\tau_{\mathrm{d}\to\mathrm{w}}$ is the excitation rate from ground state to wetting layer and τ_dr is the recombination rate in semiconductor dot. τ_SHB is the carrier-carrier scattering rate while τ_CH is the temperature relaxation rate. ε_SHB and ε_CH are the nonlinear gain suppression factors due to carrier heating and spectral hole burning. a is the differential gain of QD-SOA (a =2×10^{-15} cm^2), J is the injection current density, d is the total wetting layer thickness and e is the electron charge. The values of J and d used here are 4 kA/cm^2 and 0.5 μm, respectively. Factor α is derived from density of states and Fermi function in QD and wetting layer. It represents the ratio of carriers in the wetting layer and those in quantum dots. Large number of carriers are present in the wetting layer, which makes a fast transfer to QD when the QD carriers are depleted. The phase response is related to the temporal gain as:

$$\phi(t)=-0.5\left[\alpha\,h_\mathrm{d}(t)+\alpha_\mathrm{CH}h_\mathrm{CH}(t)\right], \tag{7}$$

where α is the traditional linewidth enhancement factor, α_CH is the carrier heating alpha factor and α_SHB is the spectral hole-burning alpha factor, α_SHB ~ 0[10, 11].

In the QD model used here, most of the carriers are injected into the wetting layer from which they transfer to the QD energy levels. The carrier relaxation time from the wetting layer to the QD is ~ 0.5−10 ps[8].

We assume the data stream pulse to be a Gaussian pulse, i.e.,

$$P_{A,B}(t)=\sum_{n=-\infty}^{n=+\infty}a_{nA,B}\,\frac{2\sqrt{\ln(2)}\,P_0}{\sqrt{\pi}\,\tau_{FWHM}}\times$$

$$\exp\left(-\frac{4\ln(2)(t-nT)^2}{\tau^2_{FWHM}}\right), \quad (8)$$

where $a_{nA,B}$ represents the nth data in data streams A and B, which equals 1 or 0. P_0 is the input pulse energy, and T is the bit period. τ_{FWHM} is the pulse width (full width at half maximum).

NAND gate is important for logic operations because logic operations can be built using a combination of NAND gates. In this work, NAND is demonstrated by a series combination of AND and INVERT operations as shown in Fig.2. The first SOA-MZI serves in the system as an optical logic AND gate. For AND operation, data stream A (centered at λ_1) is coupled into port 1 and the low power CW (wavelength λ_1) light into port 2, while data stream B (centered at λ_2) is split at port 3 and sent into both SOAs. Then we can receive the patterned interference light centered at λ_2 coming out of port 4. When data B = 0, no light centered at λ_2 is injected to the system, resulting in no output from port 4; when B = 1 and A = 0, the gain and phase shifted by two branches of data stream B in both SOAs are the same, and if the two phase shifters are used in the two arms to produce an initial phase difference of π between the two branches, they will undergo a destructive interference in port 4 and give "0" output bit; when B = A = 1, the two branches will experience different gains in the two SOAs and will have a constructive interference pattern at port 4. To sum up, only in the case when both data A and B are "1", this system can yield "1" at port 4, which is logic operation A AND B.

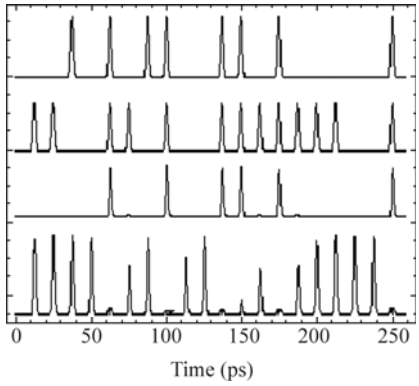
After screening out all other wavelength components using a band-pass filter (BPF), the A AND B output data stream (λ_2) is amplified to the desired power by an amplifier and guided into port 5 as data to one arm of the second MZI for INVERT operation. A clock pulse train with the same pulse shape and pulse energy (centered at λ_2) is injected to port 6 and the CW light (wavelength λ_1) is injected into port 7 as control beam. In this way, the result centered at λ_1 coming out from port 8 will be the XOR of signals injected into port 6 and port 5, or INVERT (A AND B), which is the same as logic A NAND B.

The modulated clock signals (probe) from the two arms of MZI interfere obeying the following formula:

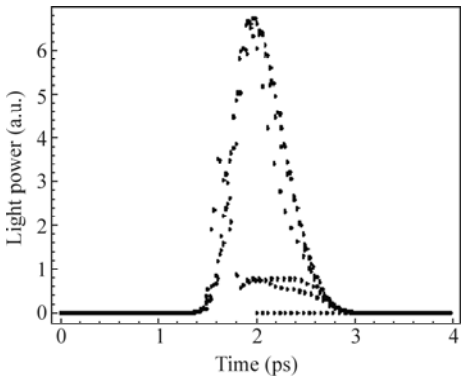
$$P_{\text{out}}(t) = 0.25\,P_{\text{in}}(t)\left\{G_1(t)+G_2(t)-2\sqrt{G_1(t)G_2(t)}\,\cos[\Phi_1(t)-\Phi_2(t)]\right\}, \quad (9)$$

where $P_{\text{in}}(t)$ is the input probe power (series of 1's), $G_1(t)$ and $G_2(t)$ are the control beam gains in two arms of SOA-MZI, and $\Phi_1(t)-\Phi_2(t)$ is the phase difference of the probe signal in two arms. Parameters used in this simulation are: P_0 = 0.2 pJ, τ_{FWHM} = 0.8 ps, $\tau_{\text{w}\to\text{d}}$ = 5 ps, $\tau_{\text{d}\to\text{w}}$ = 10 ns, τ_{wr} = 2.2 ns, τ_{dr} = 0.4 ns, τ_{CH} = 0.3 ps, τ_{SHB} = 0.1 ps, ε_{CH} = ε_{SHB} = 0.08 ps, α = 7, α_{CH} = 1 and P_{sat} = 28 mW.

Fig.3(a) illustrates the simulation results of NAND gate operation with a pattern of signal A and a pattern of signal B. The bottom trace shows the NAND output after QD-SOAs-MZIs. The eye diagram of an NAND bit for pseudo-random streams of A and B bits is shown in Fig.3(b). The primary reason for noise in this calculation (which lowers the quality factor) in the absence of ASE noise is pattern effect resulting from long recovery time of gain and gain-induced phase change.



(a)



(b)

Fig.3 (a) The simulated results of SOA-MZI for NAND output (Top two traces are the signals *A* & *B*, middle trace is the AND output and the bottom trace is NAND output); (b) The eye diagram for NAND

To investigate the quality of NAND operation by simulation, Q-factor of the NAND output signal has been calculated. The Q-factor gives the information of the optical signal to noise ratio (OSNR) in digital transmission. Q-factor is given by $Q = (S_1 - S_0) / (\sigma_1 + \sigma_2)$, where S_1, S_0 are the average intensities of the expected "1"s and "0"s, and σ_1 and σ_2 are standard deviations of those intensities. Q-factor increases with the decreasing carrier lifetime and drops with the increasing input pulse energy. We have investigated the effect of ASE power. The ASE power is related to N_{SP} by the relation[10,11]:

$$P_{\text{ASE}} = N_{\text{SP}}(G-1)h\upsilon B_0, \quad (10)$$

where G is the maximum gain, h is Plank's constant, υ is the frequency, and B_0 is the band width. The ASE noise is added numerically within the input pulse trains using Eq.(10) on the pattern effect noise to obtain the Q-factor. The Q-factor versus N_{SP} for NAND output is shown in Fig.4. For an ideal amplifier (N_{SP} = 2), the Q-factor is 17.8 for 30 dB gain.

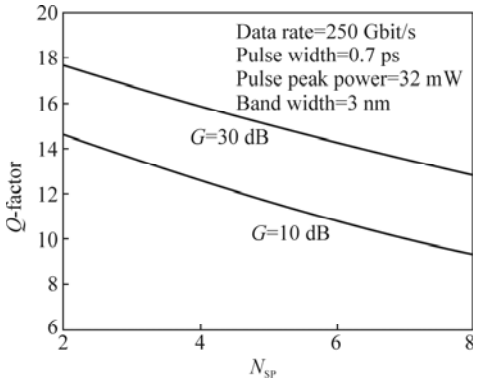


Fig.4 Q-factor versus N_{SP} for NAND operation

To obtain further information on the NAND gate performance, the Q-factors for different input single-pulse energies at 250 Gbit/s are calculated as shown in Fig.5. An increase of input pulse energy will make the SOAs easier to saturate, which results in a decrease in the Q-factor.

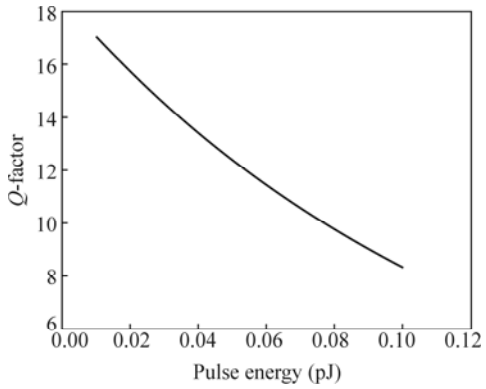


Fig.5 Q-factor versus pulse energy

The performance of all-optical logic NAND gate based on quantum dot-semiconductor optical amplifier (QD-SOA) has been simulated. Results show that the all-optical gate in QD-SOA-MZI based structure is feasible at 250 Gbit/s with proper quality factor (Q-factor). Effects of amplified spontaneous emission (ASE) and the input pulse energy on the system's Q-factor for all-optical logic NAND gate are studied. ASE is calculated as a function of the spontaneous emission factor (N_{SP}). A decrease in quality factor is predicted for high N_{SP}. The primary reason for the faster response of the QD-SOA compared with that of the SOA with a regular active region is the presence of the wetting layer. The wetting layer serves as a carrier reservoir layer. Carriers depleted by the injected optical pulse in the QD ground state are replaced via fast carrier transition from the wetting layer. Thus, the speed is limited by the relaxation time from the wetting layer to the QD state. For good performance (high Q-factor), both the injection current and the input power need to be optimized. The effect of ASE can be experimentally verified by adding wideband optical unmodulated signal to the data and measuring the Q-factor as a function of the intensity and band width of this signal. ASE effects are important for cascaded logic operations.

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