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A 33~170 GHz cascode amplifier based on InP DHBT technology

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Abstract: In this paper, a wide band cascode power amplifier working at 33~170 GHz is designed, based on the 500 nm InP dual-heterojunction bipolar transistor (DHBT) process. Two pairs of parallel input and output stub lines can effectively expand the working bandwidth. The output coupling line compensates the high frequency transmission. The measured results show that the maximum gain of the amplifier is 11.98 dB at 115 GHz, the relative bandwidth is 134.98 %, the gain flatness is ±2 dB, the gain is better than 10 dB and the output power is better than 1 dBm in the operating bandwidth.

Key words: InP dual-heterojunction bipolar transistor (InP DHBT), monolithic microwave integrated circuit (MMIC), cascode amplifiers, wide band

基于InP DHBT工艺的33~170 GHz共源共栅放大器

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摘要:基于500 nm磷化铟双异质结双极晶体管(InP DHBT)工艺,设计了一种工作在33~170 GHz频段的超宽带共源共栅功率放大器。输入端和输出端的平行短截线起到变换阻抗和拓展带宽的作用,输出端紧密相邻的耦合传输线补偿了一部分高频传输损耗。测试结果表明,该放大器的最大增益在115 GHz达到11.98 dB,相对带宽为134.98%,增益平坦度为±2 dB,工作频段内增益均好于10 dB,输出功率均好于1 dBm。

关 键 词:磷化铟双异质结双极晶体管(InP DHBT);单片微波集成电路(MMIC);共源共栅放大器;宽带

Introduction

With the increasing demand for high data rate and high resolution, it is foreseeable that millimeter wave radar, imaging and communication systems will become are widely applied [1-3]. But at higher frequencies, the achievable gain of tunable amplifiers is low, while distributed amplifiers inherently have wider bandwidths. Therefore the distributed topology is an important way to realize the wide band amplifier. In addition, the cascode amplifier structure also has wide band characteristics and can be used as a basic unit to form a distributed amplifier. The reported cascode amplifiers cover the DC-110 GHz[4], 110~170 GHz[5-6], and 140~250 GHz[7] frequency bands, however, designers always have to make a trade-off between bandwidth and gain.

In this paper, an ultra-wideband cascode amplifier operating at 33~170 GHz is demonstrated. The proposed amplifier can achieve 134.98% relative bandwidth and maintain a gain flatness of ±2 dB, with the small signal gain better than 10 dB and the output power better than 1

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dBm over the operating bandwidth.

1 InP DHBT technology

The monolithic microwave integrated circuit (MMIC) was fabricated based on 500-nm dual-heterojunction bipolar transistor (DHBT) process on 3 inch semi-insulating InP substrate using molecular-beam epitaxy (MBE) manufactured by Nanjing Electronic Devices Institute. An InGaAsP composite collector was used to eliminate the current blocking effect caused by the B-C heterojunction conduction band spike[8]. The composite collector area consist of an InGaAs layer, a step-graded InGaAsP layer, and a δ-doping layer, all the layer structures are listed in Table I[9-10]. The width of emitter contact is 500 nm, and two 300 nm wide base contacts at its both side. A transit frequency of 300 GHz and a maximum oscillation frequency above 400 GHz are extracted, as shown in Fig. 1. The process provides three wiring metal layers and compact interconnect vias between them. The MIM capacitor with 0.26 fF/μm^2 capacitance density and 25 Ω/square TaN TFR are also available[11].

Table 1 Layer structure of the InGaAs/InP DHBT
表1 InGaAs/InP基DHBT外延材料结构

Layer	Material	Thickness/nm	Dopant
Emitter contact	InGaAs	200	Si
Emitter	InP	200	Si
Base	InGaAs	35	C
Setback layer	InGaAs	30	Si
Step-graded	InGaAsP	50	Si
δ-doping	InP	5	Si
Collector	InP	150	Si
Collector contact	InGaAs	50	Si
Sub-collector	InP	200	Si
InP substrate		100 μm	S. I.

The schematic diagram of the multilayer integrated circuit process used in this paper is shown in Fig. 2. The thickness of the metal layer and corresponding BCB layer are all on the order of 1μm[12]. Each layer of metal can be used as a signal line or a common ground layer. However, when M2 or M3 is used as the ground, the interconnection structures are more complicated and will bring more parasitic mode effects. Therefore, M1 is used as the common ground, in which case only the windows around the series capacitors are opened that will greatly reduce the leak area[13]. Thin-film micro-strip lines (TFMLs) can be realized with M1 as ground and M3 for signal line shown in Fig. 2(b). The effective dielectric thickness is only a few micro-meters, and for a 50 ohm TFML, its line width is almost 12 μm in the band of 1~300 GHz[14].

2 Circuit design

Figure 3 shows the block diagram of a typical cascode amplifier. The common-emitter (CE) HBT produces the controlled output current, this controlled current flows into the common-base (CB) HBT and is buffered by the (CB) HBT. The buffer effect reduces the output resistance of (CE) HBT and reduce the voltage gain of (CE) HBT, which in turn reduces the Miller effect. Such structure has the benefits of better gain while maintaining good linearity and reverse isolation.

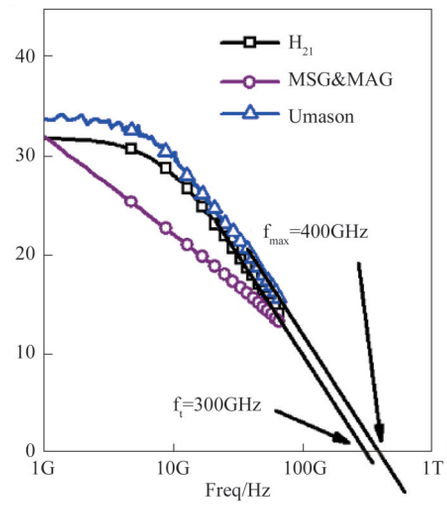

Fig. 1 The f_T and f_{max} of the transistor
图1 器件的fT和fmax

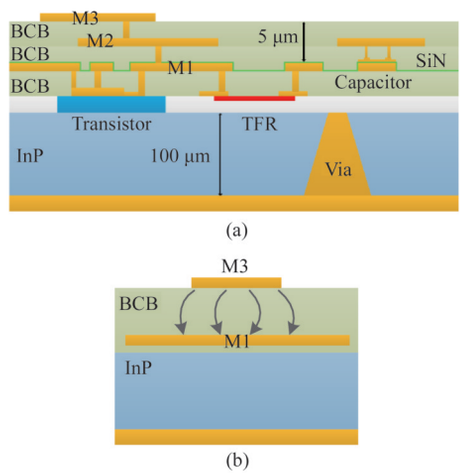

Fig. 2 Schematic cross-sectional view of (a) multilayer interconnect, and (b) thin-film microstrip lines
图2 (a)多层互联结构和,(b)薄膜微带线示意图

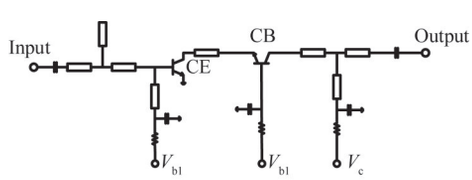

Fig. 3 Block diagram of the typical cascode amplifier
图3 典型共源共栅放大器结构示意图

Figure 4 shows the circuit topology for the designed cascode amplifier. In order to obtain wide bandwidth, two pair parallel open-ended stubs were respectively add-

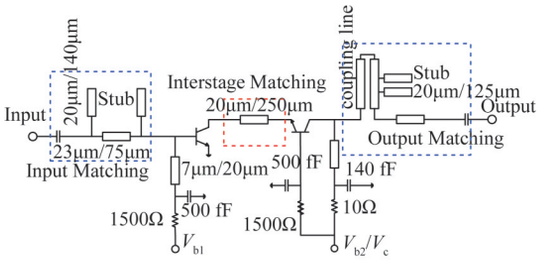

Fig. 4　Circuit topology for the wide band cascode amplifier
图4　宽带共源共栅放大器电路拓扑结构

ed to the input matching networks of the first stage (CE) HBT and the output matching networks of the second stage (CB) HBT. One pair of stubs is designed at the higher frequency band, and the other pair is designed at the lower frequency band. Figure 5 shows the amplifier's optimum power input and output impedance matching network schematics. This makes a trade-off between bandwidth and gain of the amplifier. The folded coupling lines act as parts of matching network while compensating some high frequency transmission loss. An impedance matching line with a width of 20 μm and a length of 250 μm was introduced between the two HBT devices. Since both (CE) HBT and (CB) HBT are supplied by V_c, then the stability of the cascode amplifier is sensitive to the current (the controlled CE output current) passing through the inter-stage matching line. Figure 6 shows this chip photograph of the cascode amplifier MMIC. The size is 1. 0 mm × 0. 8 mm.

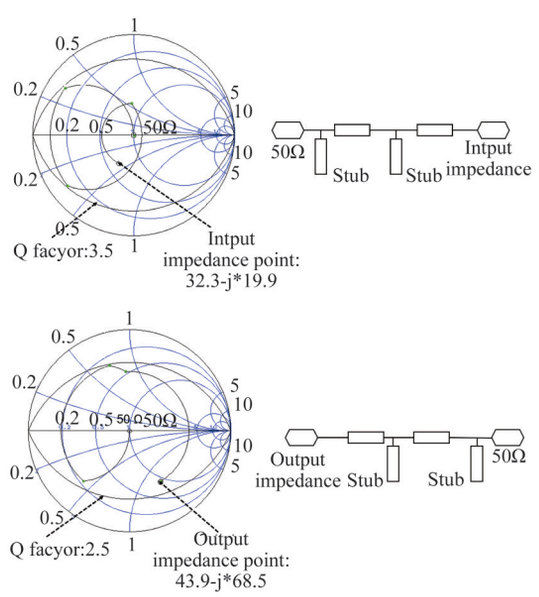

Fig. 5　Impedance matching Smith chart and the network schematic
图5　Smith chart匹配和拓扑结构

3　On-wafer measurement

Characterization of the MMIC cascode amplifiers were obtained by on-wafer measurements. The measured results are shown in Fig. 7 and Fig. 8. The S-parameter

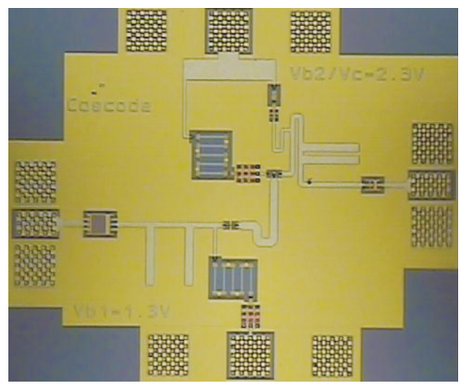

Fig. 6　Chip photograph of the cascode amplifier MMIC. Size: 1. 0 mm × 0. 8 mm
图6　放大器照片,整体尺寸:1. 0 mm × 0. 8 mm

measurements were performed using a Keysight PNA-X N5247B network analyzer with Keysight N5293AX01 (1~110 GHz) frequency extenders, and Rohde & Schwarz ZVA50 network analyzer with Rohde & Schwarz ZC170 (110~170 GHz) frequency extenders.

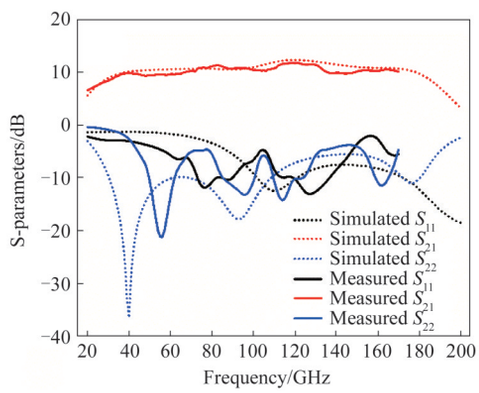

Fig. 7　Measured and simulated *S*-parameters of the broadband amplifier MMIC On-wafer bias: V_{b1}=1. 5 V, V_{b2}/V_c=2. 5 V
图7　仿真与测试S参数对比,在片测试偏置:V_{b1}=1. 5 V, V_{b2}/V_c=2. 5 V。

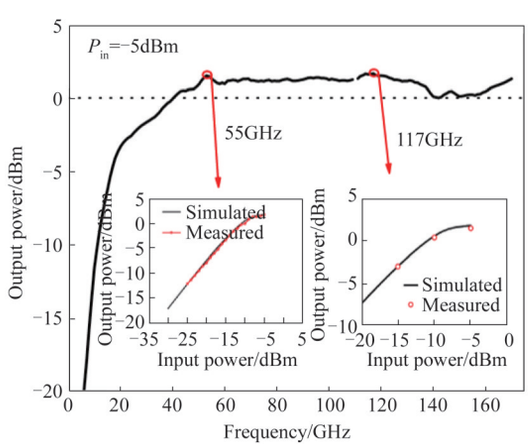

Fig. 8　Output power measured results
图8　输出功率测试结果

The measured results show that the maximum gain

Table 2 State-of-the-art of ultra-broadband amplifier
表2 超宽带放大器特性对比

Ref.	. *f*/GHz	Technology	Gain /dB	Gain Flatness/dB	Topology/ Devices	Chip-size /mm^2	Pout/dBm
[1]	40~185	500 nm InP DHBT	10	±2	Distributed ×10	0.8×0.75	10
[4]	0~110	100 nm GaAs pHEMT	6	±2.5	Cascode ×2	–	–
[5]	123~143	130 nm SiGe BiCMOS	24.3	–	Cascode ×10	0.7×0.43	7.7
[6]	110~170	SiGe BiCMOS	10.8	±2.5	Cascode ×2	0.035	–
[7]	118~236	35 nm GaAs mHEMT	10	–	Cascode ×8	1.5×0.5	10
This work	**33~170**	**500 nm InP DHBT**	**10**	±2	Cascode ×2	**1.0×0.8**	**1.8**

of the amplifier at 115 GHz is 11.98 dB, and the 3 dB bandwidth is 33 to 170 GHz (134.98%). Figure 7 also shows the simulation results of no stub or matched impedance line. Through comparison, it can be found that these stubs and matching lines can effectively increase the amplifier bandwidth. Signal fluctuations in the range of 65~85 GHz and 100~110 GHz are large, which is caused by overheating of the frequency extender modules for a long time. The spectrum spurs can be reduced by turning off the system and cooling, but it cannot be completely eliminated. The saturated output power of the device is 1.8 dBm at 117 GHz, when the input power is -5 dBm. The output power is better than 1 dBm in the range of 35~134 GHz, and greater than 0 dBm in the range of 41~170 GHz, as shown in Fig. 7. Accordingly, the output collector current is 5 mA at 2.5V supply and the peak power added efficiency (PAE) is 8.8%.

Table 2 shows the performance comparison of several wide band amplifiers. We noticed that this design provides the considerable gain, output power and bandwidth characteristics.

4 Conclusion

In this paper, a wide band amplifier is presented, which exhibits a good operating bandwidth (better than 1 dBm in the range of 35~134 GHz). The high 134.98% relative bandwidth completely covers the Q, V, W and D bands, which makes it a suitable option for measurement and spectroscopic systems. In the future, the cascode amplifier shown in this paper can be used as a cell to achieve greater output power through power combining.

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