文章编号：1001-9014(2022)04-0668-04

DOI:10.11972/j.issn.1001-9014.2022.04.002

Lateral linear mode avalanche photodiode through 0.35 μm high voltage CMOS process

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Abstract: This letter reports on a lateral linear mode avalanche photodiode through 0.35 μm high voltage CMOS process. The linear mode avalanche photodiode is designed and fabricated with the lateral separate absorption, charge and multiplication (SACM) structure using an epitaxial wafer. The DNTUB layer, DPTUB layer, Pi layer and SPTUB layer are used for the lateral SACM structure. This improves freedom of the design and fabrication for monolithic integrated avalanche photodiode without high voltage CMOS process modifications. The breakdown voltage for the lateral linear mode avalanche photodiode is about 114.7 V. The dark currents at gain M = 10 and M = 50 are about 15 nA and 66 nA, respectively. The effective responsive wavelength range is 450 ~ 1050 nm. And the peak responsive wavelength is about 775 nm at 20 V while M = 1. With unity gain (M = 1), the responsivity at 532 nm is about half of the maximum.

Key words: avalanche photodiode, lateral SACM, high voltage CMOS, breakdown voltage
PACS: 61.72.uf, 85.60.Bt, 85.60.Dw

基于0.35 μm高压CMOS工艺的横向线性雪崩光电二极管

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摘要:提出了一种基于0.35 μm高压CMOS工艺的线性雪崩光电二极管(Avalanche Photodiode, APD)。APD采用了横向分布的吸收区-电荷区-倍增区分离(Separate Absorption, Charge and Multiplication, SACM)的结构设计。横向SACM结构采用了高压CMOS工艺层中的DNTUB层、DPTUB层、Pi层和SPTUB层,并不需要任何工艺修改,这极大的提高了APD单片集成设计和制造的自由度。测试结果表明,横向SACM线性APD的击穿电压约为114.7 V。在增益M = 10和M = 50时,暗电流分别约为15 nA和66 nA。有效响应波长范围为450 ~ 1050 nm。当反向偏置电压为20 V,即M = 1时,峰值响应波长约为775 nm。当单位增益(M = 1)时,在532 nm处的响应度约为最大值的一半。

关 键 词:雪崩光电二极管;横向SACM;高压CMOS工艺;击穿电压
中图分类号:TN364 **文献标识码**:A

Introduction

Optical detection of visible and near-infrared (NIR) radiation (λ < 1100 nm) has been focused on various developments of silicon avalanche photodiodes (APDs).

Received date: 2021-10-21, **revised date**: 2022-05-25 **收稿日期**:2021-10-21,**修回日期**:2022-05-25
Foundation items:Supported by the Shanghai Pujiang Program (18PJ1410700), Key Laboratory of Defense Technology Funding of Chinese Academy of Sciences (CXJJ-20S004), and Innovation Program of Shanghai Institute of Technical Physics, Chinese Academy of Sciences (CX-268)
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APD is a semiconductor photodetector in which a photon carrier can be generated due to photoelectric effect of solid-state semiconductor material[1]. The avalanche multiplication of carriers can be triggered by the photon-generated carrier in strong electric field due to an impact-ionization mechanism[2]. The separate absorption, charge and multiplication (SACM) silicon APD[3-4] is a very attractive device with an internal avalanche gain for supporting high sensitivity and low illumination detection. It is also highly desirable to fabricate silicon APDs together with electronic circuits in a cost-effective and less-parasitic single-chip[5-6] through high voltage CMOS process without process modifications.

However, with the limitations of design rules for most CMOS process, it is extremely difficult to achieve a suitable charge layer which is used to modulate the electric field in multiplication region for the vertical SACM APDs. Until now, most commercial SACM APDs have not been able to meet the requirements of low-cost, high-performance, monolithic integration and large-scale arrays. And only units APD or small-scale linear array APD can be fabricated and available. In order to design and fabricate vertical SACM APD through CMOS process without any process modification there are two design approaches which are usually carried out to get a suitable charge layer. The first way is the transverse space doping modulation. The groups have designed several silicon APDs by applying lateral well modulation[7-8]. The other method is the compensation doping modulation. Some silicon APDs were designed by combining different doping process layers[9]. For most lateral structure silicon APDs, the ordinary lateral p-n junction is adopted with p type and n type doping[10-12].

In this letter, we report the fabrication and characterization of lateral linear mode avalanche photodiode based on 0.35 μm high voltage CMOS process without any technology rules modification. This linear mode APD is fabricated with the lateral SACM structure using the 15 μm thick epitaxial layer. The photosensitive surface is an octagonal region[13] which is partially covered with electrode metal and shielding metal. In the next section, the structure and fabrication of the APD will be introduced. Then, in Sect. 2, the APD will be characterized and discussed, including current, gain, breakdown voltage and responsivity. In Sect. 3, the conclusion of this work is given.

1　Device structure and fabrication

The cutaway schematic (not to scale) of the lateral SACM APD presented in this paper is seen from Fig. 1 (a). As shown in Fig. 1 (a), the linear mode APD is designed with lateral SACM structure including DNTUB (Deep-N-TUB) layer, DPTUB (Deep-P-TUB) layer, Pi (π) layer and SPTUB (Shallow-P-TUB) layer. The regular DNTUB layer and DPTUB layer for modulating electric field distribution are fabricated in 0.35 μm high voltage CMOS technology. The multiplication zone of such structure is between the central DNTUB layer and loop-locked DPTUB layer. As shown in Fig. 1 (b), this structure can ensure that the lateral electric field strength in absorption zone is much lower than that in the multiplication zone, thus to confine the avalanche to the multiplication zone. The high doping concentration of the top NPLUS layer and PPLUS layer can form ohmic contact with the front metal electrodes. Meanwhile, the top NPLUS layer and PPLUS layer supply voltage to the DNTUB layer and Pi layer. The SPTUB layer and DPTUB layer connected to the PPLUS layer serve as the transition layer. Except for the absorption zone surface, the other surfaces are covered with a separate metal layer to shield incident light. The shielded multiplication zone can effectively reduce the participation of holes generated from incident light absorption in avalanche process.

Figures 1 (c) and (d) are the microscopic picture of the complete lateral SACM APD device and the microscopic picture of the photosensitive region, respectively. The size of the complete APD device is 910 μm×910 μm. Excluding the center electrode, the area of the active octagonal photosensitive region is 618 μm^2. The size of the PAD is 100 μm×100 μm. The metal M3 layer and M4 layer are used as shielding layer and the top electrode, respectively.

2　Results and discussions

2.1　Current and gain

The light current and dark current of the lateral APD are measured through Keithley 4200A-SCS Parameter Analyzer. The unity gain for M = 1 is defined at the low reverse bias voltage of 20 V. Furthermore, the breakdown voltage of the lateral APD is defined as the reverse voltages at which the dark current reaches 1 μA[14]. The photocurrent is measured using a light source with center wavelength λ = 905 nm and spectral width $\triangle\lambda$ = 3 nm. The dark current in Fig. 2 shows that the breakdown voltage of the lateral linear mode APD is at about 114.7 V. The dark currents of the lateral APD are about 15 nA and 66 nA when the typical gains are set at M = 10 and M = 50, respectively.

The photocurrent multiplication gain defined through equation (1) is shown in Fig. 3. In the following formula, I_{light} represents the total current, I_{ph} denotes the photocurrent, V represents the reverse bias voltage and V_0 stands for the reference reverse bias voltage for M = 1[15]. V_0 = 20 V was used for the data shown in Fig. 3. The test result indicates that the reverse bias voltage of the device is about 114 V at the typical photocurrent multiplication gain M = 50. Besides, the photocurrent multiplication gain is up to 100 at reverse bias voltage of 114.5 V.

$$M = \frac{I_{ph}(V)}{I_{ph}(V_0)} = \frac{I_{light}(V) - I_{dark}(V)}{I_{light}(V_0) - I_{dark}(V_0)} \quad , \quad (1)$$

2.2　Responsivity

The normalized spectral responsivity for the lateral linear mode APD is obtained at the low bias voltage of 20 V with unity gain (M = 1) with the spectral responsivity test system and is shown in Fig. 4. The normalized responsive wavelength range of the device is tested to be 450~1 050 nm. The maximum responsivity wavelength of

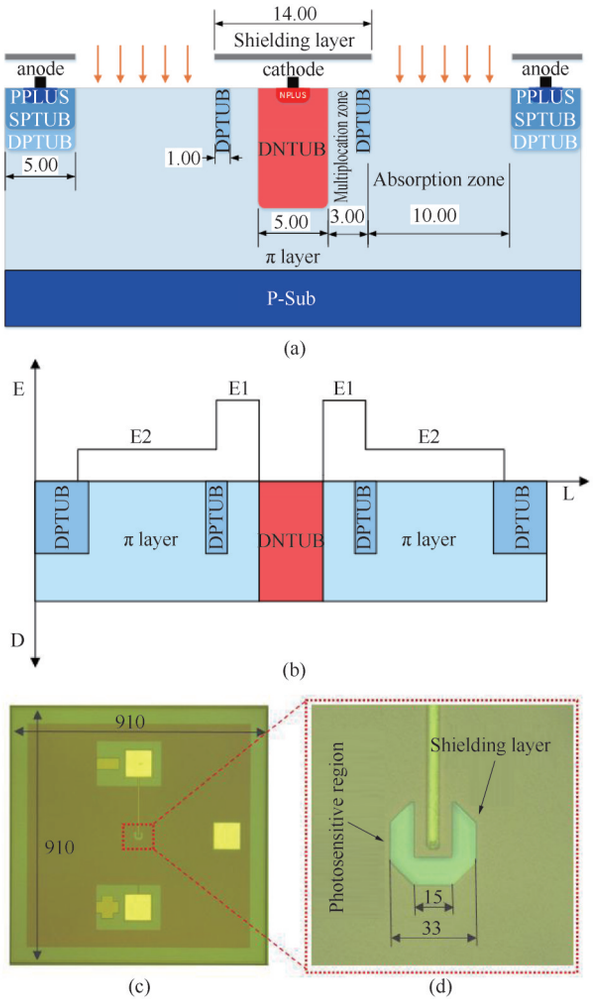

Fig. 1 Schematic views of APD (a) cross section, (b) simplified electric field distribution, (c) the microscopic picture of the complete APD device, (d) the microscopic picture of the photosensitive region (Unit: μm)

图1 APD示意图(a)横截面,(b)电场分布,(c)APD器件的显微照片,(d)光敏区的显微照片(单位:μm)

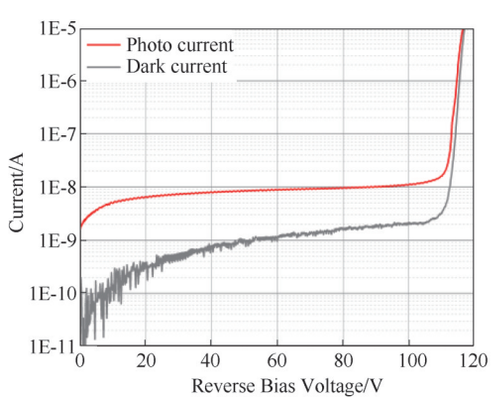

Fig. 2 Currents *vs.* reverse bias voltage

图2 电流-反向偏置电压特性

the device is about 775 nm at 20 V while M = 1. With unity gain (M = 1), the responsivity at 532 nm is about half of the maximum. As shown in Fig. 4, the spectral response curve reveals peak of interference with wavelength, which is caused by the multi passivation layers through 0.35 μm high voltage CMOS process. A black broken line is marked by fitting peaks of measured data. It shows the definite trend relationship between responsivity and wavelength (450~1 050 nm) if an anti-reflective coating (ARC) layer is fabricated through 0.35 μm high voltage CMOS process in the future.

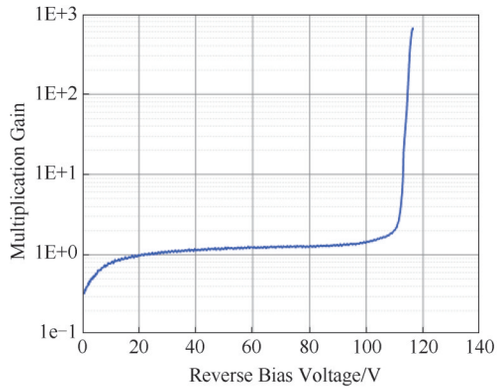

Fig. 3 Multiplication gain vs. reverse bias voltage

图3 增益-反向偏置电压特性

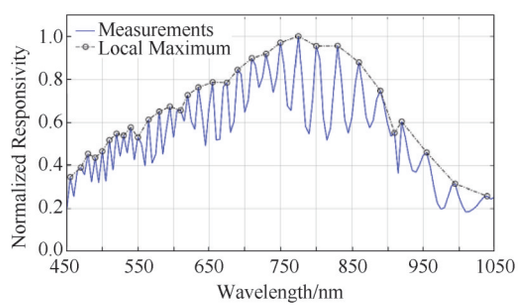

Fig. 4 Normalized responsivity vs. wavelength (450 ~ 1050 nm)

图4 归一化响应-波长特性

3 Conclusions

The lateral linear mode avalanche photodiode with the photo sensitive area of 618 μm^2 is implemented through 0.35 μm high voltage CMOS process. The lateral SACM and DNTUB/DPTUB/Pi/SPTUB layers are adopted. The breakdown voltage is observed about 114.7 V. And the dark currents are tested to be about 15 nA and 66 nA at gain M = 10 and M = 50, respectively. The responsive wavelength range is 450 ~ 1050 nm. The maximum responsivity wavelength is about 775 nm at 20 V while M = 1. With improved anti-reflective coatings (ARC), the spectral response of the device is expected to be better.

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