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A readout structure with double column buses and shared source follower for IRFPAs

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Abstract: A new readout circuit structure for infrared focal plane array with pixel-level shared source follower and double column buses is proposed in this paper. The voltage signal of the pixel is transferred through double column buses instead of single column bus, and therefore the non-uniformity and non-linearity caused by the parasitic resistor of the column bus is eliminated. By sharing the source follower within four adjacent pixels in the same column, the aspect ratio (W/L) and area of the source follower are increased to suppress the thermal noise, flicker noise and non-uniformity caused by process. A 640×512 readout circuit using this structure is designed and fabricated in 0.35μm 2P3M CMOS process and the pixel pitch is 15μm. The test results indicate the readout circuit receives a high dynamic range (DR) of 81dB high-quality infrared images with a low power consumption of 30mW. The nonlinearity is 0.11%, and the non-uniformity is less than 1%. Medium-wave infrared detector assembly is fabricated and tested. The assembly's non-uniformity is less than 5% and the NETD is 18mK. High-quality infrared images are obtained.

Key words: IRFPA, ROIC, shared source follower, double column buses
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一种像素级源跟随管共享的双列线信号传输的红外焦平面读出电路新结构

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摘要:提出一种像素级源跟随管共享、双列线信号传输的红外焦平面读出电路新结构。像素的电压信号通过两条列线传递到列级,消除了列线寄生电阻带来的非均匀性和非线性。同一列的相邻四行像素共享源跟随管,增大了源跟随管的尺寸和面积,从而降低了热噪声、闪烁噪声以及工艺偏差带来的非均匀性。采用该结构并基于0.35 μm 2P3M CMOS工艺设计和制造了一款640×512规格读出电路,像素中心距为15 μm。测试结果表明:功耗仅30 mW,动态范围81 dB,非线性度0.11%,非均匀性小于1%。与中波红外探测器阵列互连后进行了组件测试和成像实验,组件非均匀性小于5%,NETD为18 mK,获得了高质量红外图像。

关 键 词:红外焦平面;读出电路;源跟随管共享;双列线

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Introduction

Infrared imaging systems are widely used in the national defense, science, medical and industrial fields [1-3]. The infrared focal plane detector assembly is the core of the infrared imaging system, which consists of a photodiode array and a readout circuit interconnected by indium bumps [4-5]. The readout circuit achieves the amplification and acquisition of the photodiode array signals, and has a significant impact on the performance of

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the infrared imaging system [6-8]. With the development of infrared imaging system, the scale of the detector array is increasing and the pixel pitch is decreasing. As a result, the non-uniformity and nonlinearity of the array are gradually increasing due to process fluctuation and parasitic effect [9]. Meanwhile, the shrinking pixel pitch also results in a challenge to high signal-to-noise ratio (SNR) [10-11].

The pixel circuit in the readout circuit is directly connected to the photodiode to integrate the photocurrent. Two modes are typically used to readout the pixel signal: charge readout mode [7,9] and voltage readout mode [12-15]. In the charge readout mode, with the increase of the array size, the parasitic capacitance of the column bus becomes larger and degrades the SNR when the signal is transferred from pixel to column. Accordingly, the charge readout mode is not suitable for a large-scale readout circuit [16]. In the voltage readout mode, an op-amp or a source follower (SF) is needed in the pixel to transfer the signal from pixel to column. However, the small pixel size limits the area of the op-amp or source follower, which results in poor noise performance [16-17]. Moreover, the non-uniformity introduced by process fluctuations will increase due to the increase of the array scale [18-21].

This paper proposes a new voltage readout structure to solve the problems mentioned above. The signal is transferred from pixel to column by double column buses instead of single column bus, reducing the non-uniformity and the nonlinearity caused by the parasitic resistor of the column bus. The source follower within four adjacent pixels in the same column is shared to increase the area and the aspect ratio. Therefore the non-uniformity and noise are reduced.

The content of this paper is as follows. Section 1 will introduce the new structure and operating principle of the proposed readout circuit, focusing on the analysis of double column buses readout mode and the four-pixel-shared source follower. And simulation results are presented as well. Section 2 will present the test results and imaging experiment. The conclusion will be given in Section 3.

1 The structure and principle of the readout circuit

1.1 Conventional readout circuit structure

The conventional 640×512 readout circuit architecture with voltage readout mode is shown in Fig. 1. The operating principle of the circuit is as follows. First, the pixel circuit converts the photocurrent into a voltage signal. Second, the voltage in the pixel circuit is transferred to column circuit row-by-row. Finally, the voltage in column circuit is sent off-chip through the output buffer column-by-column.

The circuit of conventional voltage readout mode [13,20,22] is shown in Fig. 2 and single column bus is used to transfer signal from pixel to column. As the scale of the array increases, the length of the column bus is also increasing, and its parasitic resistor is gradually becoming non-negligible.

It can be seen in Fig. 2 that the sources of M1 and M2 are connected through the parasitic resistor of the column bus instead of connected directly. The parasitic resistor mainly includes the bus parasitic resistor (513-i)× R_U and the R_{on} of the row selection switch, where R_U is the parasitic resistor of a metal wire with the length of one pixel and i is row number. (513-i) is the number of the unit resistors which are connected in series and depends on the location of the pixel. Since the parasitic resistor of the column bus is network-like, (513-i) differs with different pixel, which results in different voltage drops of corresponding pixel signals. Therefore, the output V_{OUT} will show a great spatial non-uniformity.

$$V_{OUT}(i,j) = V_{INT}(i,j) - V_{gs,1} - I_0 \times \left(R_{on} + (513 - i) \times R_U\right) + V_{gs,2} \approx V_{INT}(i,j) - I_0 \times (R_{on} + (513 - i) \times R_U) \quad . \quad (1)$$

The term of $i \times R_U$ is increasing as the scale of the array increases and the entire array will show a greater spatial non-uniformity.

In the readout circuits [13,20,22], V_{INT} of the pixel is read through the source follower in the pixel. As the pixel pitch decreases, the area of the source follower is decreasing, so the mismatch of the source followers within different pixels will result in a severe non-uniformity. Moreover, the area and *W/L* of the source follower are limited by the pixel area. Since the thermal noise and flicker noise of the source follower are the main sources of noise in the signal path, the noise from the pixel-column transmission is seriously affected by the pixel area.

1.2 The proposed readout circuit structure

To solve the above problems, a readout structure with pixel-shared source follower and double column buses transmission is proposed as shown in Fig. 3.

The pixel-column signal transmission is completed through two column buses, eliminating the non-uniformity caused by the parasitic resistor and the nonlinearity caused by the source follower. The four adjacent pixels in the same column share a source follower, increasing the *W/L* and area of the source follower. Thereby the thermal noise, flicker noise, and non-uniformity caused by process variations are reduced. The circuit diagram of the signal path is shown in Fig. 4.

The working principle is as follows. When RS<1> and RSW<1> is high, the voltage V_S is transferred to the column circuit by the shared source follower of the four adjacent pixel circuits. Thus, the area and the *W/L* of the source follower is four times of that of one single pixel. When the switches M_{SA} and M_{SB} are turned on, the current through M1 flows into M3 through M_{SA} and the column bus BUSA. Similarly, the current through M2 flows into M4. Hence there is no current flowing through M_{SB} and the column bus BUSB and no additional voltage drop over the parasitic resistor of this signal path. The source voltages of M1 and M2 are equal. The output voltage is:

$$V_{OUT}(i,j) = V_S(i,j) - V_{gs,1} + V_{gs,2} - I_0 \times 0 = V_S(i,j). \quad (2)$$

The proposed structure and the conventional structure are

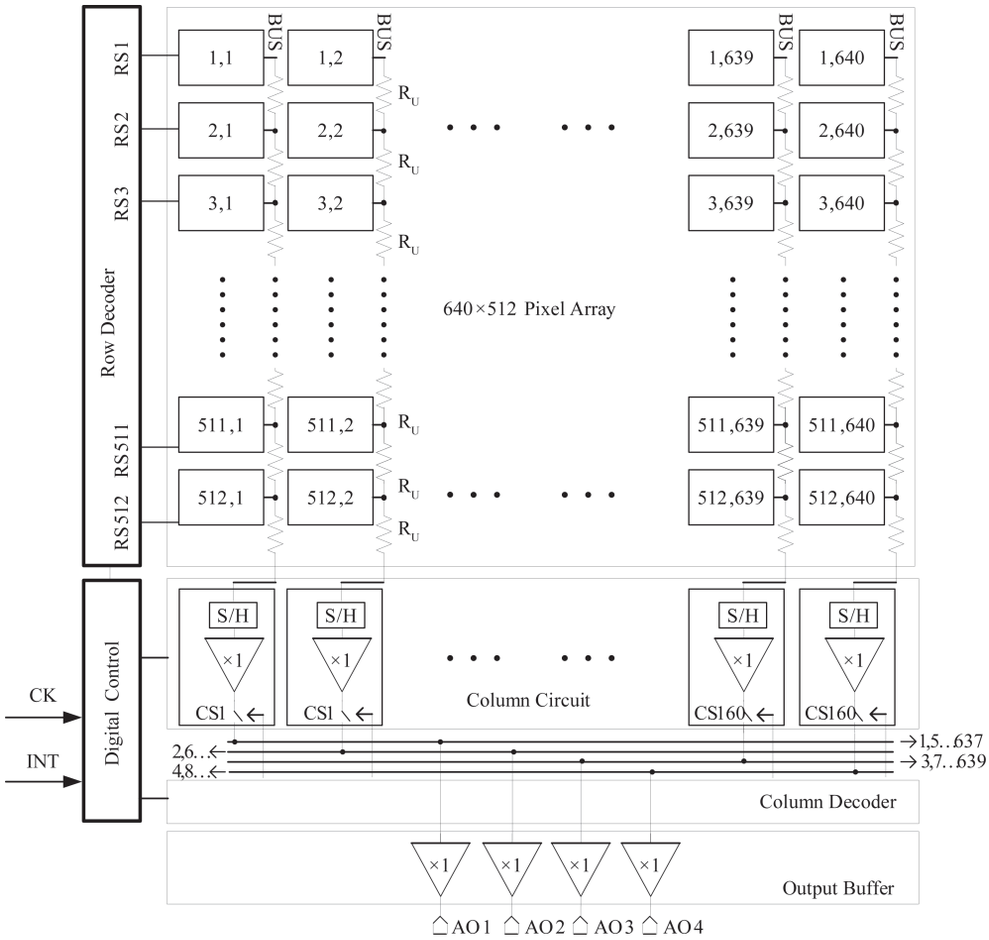

Fig. 1 Block diagram of the 640×512 conventional voltage readout mode readout circuit.
图1 传统电压读出模式640×512读出电路的框图

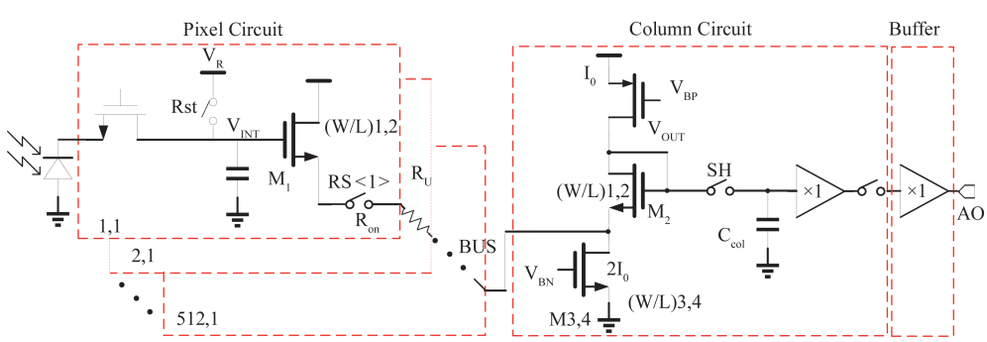

Fig. 2 Circuit diagram of the conventional voltage readout mode readout circuit.
图2 传统电压读出模式读出电路的电路图

compared by simulation. The nonlinearity and non-uniformity caused by the parasitic resistors of column bus and MOS switch are simulated and the results are shown in Fig. 5.

Shared source follower of four adjacent rows firstly reduces the local non-uniformity within four rows. It also increases the area of the source follower by four times and the macroscopic non-uniformity of the entire array can be reduced. Monte-Carlo simulations are performed to compare the non-uniformity of the conventional structure and the proposed structure. The simulation result is shown in Fig. 6 and the proposed structure has lower non-uniformity.

The simulation results of Fig. 5 and Fig. 6 are summarized in Table 1.

The pixel- shared source follower can reduce the noise as well as reduce the non-uniformity of the array. As shown in Fig. 2, the equivalent input noise introduced by the signal transmission from pixel to column is V_n^2. It includes not only the noise of the source follower MOSFETs but also the noise of the current source MOSFETs. The current source MOSFETs in the column have

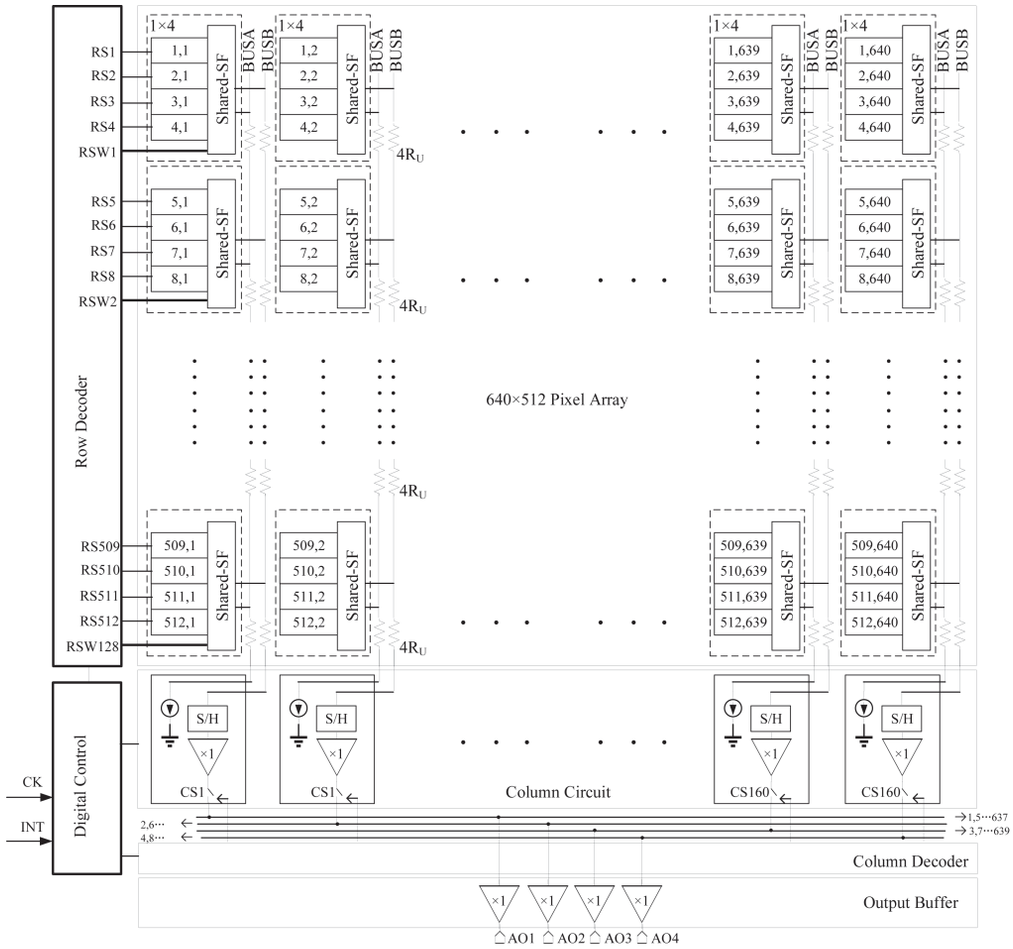

Fig. 3　Block diagram of the pixel-level shared-SF and double column buses readout circuit.
图3　像素级源跟随管共享的双列线读出电路的框图

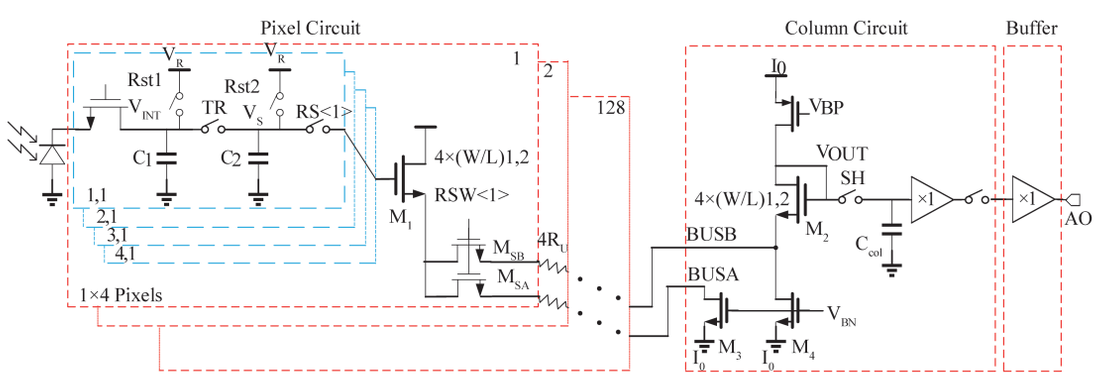

Fig. 4　Circuit diagram of the pixel-level shared-SF and double column buses readout circuit.
图4　像素级源跟随管共享的双列线读出电路的电路图

less area limitation and their noise contribution can be designed to be negligible. The main noise source is the same size source followers of M1 and M2. V_n^2 can be simplified as follows:

$$V_n^2 \approx 2 \times \left(V_{n,t,M1}^2 + V_{n,\frac{1}{f},M1}^2 \right)$$
$$\approx 2 \times \left(\frac{4KT\lambda}{g_{m1}} \times f_1 + \frac{K_n}{C_{ox} W_1 L_1} \times \ln \frac{f_1}{f_0} \right), \quad (3)$$

f_1 is the upper limit of the noise integration bandwidth, f_0 is the lower limit of the flicker noise integration. As shown above, the noise includes thermal noise and flicker noise. Since the readout circuit operates at the temperature of liquid nitrogen, the thermal noise is relatively small compared to the flicker noise. To reduce the flicker noise, it's necessary to increase the area of the M1 and M2. The source followers M1 and M2 are limited by the pixel area and the matching relationship respectively, so the flicker noise cannot be effectively reduced.

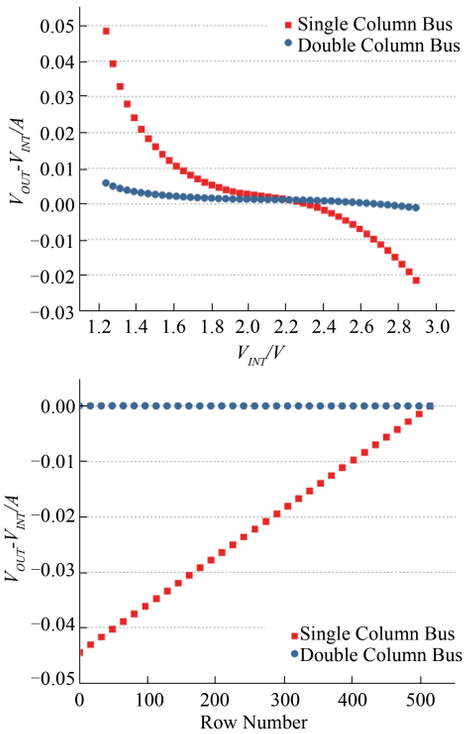

Fig. 5 Simulation results of the output deviation of the conventional and the proposed structure
图5 传统结构和新型结构的输出偏差仿真结果

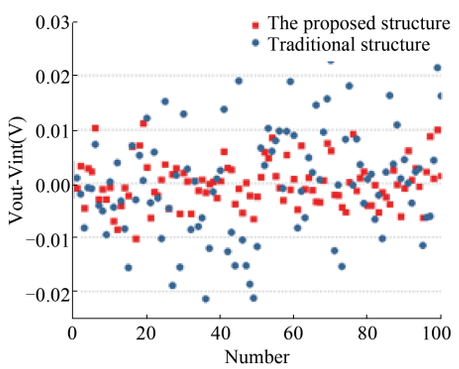

Fig. 6 Monte-Carlo simulation results of the conventional and the proposed structure
图6 传统结构和新型结构的蒙特卡洛仿真结果

Table 1 Comparison of the nonlinearity and non-uniformity between the conventional and the proposed structure
表1 传统结构和新型结构的非线性和非均匀性性能的比较

Structure	Nonlinearity (Parasitic Resistor)	Non-uniformity (Parasitic Resistor)	Non-uniformity (Process Fluctuation)
conventional structure	2.78%	2.5%	1.67%
proposed structure	0.27%	<0.1%	<0.6%

The proposed pixel circuit uses a shared source follower of four adjacent pixels in the same column, and the source follower's area is increased by four times compared with the conventional structure. In this case, the equivalent input noise $V_n'^2$ is:

$$V_n'^2 \approx 2\times\left(V_{n,t,M1}'^2 + V_{n,\frac{1}{f},M1}'^2\right) \approx 2\times\left(\frac{4KT\lambda}{g'_{m1}}\times f_1' + \frac{K_n}{4C_{ox}W_1L_1}\times\ln\frac{f_1'}{f_0}\right). \quad (4)$$

Since the frequency range of noise integration can be adjusted by the loading capacitance, f_1 and f_1' can be equal. The ratio of g'_{m1} to g_{m1} is k. If the source follower MOSFETs of both structures work in the saturation region, k is approximately 2. If the source followers work in the sub-threshold region, k is slightly less than 2.

$$g'_{m1} = \mathrm{k}\times g_{m1}, \quad (5)$$

The ratio of the equivalent input noise of the two structures is as follows:

$$\frac{V_{n,\mathrm{tran}}}{V'_{n,\mathrm{tran}}} \approx \sqrt{\frac{2\times\left(V_{n,t,M1}^2 + V_{n,\frac{1}{f},M1}^2\right)}{2\times\left(V_{n,t,M1}'^2 + V_{n,\frac{1}{f},M1}'^2\right)}} = \sqrt{\frac{V_{n,t,M1}^2 + V_{n,\frac{1}{f},M1}^2}{\frac{V_{n,t,M1}^2}{k} + \frac{V_{n,\frac{1}{f},M1}^2}{4}}} > \sqrt{k}. \quad (6)$$

It can be seen that when source-followers in n pixels are shared, the area increases by n times, the flicker noise reduces to $1/\sqrt{n}$ the thermal noise reduces significantly because of the increase of g_m.

2 Experimental results

Based on the proposed structure of shared source follower and double column buses, a readout circuit for medium-wave infrared imaging system is designed and fabricated using a 0.35μm 2P3M CMOS process. The array size is 640×512 and the pixel pitch is 15μm. The supply voltage is 3.3V. Fig. 7 shows the photograph of the readout circuit chip.

The readout circuit has two operation modes: integration while read (IWR) mode and integration then read

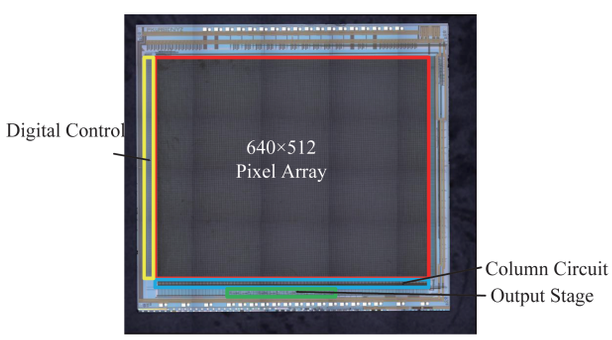

Fig. 7 Photograph of the 640×512 readout circuit chip.
图7 640×512规格读出电路芯片照片

(ITR) mode. Fig. 8 shows the test results of noise and nonlinearity in IWR mode. Fig. 8(a) shows the output rms noise with different integrated charge, and Fig. 8 (b) shows the nonlinearity of different V_{INT}. As we can see from Fig. 8, the noise of the readout circuit is less than 0.2 mV, and the nonlinearity is 0.11%. The dynamic range (DR) is calculated from noise and output swing to be 81 dB. The non-uniformity is tested to be less than 1%. The output buffer of the readout circuit adopts the circuit structure in Ref. [24], which significantly reduces the power consumption while increases the output rate. The total power consumption of the readout circuit is only 30 mW.

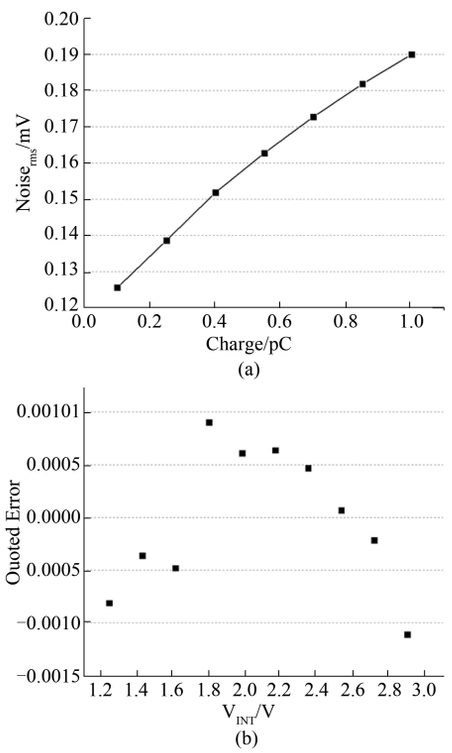

Fig.8　Test results of the readout circuit in IWR mode: (a) noise, (b) nonlinearity
图8　读出电路在IWR模式下的测试结果:(a) 噪声,(b) 非线性

The readout circuit is interconnected with mercury cadmium telluride (MCT) detector array by indium bumps, and the detector assembly is tested at the temperature of liquid nitrogen. The NETD is 18 mK and the non-uniformity is less than 5%. An infrared image captured by this assembly is shown in Fig. 9.

Fig. 9　Imaging result of the infrared imaging system.
图9　红外成像系统的成像结果

The performance parameters of the readout circuit and imaging system are compared with other literatures in Table 2. It can be seen that our work has obvious advantages in terms of noise and power consumption.

3　Conclusion

This paper presented a new readout structure for infrared focal plane array. The voltage signal is transferred from pixel to column by double column buses instead of a single column bus. The non-uniformity and the nonlinearity caused by parasitic resistor of column bus are eliminated. The source follower MOSFET is shared within four adjacent pixels. The transconductance and area of the source follower are increased and the thermal noise, flicker noise, and non-uniformity caused by the source follower mismatch are suppressed. A readout circuit using this structure is designed and fabricated in 0.35μm 2P3M CMOS process. It is assembled with mercury cadmium telluride (MCT) detector array and high-quality infrared images are obtained.

Table 2　Comparison of the performance parameters of readout circuits
表2　读出电路性能参数比较

Parameters	[23]	[11]	[20]	This work
Pixel size	15 μm×15 μm	15 μm×15 μm	7.5 μm×7.5 μm	15 μm×15 μm
Array size	640×512	640×512	640×512	640×512
Process	N/A	0.35μm CMOS	0.18μm CMOS	0.35μm CMOS
Power	50 mW	60 mW	N/A	30 mW
Charge handling capacity	5.0 Me^-	6.6 Me^-	3.1 Me^-	7.0 Me^-
NETD	25 mK	20 mK	25.5 mK	18 mK
Frame frequency	100 Hz	100 Hz	100 Hz	120 Hz

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References

[1] Rogalski A. Infrared detectors: status and trends [J]. *Progress in quantum electronics*, 2003, **27**(2-3): 59-210.
[2] Sizov F F. IR region challenges: Photon or thermal detectors? Outlook and means [J]. *Semiconductor physics quantum electronics & optoelectronics*, 2012,15(3): 183-199.
[3] Piji B, Jun Z, Fuzhong H. Review of digital mid wave infrared focal plane array detector assembly [J]. *Infrared and Laser Engineering*, 2017, **46**(1): 0102003.
[4] DONG Shu-Cheng, WANG Jian, TANG Qi-Jie, *et al*. Design of a multiband near-infrared sky brightness monitor using an InSb detector[J]. *Review of Scientific Instruments*, 2018, **89**(2): 023107.
[5] Kopytko M, Jóźwikowski K, Martyniuk P, *et al*. Status of HgCdTe barrier infrared detectors grown by MOCVD in Military University of Technology [J]. *Journal of Electronic Materials*, 2016, **45**(9): 4563-4573.
[6] YAO Li-Bin. CMOS readout circuit design for infrared image sensors [C]. International Symposium on Photoelectronic Detection and Imaging, 2009. International Society for Optics and Photonics, 2009. **7384**: 73841B.
[7] Mottin E, Pantigny P, Boch R. Improved architecture of IRFPA readout circuits[C]. Infrared Technology and Applications XXIII. International Society for Optics and Photonics, 1997, **3061**: 117-126.
[8] GONG Hai-Mei, SHAO Xiu-Mei, LI Xiang-Yang, *et al*. Advanced technology and application of spaceborne infrared detectors [J]. *J. Infrared and Laser Engineering*, (龚海梅, 邵秀梅, 李向阳, 等. 航天先进红外探测器组件技术及应用. 红外与激光工程) 2012(12): 15-26.
[9] LIU Jun-Ming, GUO Qiang, WANG Wei, *et al*. Response characteristic of InSb IRFPA under high reverse bias condition[C]. Advances in Infrared Imaging and Applications. International Society for Optics and Photonics, 2011, **8193**: 81932C.
[10] Tribolet P M, Chorier P, Manissadjian A, *et al*. High-performance infrared detectors at Sofradir[C]. Infrared Detectors and Focal Plane Arrays VI. International Society for Optics and Photonics, 2000, **4028**: 438-456.
[11] Lee I I. Silicon readout ICs for third-generation 2D IR focal-plane arrays operating over the wavelength range 8 - 12 μm[J]. *Russian Microelectronics*, 2008, **37**(2): 114-120.
[12] GUAN Yu, WANG Jin-Chun, MA De-Jun. Design of 128× 128 two-color IRFPA readout circuit[C]. Applied Optics and Photonics China, 2015: Optical and Optoelectronic Sensing and Imaging Technology. International Society for Optics and Photonics, 2015, **9674**: 967434.
[13] Tribolet P M, Chorier P, Dugalleix S, *et al*. Lightweight, compact, and affordable MW TV-format IR detectors[C]. Infrared Technology and Applications XXX. International Society for Optics and Photonics, 2004, **5406**: 193-204.
[14] Ballet P, Noël F, Pottier F, *et al*. Dual-band infrared detectors made on high-quality HgCdTe epilayers grown by molecular beam epitaxy on CdZnTe or CdTe/Ge substrates [J]. *Journal of electronic materials*, 2004, **33**(6): 667-672.
[15] Benson J D, Cornfeld A B, Martinka M, *et al*. Ellipsometric Determination of CdZnTe preparation for HgCdTe MBE Growth [C]. APS March Meeting Abstracts. 1996.
[16] Choi J H, Kim S H, Kim C Y, *et al*. Development of mid-wave 320x256 infrared focal plane array in Korea[C]. Infrared Technology and Applications XXXIII. International Society for Optics and Photonics, 2007, **6542**: 65420H.
[17] Tribolet P, Destefanis G. Third generation and multicolor IRFPA developments: a unique approach based on DEFIR[C]. Infrared Technology and Applications XXXI. International Society for Optics and Photonics, 2005, **5783**: 350-365.
[18] Baylet J, Gravrand O, Laffosse E, *et al*. Study of the pixel-pitch reduction for HgCdTe infrared dual-band detectors[J]. *Journal of electronic materials*, 2004, **33**(6): 690-700.
[19] Guériaux V, Belhaire E, Besnard V. Image quality for an IRFPA: a system integrator point of view[C]. Infrared Imaging Systems: Design, Analysis, Modeling, and Testing XXX. International Society for Optics and Photonics, 2019, **11001**: 110010D.
[20] Bisotto S, Abergel J, Dupont B, *et al*. 7.5 μm and 5μm pitch IRFPA developments in MWIR at CEA-LETI[C]. *Infrared Technology and Applications XLV. International Society for Optics and Photonics*, 2019, **11002**: 110021C.
[21] ZHONG Yan-Ping, YUAN Hong-Hui, JU Guo-Hao. Design of RO-IC for long wave photoconductive detector with nonuniformity correction [J]. *J. Infrared and Laser Engineering*, (钟燕平, 袁红辉, 鞠国豪. 非均匀性校正的长波光导探测器读出电路设计. 红外与激光工程) 2018(1):105-110.
[22] Fièque B, Lamoure A, Salvetti F, *et al*. Development of astronomy large focal plane array" ALFA" at Sofradir and CEA[C]. High Energy, Optical, and Infrared Detectors for Astronomy VIII. International Society for Optics and Photonics, 2018, **10709**: 1070905.
[23] Bouakka-Manesse A, Jamin N, Delannoy A, *et al*. Space activity and programs at SOFRADIR[C]. Planetary Defense and Space Environment Applications. International Society for Optics and Photonics, 2016, **9981**: 998109.
[24] HUANG Zhao-Feng , NIU Yu-Ze , LU Wen-Gao , *et al*. Low-power, high-speed output buffer with shared-TIA for ultra-large IRFPAs [J]. *Electronics Letters*, 2019, **55**(4):176-178.