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Compact on-chip structured illumination system based on integrated optics

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Abstract: Structured illumination has been used for several decades in the field of three-dimensional (3D) shape measurement and machine vision. However, the bulky structured illumination generation system limits its potential in practical applications. In this paper, a compact design method based on the silicon-on-insulator (SOI) optoelectronic integrated chip is proposed. Compared with the traditional structured light generation methods, the chip-based illumination method is simple, stable and flexible. The beam modulation and interference are achieved by on-chip devices, which efficiently avoids external disturbance and increases the portability of system. This is the first time using only on-chip devices to control the infrared beam and generate structured light pattern. The chip can provide an illumination area of about 200*200 μm^2 with the chip size of 0.5*0.5 mm. The illumination area and structural period are related to the design of grating couplers and the wavelength of light. Moreover, different illumination patterns can be achieved by appropriately designing the optical devices on the chip.

Key words: integrated optics, structured illumination, on-chip, gratings
PACS: 42.79.Gn, 42.82.Et, 42.82.Bq

一种基于光学集成芯片的紧凑型结构光产生系统

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摘要:过去的几十年中,结构光照明在三维立体成像和计算机视觉有着重要的应用。然而,传统结构光产生系统结构复杂、体积庞大,这严重限制了它的潜在应用价值。提出了一种用于产生结构光的紧凑型的光电集成芯片,这种芯片基于绝缘体上的硅(SOI)材料。该方法具有结构简单、输出稳定、设计灵活等优势。不同于传统的结构光发生系统,该方法中,光束的强度及相位调制以及光束间的相互干涉都是由片上系统操控的。这有效避免了外界扰动对光斑质量的影响,同时提升了系统的便携性。实现了全片上调控的红外结构光产生系统。该结构光芯片大小仅为0.5×0.5 mm,可以产生约200×200 μm的结构光照明区域。芯片照明区域的大小和结构光的单元结构周期与光栅的结构设计和光源波长相关。此外,通过设计合理地设计芯片上的元件布局,我们可以得到多种不同结构的照明图样。

关 键 词:集成光学;结构光;片上;光栅
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Introduction

Structured light illumination is a special illumination method which is effective in performing 3D shape measurement and machine vision.[1-2] Rapid development in 3D scanner strengthens the need to produce high-quality structure light with a convenient and effective way.

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For generating a structured illumination field, various methods are explored. The traditional methods to produce structure light usually rely on beam splitters and gratings. [3] Currently, the most common way for generating structured light pattern is using a spatial light modulators (SLM). Low-coherence LED light combined with a digital micro-mirror device (DMD) is another practical way to project structure light. [4-5] However, the grating methods need mechanical rotation to modulate the beam, which result in inefficiency. The SLM methods can only modulate polarized light and have a narrow operating bandwidth. The DMD methods have the disadvantage of low energy efficiency. All of these methods require the use of free-space optics. The optical setups are complicated and expensive. Furthermore, the free-space optical elements may introduce distortion and power loss as well as their bulkiness and spatial redundancy.

In this letter, a novel portable and economical structured light generation system based on an optoelectronic integrated chip with a broad bandwidth is proposed. In this method, lights coupled out from specific gratings interfere mutually above the chip and afterwards generate the necessary excitation patterns of structured illumination microscopy (SIM). An upright microscope is placed directly on the top of the integrated chip to gather specimen images. The beam intensities and phases steps are modulated on the chip taking advantage of thermo-optic or electro-optic effect. This design enables beam control without the need for free-space bulky equipment. The integrated chip is based on silicon-on-insulator (SOI), which has been mentioned in our previous work. [6] SOI waveguide structures are very promising and interesting for the realization of high-density photonic integrated circuits as they are intrinsic fully compatible with complementary metal-oxide semiconductor (CMOS) technology. [7-11] Also, silicon has a relatively large thermo-optic and electro-optic coefficient resulting in an easy and stable way to achieve phase modulation. [12-13] These characteristics make it a suitable material of the integrated photonic circuit chip. This is the first time using only on-chip devices to generate and modulate infrared structure light. The on-chip design can not only reduce the space waste, but also lower the cost. Because the light propagation and control are all done in the waveguide, it can efficiently avoid the disturbances caused by changes of external environment such as temperature variation, vibration and so on. The period and shape of the interference fringe are totally determined by the chip design. The flexibility of the chip design makes it possible to develop even new illumination patterns and will have broad applications in the future.

1 Chip design

The layout of the structured illumination chip composes with three crucial parts, which are input and output grating couplers, beam splitters and intensity and phase step modulators. The schematic of the on-chip optics is shown in Fig. 1. GC stands for grating coupler; BPS stands for beam power splitter and BM stands for beam modulator. After coupled into the integrated chip, the beam is separated evenly by splitters. The beam intensity and phase of each channel are modulated separately. The modulated beams will couple out through specific gratings to generate interference pattern upon the chip.

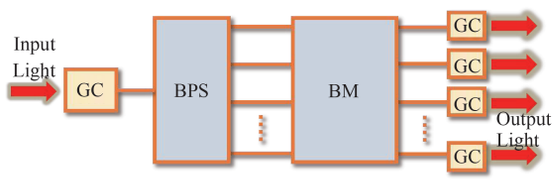

Fig. 1 The sketch of on-chip optics. GC is grating coupler; BPS is beam power splitter and BM is beam modulator including intensity and phase modulator.
图1 片上光学器件示意图。GC为光栅;BPS为光分束器;BM为光调制器,包括强度和相位调制。

1.1 Devices on the chip

1.1.1 Splitters

To achieve applicable structured light, two or more light beams need to interfere with each other. It is crucial to split the light evenly to ensure high fringe contrast and obtain a high quality interference light pattern. A tradition method to split beam is using directional coupler (DC), which is wavelength sensitive and requires high fabrication accuracy. Two other suitable ways to split the beam on-chip are investigated. Fig. 2(a) shows the structure of multi-mode interferometer (MMI) [14] device based on self-imaging, which has a compact structure and large fabrication tolerance. The key structure of MMI device is a waveguide supporting multiple modes. Beam will be separated evenly by carefully designing the position of output waveguides. Fig. 2(b) shows the structure of the adiabatic splitter [15]. Two or more taper waveguides close to each other compose the adiabatic splitter. By properly designing the lengths of waveguides and the widths of gaps between waveguides, the beams can be separated evenly with low-loss. Both of these two methods have large fabrication tolerance, broad bandwidth and low wavelength sensitivity.

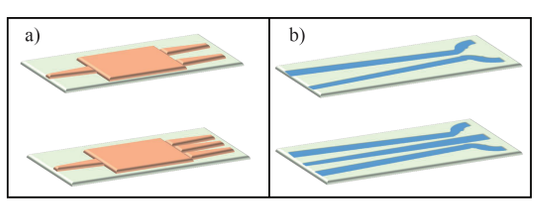

Fig. 2 The Schematic diagram of splitters (a)1*2 and 1*3 MMI and(b) 1*2 and 1*3 ADC
图2 光分束器示意图(a)1*2和1*3多模干涉耦合器,(b) 1*2和1*3绝热分束器

1.1.2 Beam modulators

After splitting the light, the phase and amplitude of each beam need to be modulated. The principle of phase shifters is to control the refractive index in the SOI wave-

guides by means of either electro-optic or thermo-optic effect. By designing the electrodes reasonably and controlling the voltages applied to them, the desired phase can be obtained. The intensities of the beams are modulated using Mach-Zehnder interferometer (MZI) structures with two arms containing phase shifters. The light intensity is determined by the phase difference between beams from two arms. When the output light passes through the way of constructive interference, the intensity of light is maximum; when the light passes through the way of destructive interference, the intensity of light is minimum. The MZI structure with a 1:1 optical splitter can not only control the intensity of the light but also determine the way of light propagation. So it can also be used as an optical switch. The on-chip modulation method allows low transmission loss, low cost, high stability and low power consumption.

1.1.3 Gratings

Since the interference occures above the chip, another key component is the input and output gratings. Due to the difference in effective refractive index, transverse-magnetic (TM) polarized mode cannot be efficiently coupled through the grating couplers. Only transverse-electric (TE) mode is considered in the design. Considering that the light beam is injected from the fiber to the input side of the waveguide through the grating coupler, a Gaussian-like beam which can match the field profile emerging from fiber is wanted. That ensures higher coupling efficiency and lower input loss. The far field beam intensity distribution coupled out from the gratings are expected to be approximate planar light. Taking these factors into consideration, a non-uniform grating coupler is designed. The grating periods, fill factors and etch depths are carefully designed using a formula method. More details can be found in our previous work [16]. Thanks to the broad bandwidth of gratings and ADCs, the 3 dB bandwidth of the designed chip exceeds 60 nm in the test.

1.2 Calculation and simulation of interference patterns

The generation of interference pattern requires at least two inverse gratings. In most cases, a structured light pattern is generated by the light coupled out from two gratings with a direction of 180 degrees or three gratings with a direction of 120 degrees. Taking two opposite gratings as an example, the density of interference fringes is related to the distance between the two gratings and the output coupling angle of the two beams. Ideally, we can model the interference as Young's Double-slit Interference. The interference period can be easily calculated by the equation (1).

$$T = \lambda_0 \frac{d}{L} = \lambda_0 \cot\frac{\alpha}{2} \quad , \quad (1)$$

where λ_0 is the center wavelength of output light, d is the height of the interference plane, L is the distance between two gratings' center, α is the angle between the output beam and the chip surface, as Fig. 3(c) shows.

In practice, the beams coupled out from gratings cannot be regarded as ones ejected from point sources. FDTD simulation is taken to research what the interference pattern looks like. Taking the distance between two gratings 200 μm as an instance, the result shows that the best interference pattern appears at the height of 400 to 500 μm above the chip. Using this simulation, the period of the interference pattern of each height can also be calculated. Fig. 3(d) to 3(f) show the simulation results at different heights. Fig. 3(d) shows the vertical section of two beams interference above the chip. Fig. 3(e) and (f) are the distributions of light intensity at the height of 400 and 500 μm above the chip. The period of interference pattern increases with the distance to the chip.

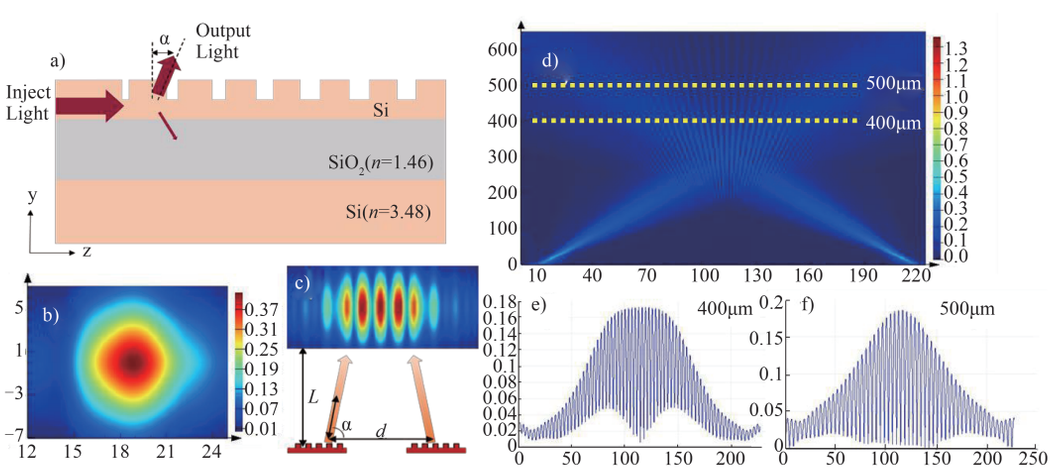

Fig. 3　The FDTD simulation of interference pattern of two beams at the wavelength of 1550 nm. The distance between the two grating is about 200 μm (a) The sketch of GC structure where θ is the output angle, (b) Intensity distribution of beam coupled out from GC, (c) The sketch of interfering process, (d) The distribution of light intensity above the chip, (e) and (f) The distribution of light intensity at the height of 400 and 500 μm upon the chip

图3　两束波长为1550nm的光的干涉图样时域差分有限算法仿真,两光栅距离为200 μm (a)光栅示意图,θ为出射光角度,(b)光栅耦合出射光的强度分布,(c)干涉过程示意图,(d)芯片上方光强度分布图,(e),(f)距离芯片上方高度400及500 μm时光的强度分布图

2 Experimental setup

In the experiment, the integrated chip is fabricated on a standard SOI wafer with a 340 nm top silicon thickness and a 1μm buried oxide layer. Electron beam lithography (EBL) and inductively coupled plasma (ICP) etching are used to define the waveguides and gratings by 210 nm etching depth considering the coupling efficiency of the grating couplers. The waveguide widths are designed to be 400 to 600 nm to transmit fundamental mode beam. The heating metals are Ti and Au with thicknesses of 100 nm and 50 nm. Al foil is used as electrode and square pads are designed to connect external circuit. In order to effectively modulate the intensities and phases of output lights through the opto-thermal effect, long and narrow heating metals are used. According to the design of our chip, the width of heating metal is 10 μm and the length is 1100 to 1500 μm. The fabricated chip is pasted on a Printed Circuit Board(PCB) and the electrical pads are connected with external circuits through gold wires. Therefore, the voltage on the heater can be controlled by modulating the external circuit.

A fiber with a 40° inclined surface is horizontally packaged upon the input grating by UV curing adhesive. The single input design ensures uniformity of light polarization and intensity. A tunable laser (AQ2200-136, Yokogawa) is used as light source in this experiment and the wavelength of 1550 nm is taken into use as a representative. After coupled into the waveguide, the light will be separated and transmit through multiple waveguides. The intensity and phase of each beam will be independently modulated. Finally, the light will be coupled out through particular output gratings and interfere with each other upon the chip. Fig. 4 shows the layout of the chip design and the optic and electronic packages. Fig. 4(a) and (b) are the micrograph and the photograph of the integrated chip sticking on the PCB. It can be seen that two symmetrical layouts are placed in one chip. This design is aimed at space-saving. The electrical pads are linked with pads on PCB through gold wires. The fiber is stuck on the edge of the chip by adhesive. The red rectangle frames highlight the output gratings which are enlarged in Fig. 4(c) and (d).

The imaging system consists of a CCD camera, a lens column, several lenses and groups of multi-axis translation stages. The composed chip is stuck on a micrometer xyz-stage whose height can be controlled precisely by a computer. The microscope is suspended from the chip via a xyz-translation holder. The objective lens used in this experiment is the Mitutoyo 50× lens of with an N. A. of 0.42. Images are acquired using an infrared camera (HAMAMATSU C10633-23 CMOS camera) linking to the column by a C-mount adapter. Fig. 5 shows the stretch and the photograph of the experimental setup.

3 Experiments and results

Fig. 6(a), (b) and Fig. 6(c), (d) are structured light photos of two different switch patterns taking by CCD camera. The period of the interference fringe changes with the height of the image plane. The fringe period of Fig. 5(b) and (d) is about 3.7 μm in the height of 500 μm above the chip. Fig. 5(e) shows three images with the same output gratings but different phase steps. Finally, we can get any phase by changing the voltage of

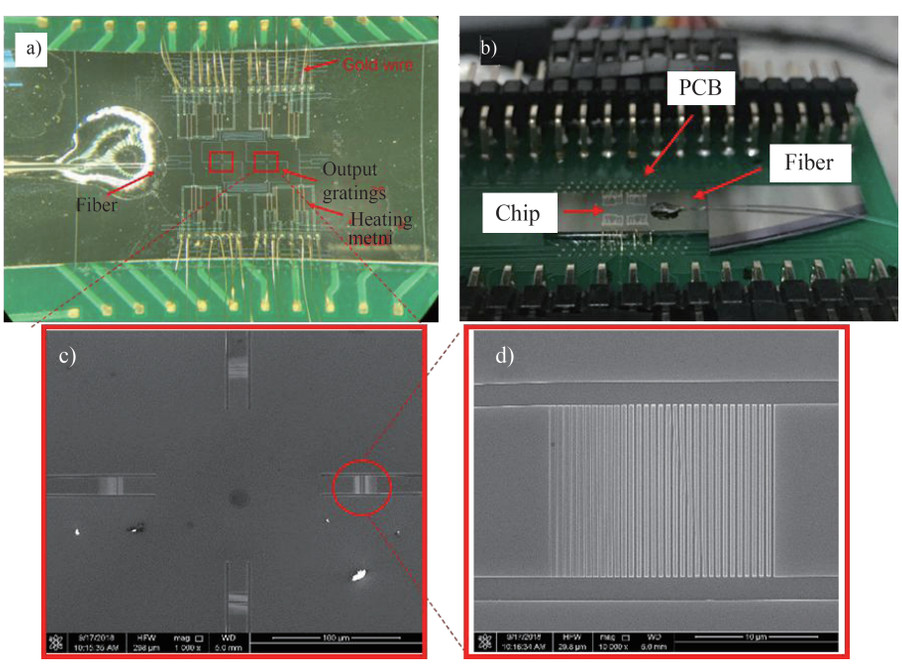

Fig. 4 (a) The microscope photograph of the integrated chip on PCB. Gold wires link the chip circuit and the external circuit, (b) Inclined surface fiber is packaged to the chip using UV adhesives, (c) and (d) Scanning electron microscope (SEM) photographs of the integrated chip

图4 (a)印刷电路板上集成芯片的显微镜照片. 芯片电路与外部电路通过金丝相连,(b)采用紫外固化胶将斜面光纤封装在芯片上,(c),(d)集成芯片的扫描电子显微镜照片

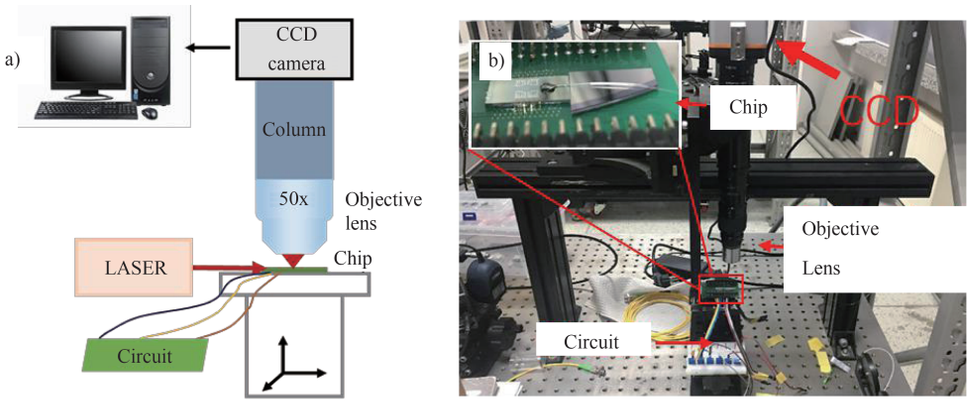

Fig. 5　The experiment setup used for SIM imaging. (a) The stretch of the experiment setup; (b) The experiment setup on the optical platform.
图5　结构光照明扫描显微系统照片。(a)实验装置示意图 (b)光学平台上的实验装置照片

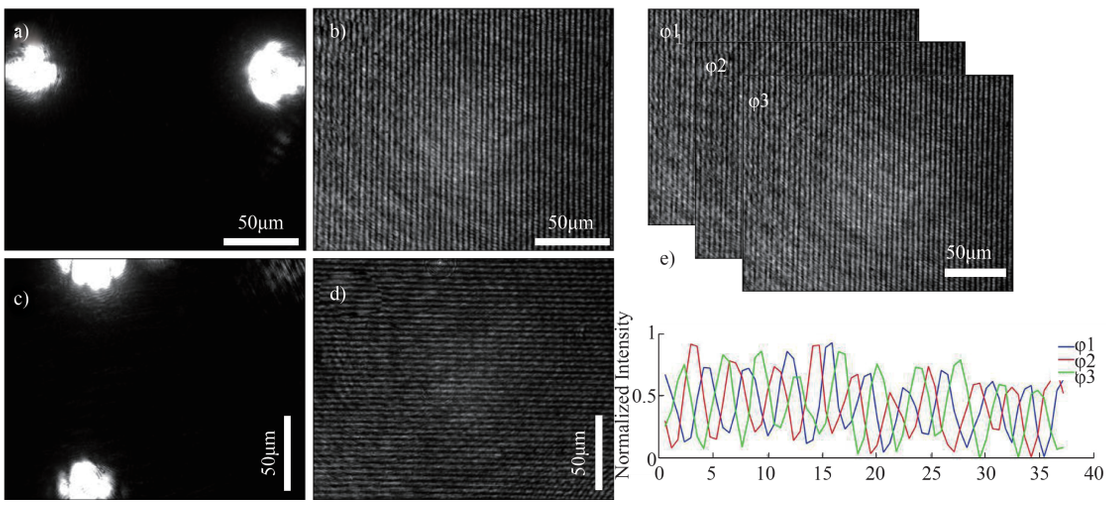

Fig. 6　Photographs from the CCD camera show the interference patterns at different positions. (a) and (c) Beam spot above the chip along two orthogonal directions, (b) and (d) Interference patterns of two orthogonal directions at the height of 500μm above the chip, (e) Three images with same output gratings but different phase steps
图6　不同位置干涉图样的CCD照片(a),(c)两个互相垂直方向的芯片上方的光斑,(b)、(d)两个互相垂直方向的芯片上方500μm高度的干涉图样,(e)三幅同一出射光栅出射的不同相位的干涉图样

metal on phase shifter. Corresponding to the simulation, the interference pattern on 500 μm above the chip has a fringe period of 3.7 μm and the area of interference pattern is about 200×200 μm. This parameter can be modulated by changing the distance between the output gratings, the wavelength of input light and the structure of gratings. Thanks to the convenience of chip designing, we can achieve any pattern of structured light by appropriately designing the layout of waveguides and gratings.

4　Conclusion

In conclusion, a novel compact photonic integrated chip is proposed to generate structured light patterns. This is the first time using only on-chip devices to generate and control infrared structured light. Compared with traditional methods, this method not only is flexible and economical but also has large tolerance of external disturbance and broad bandwidth. Although infrared structured illumination cannot be used in super-resolution imaging, it can be widely applied in 3D shape imaging of biomedical field owing to its absorption character of infrared beam for water. If super-resolution imaging is wanted, other waveguide materials which can transmit visible light such as Si_3N_4 or Ta_2O_5 can be applied in this design. It is also possible to expand utilizations of the on-chip modulation methods in other research by developing new illumination patterns in the future.

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