

半导体集成电路制造中的准分子激光退火研究进展

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摘要: 随着半导体集成电路芯片的尺寸越来越小、结构越来越复杂, 芯片制造过程中的退火工艺技术也在不断进步。激光退火以其在芯片制造过程中热预算控制的优势, 在芯片制造退火工艺中的重要性正在显现。而准分子激光的特点是波长短、峰值功率高、作用于大多数物质表面时能量迅速被物质表面吸收。准分子激光退火可以实现对材料表面温度梯度的控制, 是半导体集成电路制造中热处理工艺的重要选择。对半导体集成电路制造过程中准分子激光退火研究进展进行了综述。概述了集成电路制造中退火工艺热预算控制与激光退火的理论模拟研究结果; 着重介绍了准分子激光退火在离子掺杂控制、超浅结形成、沟道外延等材料处理中的研究进展, 以及在金属层制备和 3D 器件中的应用。研究表明, 准分子激光退火工艺有望为三维半导体集成电路制造提供新的解决方案。

关键词: 半导体制造工艺; 热预算; 激光退火; 准分子激光

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0 引言

随着集成电路制造按摩尔定律发展, 半导体器件的制备工艺不断进步, 单位面积上的晶体管数量越来越多, 芯片中器件的体积越来越小, 芯片的制作难度和复杂程度也随之提升, 因此半导体集成电路制造的退火工艺技术也在不断改进。

以金属氧化物半导体场效应晶体管 (MOSFET) 为例, 其源漏区域的离子掺杂是通过离子注入将杂质原子加速形成高能离子束轰击待改性材料表面。在离子注入的过程中, 激烈的碰撞使得被注入材料的晶格遭到破坏, 出现大量晶格缺陷, 而且随着离子注入剂量增多, 晶格损伤也会越大, 过多的晶格缺陷会导致器件的性能下降。为了获得更高性能的器件, 通常会使用退火工艺消除缺陷并对杂质进行激活^[1-7]。但是, 随着器件尺寸不断缩小, 传统的炉式退火等退火技术已经不能适应芯片制造工艺的要求, 退火技术和

工艺参数需要不断改进以适应器件尺寸变小带来的技术挑战, 这为激光退火进入半导体集成电路制造提供了机会。

脉冲激光退火可以在极短的时间内对材料的特定区域进行照射, 被照射的特定区域材料表面吸收激光的能量之后, 温度上升融化, 并在随后的降温过程中自然地在融化层液相外延生长出晶体薄膜, 这个过程能够重构融化层的晶体结构, 同时掺杂也会重新分布溶解于晶体中, 达到消除缺陷激活掺杂的目的^[8-16]。目前已有多种脉冲激光用于半导体工艺中,

纳秒脉冲激光热退火在 20 世纪后期成功引入半导体器件制造, 用于大批量制造敏感的 3D 架构器件, 如垂直硅基绝缘栅双极晶体管、基于 SiC 基的垂直功率二极管和背面照明互补金属氧化物半导体 (CMOS) 成像传感器。目前正在被集成到下一代 CMOS 和存储器制造的关键退火工艺中^[17-29]。

半导体制造领域的激光加工和脉冲激光退火的

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很多研究采用了不同种类的固体激光^[30-37]。总体来说,脉宽越短的脉冲激光越有利于控制热预算,因此,近年来国内外对皮秒、飞秒的超短脉冲固体激光对半导体材料相互作用的研究较多。就激光波长而言,波长短有利于更精确地控制退火范围和效果,但是目前的固体激光波长大多数在红外和可见区域。

准分子激光作为纳秒脉冲的紫外激光,波长短、脉宽较窄,对材料的穿透深度较小,尤其是硅等半导体材料对准分子激光的吸收率较高。此外,聚焦或投影时分辨率高、单脉冲能量大等特点,便于根据应用场景的不同,以部分脉冲能量作为代价对脉冲光斑能量分布进行整形处理。以上特点使得准分子激光在半导体制造的退火技术上具有一定的优势^[38]。文中主要调研分析了准分子激光退火应用于半导体集成

电路制造的研究进展。

1 退火的热预算控制与激光退火理论模拟研究结果

图 1 所示为采取不同退火技术的热预算演化图。不同技术的对比点在于退火的时间窗口与相应的退火峰值温度,更好地控制这两个目标能够更加精确地控制热预算,最终实现材料性能的改善。从炉内退火到单片晶圆快速退火工艺 (RTP) 和尖峰退火,通过缩短热退火时间窗口来控制退火效果,尤其是实现从材料表面到材料内部温度梯度的控制,本身就具有一系列的挑战。如今亚微秒激光退火研究取得了一系列研究结果^[39-40]。

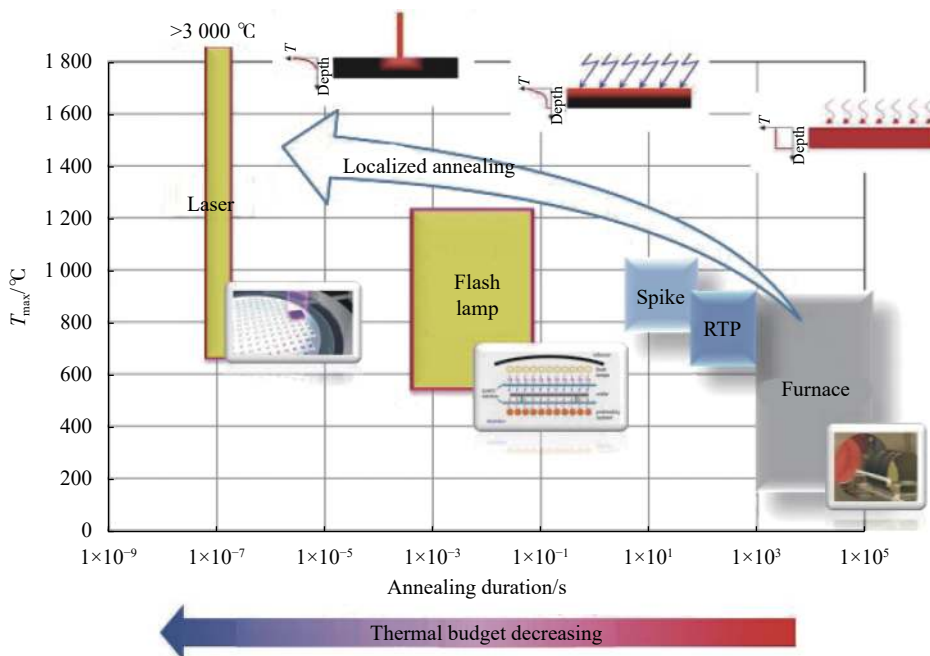


图 1 热预算演化示意图^[41]

Fig.1 Schematic diagram about thermal budget evolution^[41]

在基于降低热预算的激光退火研究上, K. Huet^[41]等人从纳秒激光退火的模拟、激光退火在 CMOS 接触模块的应用、激光退火在先进互联上的应用和激光退火在 3D 结构上的应用做了比较详细的总结和分析。

在纳米激光退火的模拟方面, K. Huet 等人整理了部分有关激光对硅锗材料进行退火处理模拟的研究结果,指出精确的数值模拟是推动突破性工艺应用的关键。在此基础上, K. Huet 等人宣称开发了专门

对一维、二维和三维结构激光退火进行模拟的计算工具^[42],该工具能够对仿真结构和设备参数进行设置,对参数批量处理和跟踪以及自动生成报告,可用于估计给定目标在制造流程中的最佳激光退火工艺插入点,并评估工艺参数(如激光能量密度、脉冲持续时间、辅助加热温度)和结构特征(如形状、堆叠、材料、掺杂浓度)对退火动力学的影响。

针对激光退火在改善 CMOS 接触模块 (contact

module) 特性方面的应用已有很多研究成果,如激光退火在层结构^[43-47]、图案结构^[48-50]、FinFet 结构^[51]、以及纳米线结构^[52-55]等器件的应用。K. Huet 等人对这些研究的分析总结表明,尽管这四种结构从简单到复杂,但在逻辑上研究方法十分类似,其最终目的都是为了了解激光与材料不同结构的相互作用,最终在器件上得到应用,优化工艺,完成更复杂的集成,获得更高性能的器件。

上述研究主要针对接触电阻,希望通过优化参数达到降低电阻的目的,研究结果也证实了激光退火能够达到降低电阻的目的。

图 2 所示为不同能量密度激光对 Ge 层结构 Ge 薄膜退火的 SIMS 图。在部分熔化和全熔化剖面中,Ge 界面仍然存在,但 Ge 在熔层内重新分布,在近表面处浓度较高,在最大熔体深度附近有一些损耗,这是典型的偏析现象^[43],在图案结构中也被证明。

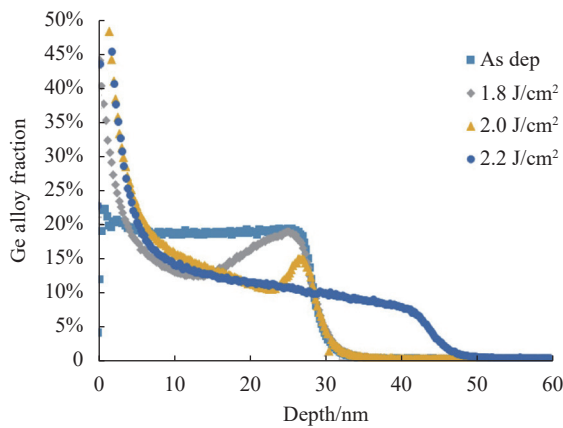


图 2 不同能量密度激光对 Ge 退火的 SIMS 图^[41]

Fig.2 SIMS diagram about laser annealing Ge SIMS diagram in different energy densities^[41]

图 3 对比了非激光退火和激光退火情况之间的接触电阻率变化,清楚地表明了激光退火方法的内在优势及其对 finFET 器件的适用性^[51]。

纳米线结构器件的研究结果表明,激光退火后亚熔化条件下高温区位于表面附近,在更深的区域,由于下面的 Ge 外延层具有很高的导热性,温度下降得非常快(图 4)。这是由于激光退火的吸收效率非常高,大部分发生在表面区域层,只有一小部分被栅和沟道吸收,在退火过程中,该区域产生的热量可以扩散到有价值的的掺杂剂活化区域^[54-55]。

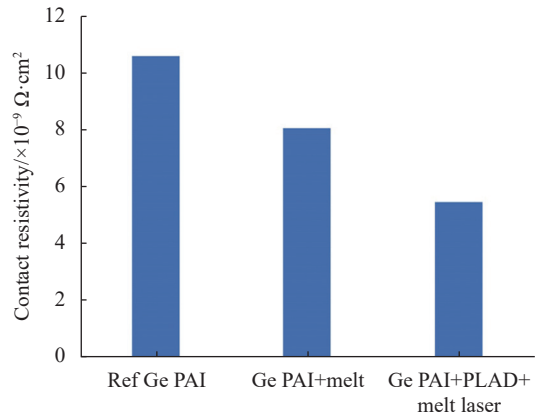


图 3 P 型 FinFET 接触电阻率与激光退火^[41]

Fig.3 Contact resistivity of P FinFET with laser annealing^[41]

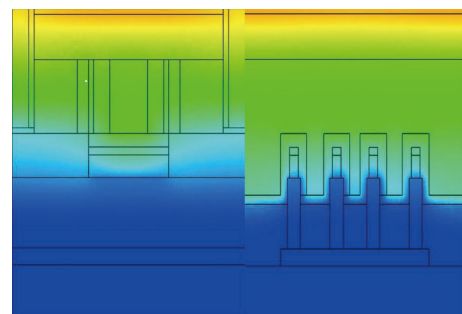


图 4 纳米线结构器件激光退火截面模拟^[41]

Fig.4 Laser annealing cross section simulation of nanowire-structured devices^[41]

激光退火在先进互联的应用上,接触孔和导电路径尺寸缩小以及互联密度不断增长是目前后道工序需亟待解决的问题,而其中对高效低热预算的材料进行改进是解决该问题的关键^[56]。对 14 nm FinFET 中所使用的熔体激光退火工艺流程研究结果见图 5。

在器件尺寸不断变小的条件下,不论是前道工序(front-end-of-line; FEOL)器件的微缩,还是后道工序(back-end-of-line; BEOL)中接触点和连线的工艺改进都面临技术挑战。激光退火在 3D 结构器件的研究方面,其主要研究成果集中在三维顺序集成的多晶硅晶化和存储器多晶硅插头形成方面。图 6 描述了 3D 顺序集成与其面临的问题。

三维顺序集成主要挑战的是在顶层实现高性能晶体管,同时不降低底层晶体管的电气性能,并将后道工序夹层的热预算保持在 500 °C 以下^[57]。在过去几年的研究中,激光退火对 3D 顺序集成的兼容性通过仿真和真实结构得到了验证^[58]。在原位掺杂非晶

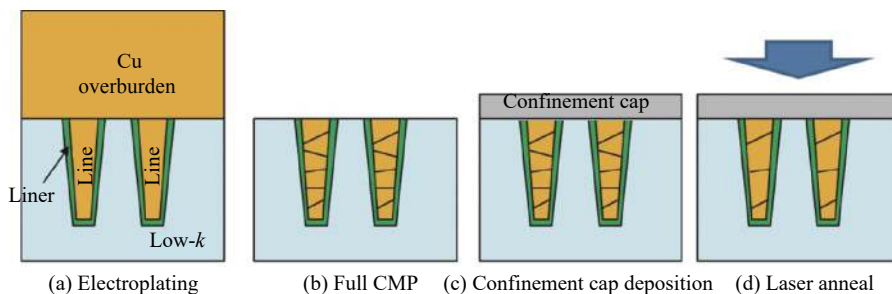


图 5 14 nm FinFET 中基于激光退火的金属互联工艺示意图^[41]

Fig.5 Process flow for M1 interconnects with melt laser anneal in 14 nm Finfet device^[41]

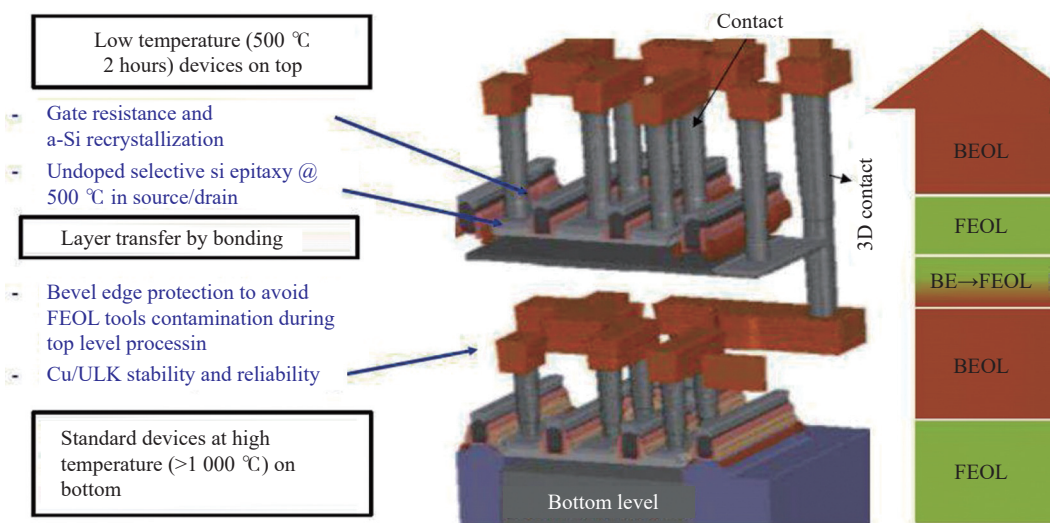


图 6 3D 顺序集成与相关问题归纳图^[41]

Fig.6 3D sequential integration related problem induction diagram^[41]

层中结晶并使用激光退火激活掺杂剂能够获得高活化率和大晶粒的充分再结晶,且不影响后道工序^[59]。此外,通过化学-机械整平解决结晶后,局部晶界引起的表面粗糙度问题是成功集成激光退火工艺的关键^[60]。

在存储器领域,3D NAND 通道形成的情况下,由于晶粒尺寸增加和界面缺陷固化,可以观察到存储性能的明显改善。然而随着 DRAM 阵列晶体管尺寸的不断缩小,接触区域的多晶硅沉积填充可能会出现一些空隙或接缝,这可能会影响接触电阻率,从而影响 DRAM 操作的整体性能。而研究结果证实激光诱导多晶硅熔解回流是一种有效解决该方法^[61-64]。

2 准分子激光退火在离子掺杂、外延层生长等工艺中的应用

自摩尔定律被提出以来,电路的集成度能够飞速

提升的一个重要原因是使用的金属氧化物半导体场效应晶体管 (MOSFET) 依照按比例缩小理论不断缩小。但事实上,按比例缩小的技术偏离了理想恒定电场规则,当 MOSFET 器件缩小到一定程度时,晶体管就遇上了短沟道效应阻碍。为了能够突破按比例缩小理论恒定电场的基本限制,人们引入了另一个方案:恒定电压下的按比例缩小。这需要器件缩小时增加掺杂浓度,使得在电压保持不变的前提下增强电场,这又导致强电场击穿器件的可能性增大,同时加剧了短沟道效应。现在人们使用的按比例缩小技术采用了恒定电场和恒定电压相结合的方式,为了防止击穿和短沟道效应,必须严格控制掺杂的横向和纵向扩散。激光退火是一个重要选择。

与传统的快速热退火相比,脉冲激光退火可以在 Si 中形成超浅结。在足够的能量密度下,脉冲激光退火会导致 Si 样品中一个明确区域的熔化,掺杂原子

均匀地重新分布,且照射后快速凝固过程中发生的非平衡偏析增强了掺杂原子的俘获,有利于高密度掺杂。

La Magna^[65]等采用相场法模拟了准分子激光退火 (ELA excimer laser annealing) 过程中的热场和掺杂浓度的演化过程。

La Magna 进行了 50 nm 的 a-Si 层和 3 nm 的 SiO₂ 层堆栈于 c-Si 衬底经受单次 ELA 脉冲退火的模拟,设置初始温度为 450 °C 的均匀热场,激光参数为波

长 308 nm, 脉冲持续时间 28 ns。图 7 所示为熔化和凝固阶段的模拟结果,图 8 所示为密度场演化图。在熔化过程中,相边界在 a-Si 区域比在 c-Si 区域移动得更快。由于两种材料的热性质的变化,相边界在到达 a-Si 和 c-Si 边界时速度降低。凝固阶段的特征是除在 SiO₂/Si 界面处和最大熔体深度,其他位置边界速度几乎恒定,且杂质只在液相中扩散,在固相中扩散率很低。

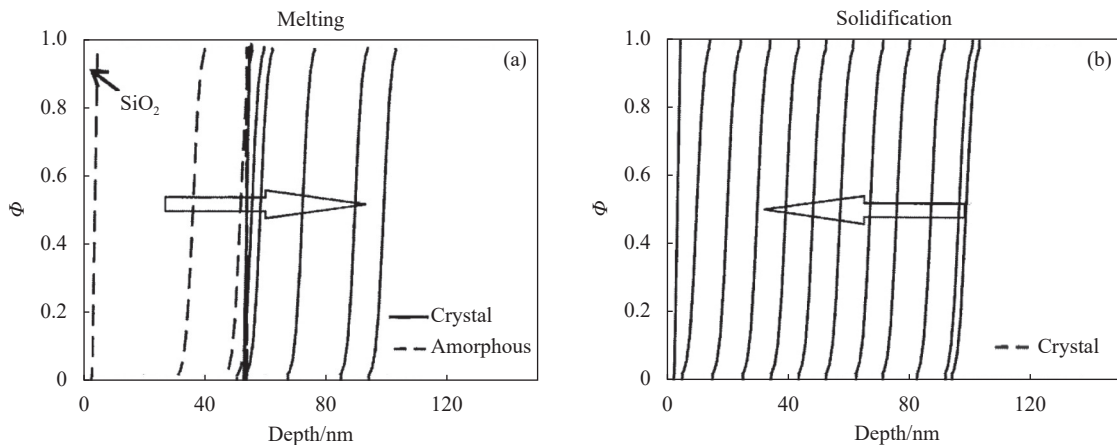


图 7 在 0.717 J/cm² 单次脉冲 ELA 过程中的相场演化,两个相场剖面之间的时间间隔为 5 ns^[65]

Fig.7 Phase field evolution of single pulse ELA process at 0.717 J/cm², the time interval between the two phase field profiles is 5 ns^[65]

La Magna 等人还注意到,模拟中只有前几个脉冲的化学剖面有显著差异。因此,他们对表面处理时所需的照射次数进行预测,认为只需要几个合适能量密度的脉冲就足以达到最佳激活效果。在之后的实验中,对两个和五个脉冲照射的样品的扩散电阻分布测量结果显示,在对应条件下可以获得很高的掺杂激活

效率,证实了模拟预测的有效性。同时,La Magna 等人还将模拟剖面与实验 SIMS 剖面进行了对比,如图 9 所示。这样的比较表明其实验和模拟之间有可靠的一致性。

Fortunato G^[66]等建立了一个考虑熔体深度、熔体时间和界面速度的模型来解释在激光脉冲下掺杂在熔化和再生长过程中的行为。其所设置的激光脉冲波长为 308 nm,并假设每次脉冲后达到的熔体深度可以呈高斯分布,在平均值附近随机变化。模拟结果表明,在低于热力学极限的条件下,通过准分子激光退火后,Si 中形成的掺杂分布是激光退火过程的固有性质,受扩散方程和熔体深度的控制,且只有在一定能量剂量范围内,扩散机制才会出现内在剂量依赖性。同时,对于低于热力学极限的原子浓度水平,Fortunato G 等还证明了实验数据可以可靠地与模型相拟合。图 10 为当衬底温度为 450 °C 时,激光照射在 Si 中形成的熔体深度随激光能量密度变化的函数模拟图。

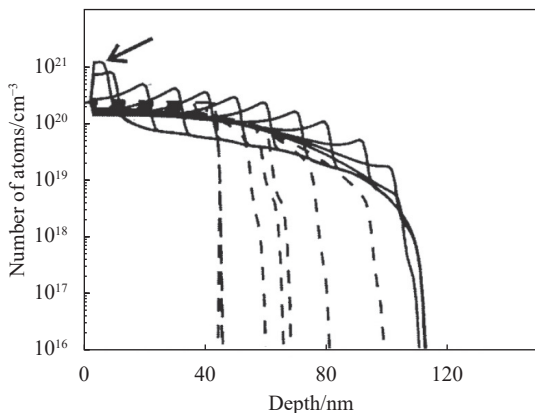


图 8 在 0.717 J/cm² 单次脉冲 ELA 过程中的密度场演化图^[65]

Fig.8 Density field evolution during a single pulse ELA at 0.717 J/cm²^[65]

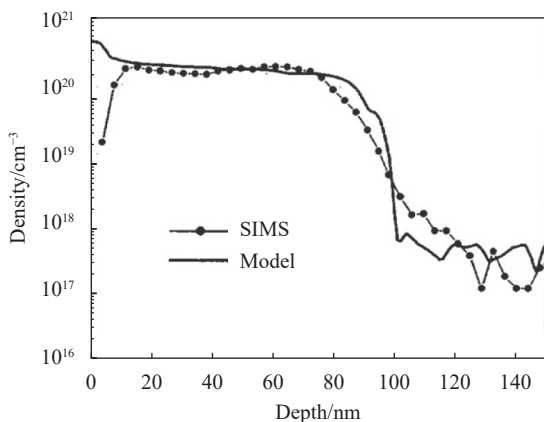


图 9 10 个脉冲后注入 As 的表面模拟曲线和 SIMS 曲线^[65]

Fig.9 Surface simulation curve and SIMS curve of As after ten pulses^[65]

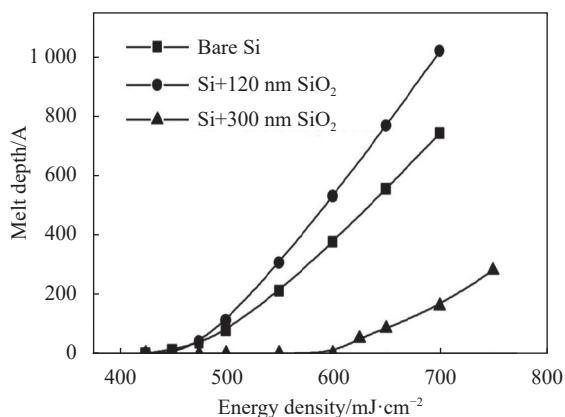


图 10 衬底温度为 450 °C 时, Si 熔体深度随激光能量密度变化的模拟图^[66]

Fig.10 Simulation diagram of Si melt depth varying with laser energy density at substrate temperature of 450 °C^[66]

因为硼离子会在退火时产生沟道效应和瞬时增强扩散,所以硼离子注入的 p+n 超浅结更难形成。Chong Y F^[67] 等通过实验表明,利用 248 nm 的准分子激光可以获得硼掺杂的超浅结。在预非晶化注入的方案下对比准分子激光退火和尖峰退火如图 11 所示,248 nm 的准分子激光退火后的样品结深达到 37 nm,相比尖峰退火的样品结深少至少 20 nm。Chong Y F 等对此的解释为预非晶化层可以在不熔化底层 Si 的情况下被熔化,当光子在 Si 衬底的顶表面区域被吸收后,在不到 1 ns 的时间内,光子的能量被转移到晶格中时,熔解就发生了。由于硼在液相中的扩散率比在固态中的扩散率高约八个数量级,硼原子在熔体深度内几乎均匀地重新分布,从而形成一个突变结。为了说明准分子激光退火对硼扩散深度具有一定控制能力,Chong Y F 等还对比了不同脉冲数的扩散深度,如图 12 所示。

Seung-Woo Do^[68] 等使用重复频率为 50 Hz、照射时间为 20 ms、能量密度为 400~500 mJ/cm² 的 ArF (193 nm) 准分子激光对磷离子注入的超浅结 CMOS 器件进行了激光退火研究。如图 13 所示,当准分子激光能量密度低于 440 mJ/cm² 时形成的结深几乎相同。将激光能量密度提高到 500 mJ/cm²,将结深提高到 40 nm,此时能量的提高并没有使结发生显著的变化。当激光能量密度设置为 460 mJ/cm² 时,可以获得 30 nm 的浅结。

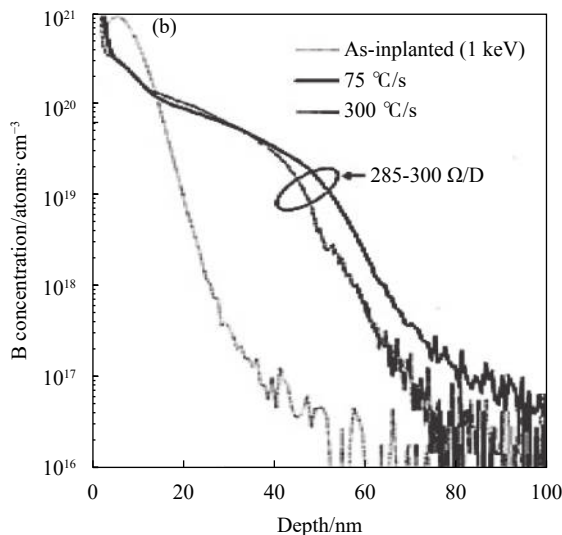
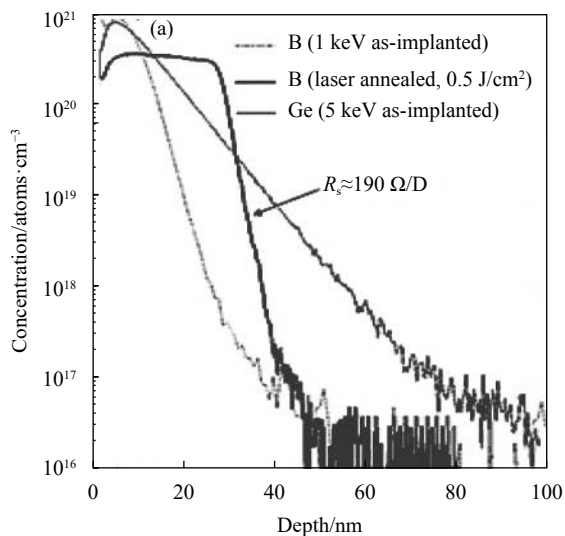


图 11 (a) 尖峰退火和 (b) 准分子激光退火的 SIMS 图^[67]

Fig.11 SIMS diagram of (a) spike annealing and (b) excimer laser annealing^[67]

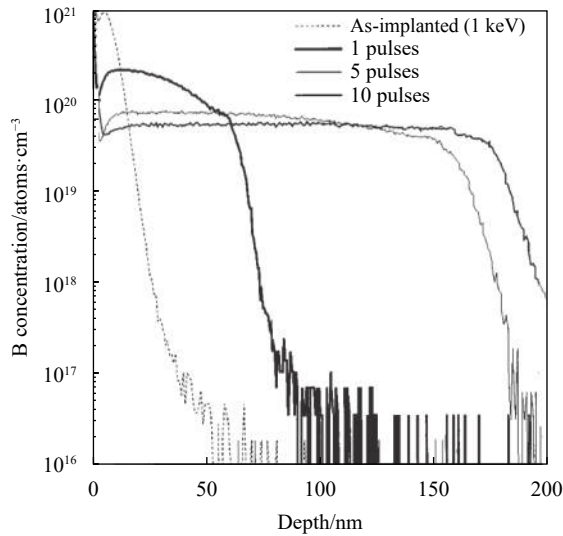


图 12 不同脉冲数对结深影响^[67]

Fig.12 Effect of different pulse number on junction depth^[67]

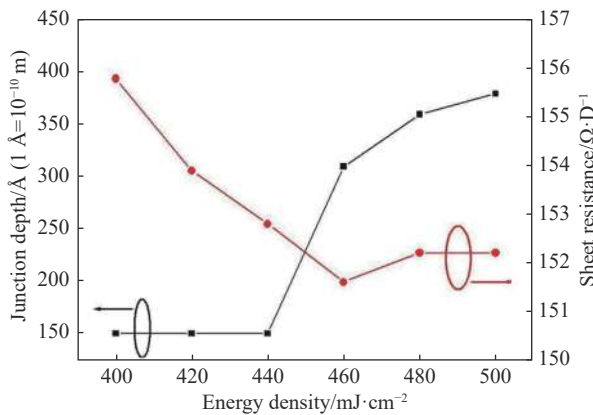


图 13 薄片电阻和结深随激光能量密度的变化规律^[68]

Fig.13 Variation of sheet resistance and junction depth with laser energy density^[68]

如图 14 所示, 通过比较双晶 X 射线衍射 (DXRD) 曲线, 经过准分子激光处理的样品具有更尖锐的峰, 说明经过准分子激光处理的掺杂样品缺陷比仅掺杂未经过准分子激光处理的样品更少。

Aid S R^[69] 等使用 KrF 准分子激光对磷掺杂的 Ge 衬底 MOS 器件进行了激光退火研究, 当衬底在 500~1 000 mJ/cm² 之间退火时, 可获得较低的电阻。他们通过电阻值估计掺杂激活, 通过测定拉曼光谱峰拉曼光谱分析了损伤注入层的再结晶情况, 证明所有退火点都发生了再结晶。图 15 为退火样品的拉曼光谱 c-Ge : a-Ge 比值图。根据 c-Ge 和 a-Ge 的比值, 分析出在高能注入下较低的激光能量密度和脉冲数不

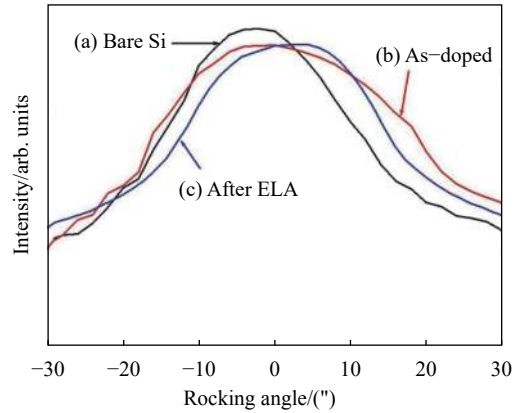


图 14 DXRD 曲线图^[68]

Fig.14 DXRD curve graph^[68]

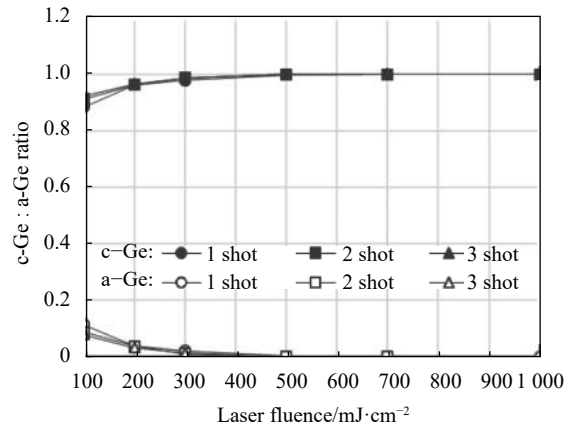


图 15 拉曼光谱 c-Ge : a-Ge 比值图^[69]

Fig.15 Raman spectrum c-Ge : a-Ge ratio chart^[69]

能使注入样品完全再结晶, 说明低能量激光热退火不能完全修复离子注入造成的损伤。当样品在大于 500 mJ/cm² 的激光能量密度下退火时, 100% 的 c-Ge 拉曼比证实了完全再结晶。由于不同脉冲次数对表面形貌的影响无显著性差异, 为了保持重叠退火区域的均匀性, 最终他们确定能量密度 700 mJ/cm², 二次脉冲作为最佳参数。

Toshiyuki Tabata^[70] 等使用 XeCl 准分子激光对铈掺杂的硅衬底 MOS 器件进行了激光退火研究。图 16 为铈原子在准分子激光退火前后的 SIMS 曲线图。当注入铈的硅外延层受到激光照射发生熔融时, 铈原子发生像表面强烈偏析。当增加激光能量密度, 这种表面偏析会增强, 非平衡偏析系数随着辐照激光能量密度的改变有很大变化。此外, 当 Si 外延层几乎完全熔融时, 激光退火后活性掺杂水平会显著提高, 约为平衡固溶极限的 2~4 倍。

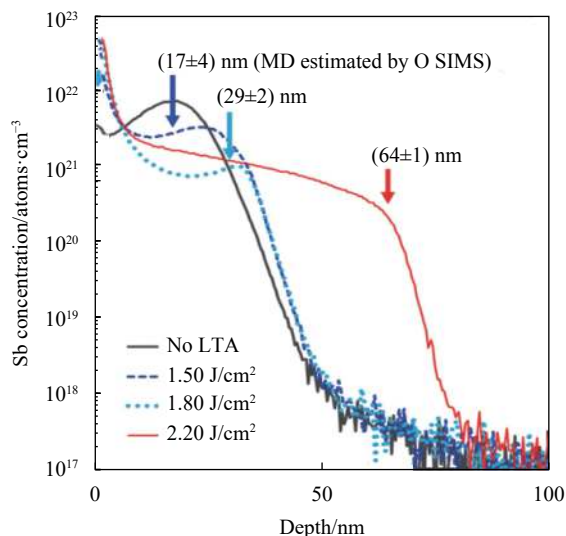


图 16 锑在准分子激光退火前后的 SIMS 曲线图^[70]

Fig.16 SIMS curves of Sb before and after excimer laser annealing^[70]

为了制备出性能更好的器件,应变硅技术和绝缘体上硅技术 (silicon on insulator, SOI) 也被引入到制程当中。应变硅技术是指通过使应变材料产生引向器件沟道的应力,改变沟道中材料导带或价带的能带结构,来增强载流子迁移率和提高器件速度的技术。SOI 在硅晶体管之间利用嵌入或键和的方法形成埋层氧化物隔离顶层硅薄膜层和硅衬底,来降低寄生电容。SOI 材料相比体硅具有许多优点,如:隔离集成电路中的元器件,减小集成电路中的寄生电容,消除 CMOS 电路中的寄生门锁效应。在处理高性能顶层

晶体管的同时需要保持底层晶体管的性能。

2002 年, Seong-Dong Kim^[71] 等利用非晶态硅层的熔化温度比晶态硅层低约 300 °C 的条件,结合激光退火和预非晶注入工艺,降低激光器对器件的能量通量,在亚 100 nm SOI CMOS 的工艺集成上实现了理想的盒形 (BOX) 超浅结,其中使用参数为脉冲宽度 20 ns、波长 308 nm 的 XeCl 激光器, SIMS 测量激光退火和预非晶注入工艺处理过的器件中硼和砷掺杂曲线如图 17 所示。Seong-Dong Kim 等推断,在非晶硅层开始熔解时存在一个激光能量阈值,低能量单脉冲不足以完全熔化非晶硅层或使掺杂剂充分扩散。与单发高能激光相比,多发辐照增加的激光能量可以在非晶硅层上积累更有效的热能,使熔解深度达到非晶硅/晶硅的初始界面,直到非晶层温度接近晶硅层熔点。之后的实验也证明,激光退火和预非晶注入工艺结合也有利于器件薄层电阻的降低。此外,额外的快速热退火处理有助于减少激光照射后再结晶层的位错。

Seong-Dong Kim 等又用热传输模型模拟了 SOI 器件和体硅器件在激光辐照后的热分布,如图 18 所示。SOI 器件上的源极或漏极区域的温度分布与栅极区域的温度分布几乎相同,而体硅器件上的源极或漏极区域的温度分布明显低于栅极区域。对于体硅器件,需要相对较高的激光能量来激活体基板中的杂质,这可能会导致集成问题,相比较而言,极低的激光

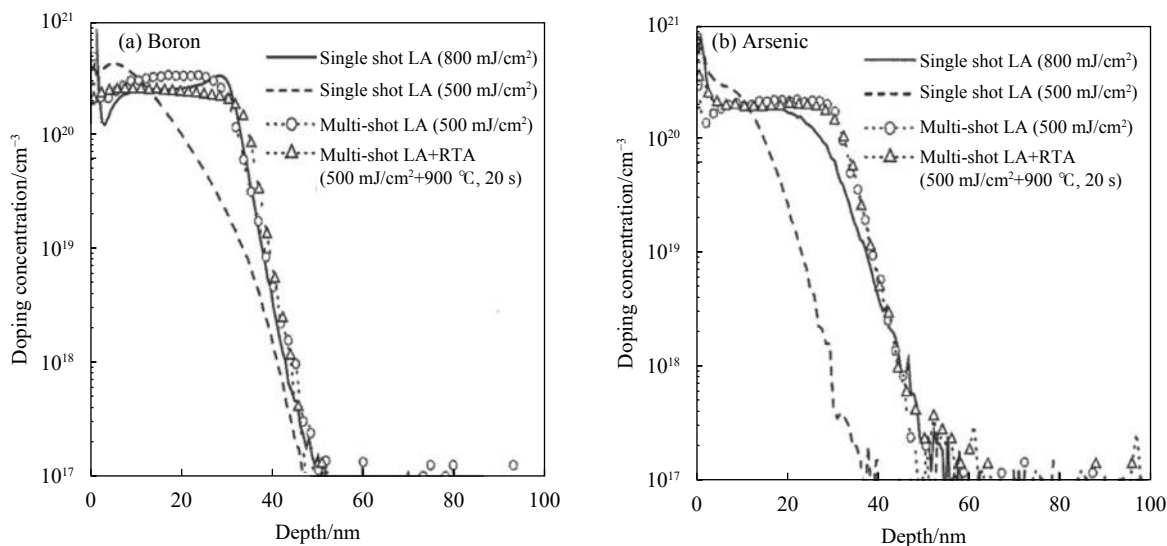


图 17 (a) 硼和 (b) 砷的 SIMS 图^[71]

Fig.17 SIMS diagram of (a) boron and (b) arsenic^[71]

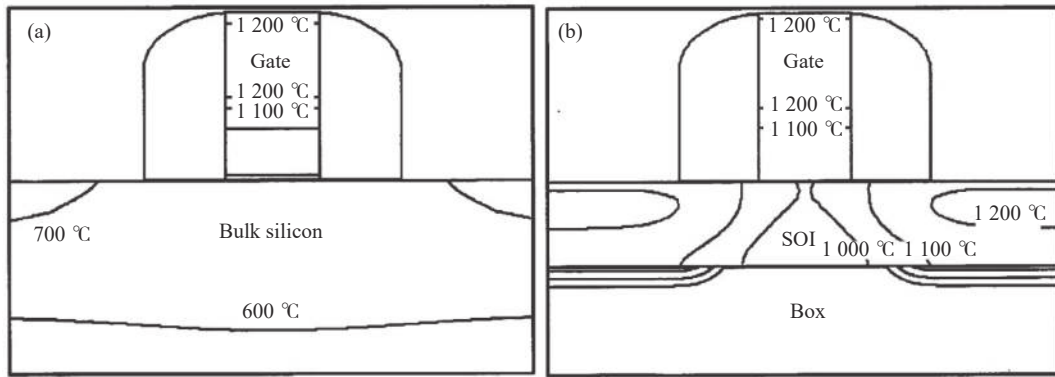


图 18 波长 308 nm 激光照射 (a) 体硅器件和 (b) SOI 器件 65 ns 后的热分布^[71]

Fig.18 Heat distribution after 65 ns 308 nm laser irradiation (a) bulk silicon devices and (b) SOI devices^[71]

能量足以激活 SOI 器件中的杂质, 激活所需的激光能量降低了四分之一, 扩大了工艺窗口裕度。

Chery N^[72] 等使用 308 nm 的准分子激光对磷注入的 SOI 器件进行了纳秒准分子激光退火研究。他们研究了通过增加激光能量密度到接近完全熔化阈值对掺杂剂激活影响, 激光能量密度的增加对于低剂量注入样品几乎没有影响, 其激活率始终接近 100%; 但是对于高剂量注入的样品, 却观察到不同的现象。如图 19 所示, 材料在注入剂量为 $7 \times 10^{15} \text{ cm}^{-2}$, 激光能量密度为 0.15 J/cm^2 和 0.10 J/cm^2 的退火条件下 (未达到完全融化阈值), 霍尔剂量 (表示被激活掺杂剂量) 表现为一个相对恒定的值。相比较而言, 在 0.05 J/cm^2 退火条件下, 霍尔剂量约 $4.3 \times 10^{15} \text{ cm}^{-2}$, 增加了约 20%, 这种霍尔剂量的增加伴随着少量霍尔迁移率 (体现载流子的迁移率) 的减少。此外, 最大激活浓度也随着激光能量密度的增加而增加。这些发现表明, 热预算

的提升与激光能量密度提升所导致的表面堆积峰值中含磷相关的非活性团簇的溶解有关。

在 pMOS 中, SiGe 与 Si 相比具有更高的空穴迁移率, 10 nm 和更高的 CMOS 制程需要局部的高迁移率 Ge 和 SiGe 应变材料^[73]。然而由于 Si 和 Ge 之间存在晶格不匹配, 高浓度的 Ge 很可能引起 SiGe 层应变弛豫和位错。为了减少失配位错的成核与扩散, 一种通过控制外延生长的方法制备 SiGe 源/漏的方法被提出。传统的热退火会导致外延生长的高 Ge 浓度 SiGe 层产生应变迟豫^[74], 因此激光退火技术被引入到该制程中, 研究人员注意到准分子激光穿透深度浅的特点, 使用准分子激光器对外延生长的 SiGe 沟道材料进行了实验。

C. Y. Ong^[74] 等使用不同能量密度的准分子激光对沟道材料进行外延, 证明了使用准分子激光可在近表面获得较浅的 $\text{Si}_{1-y}\text{Ge}_y$ 梯度层。图 20(a)~(d) 分别

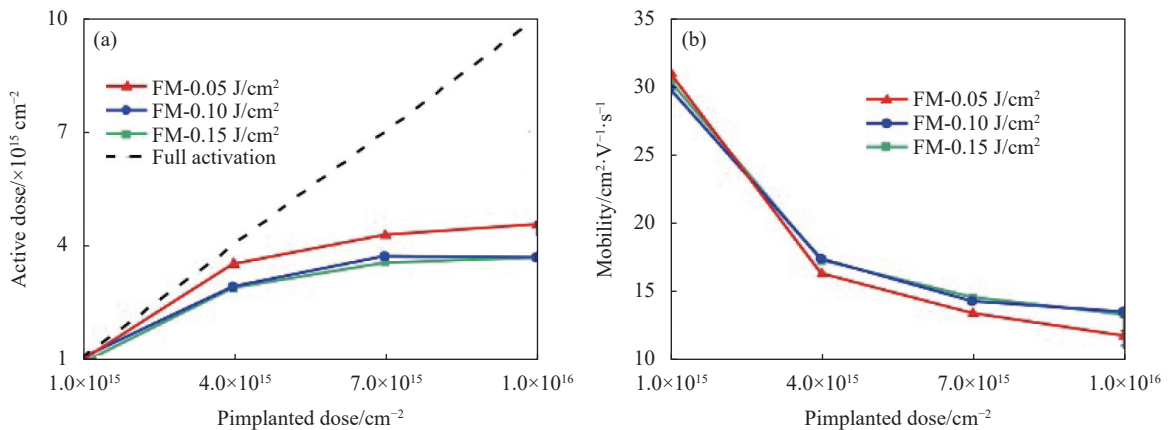


图 19 激光能量密度接近完全熔化阈值对影响掺杂剂激活的影响^[72]

Fig.19 The effect of laser energy density approaching the full melting threshold on the activation of dopants^[72]

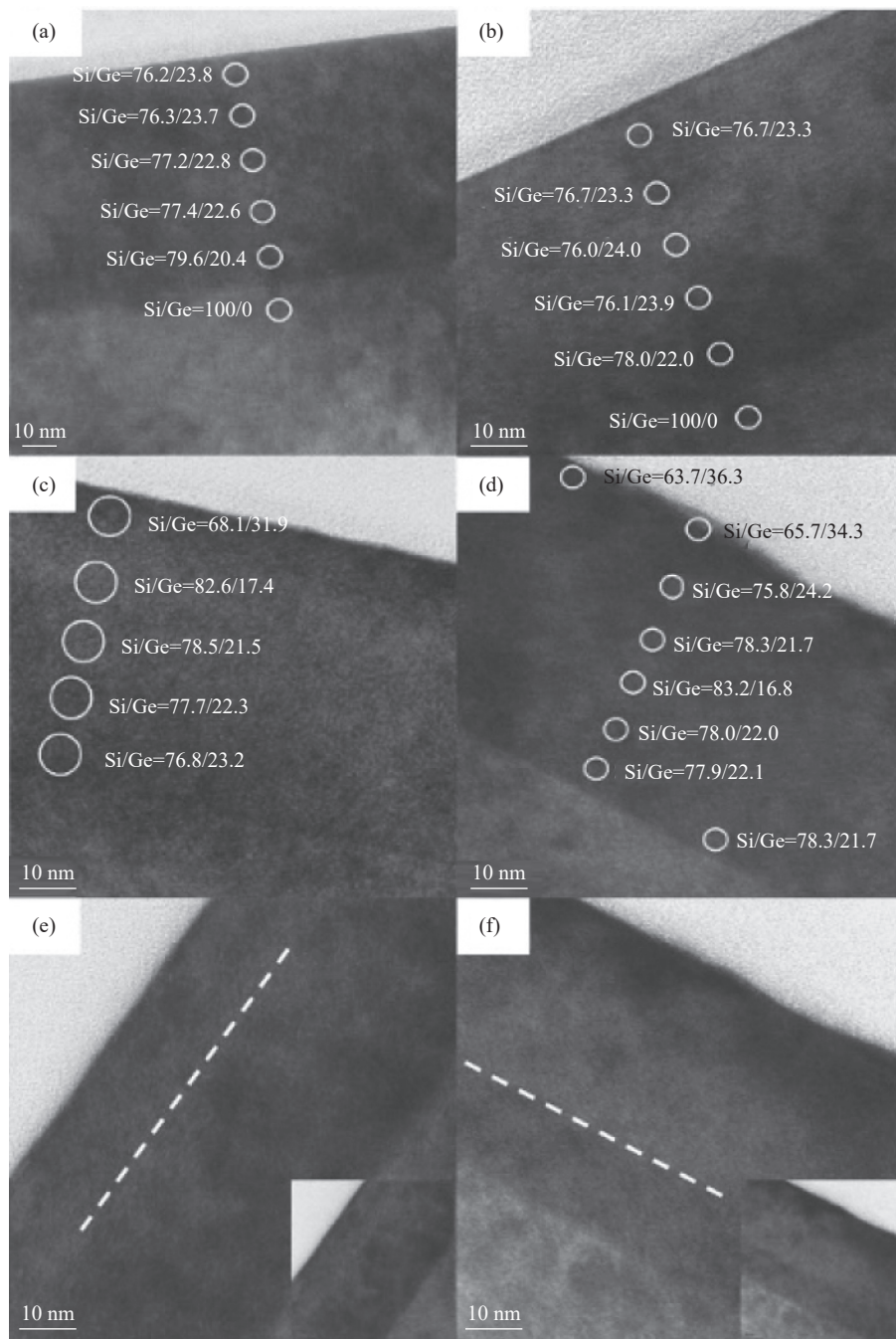


图 20 不同能量密度准分子激光处理后的材料 TEM 图^[74]

Fig.20 TEM images of materials treated by excimer laser with different energy densities^[74]

为生长时、 0.3 J/cm^2 、 0.5 J/cm^2 和 0.7 J/cm^2 激光热退火 (laser thermal annealing, LTA) 后 Ge 和 Si 的浓度。经过 0.5 J/cm^2 和 0.7 J/cm^2 准分子激光退火后的样品的透射电子显微镜照片显示, 样品中有两个不同的层 (图 20(e)、(f))。在 0.5 J/cm^2 的 LTA 条件下, 形成了 15 nm 的 $\text{Si}_{1-y}\text{Ge}_y$ 梯度层, 表面处 Ge 浓度最高, 为 32%。当激光通量增加到 0.7 J/cm^2 时, $\text{Si}_{1-y}\text{Ge}_y$ 梯度层

增加到 30 nm 。

L. Dagault^[75] 等对 Si 上的 SiGe 外延层进行了准分子纳秒激光退火研究, 如图 21 所示, 可以看出, 在激光退火过程中, 表面反射率首先受到温度升高的调制, 然后由于固-液相的变化而大幅度增加。固化后, 反射率下降到接近初始值。图 22 为部分熔融状态下样品的显微图以及 Ge 剖面 and 面内应变剖面。在

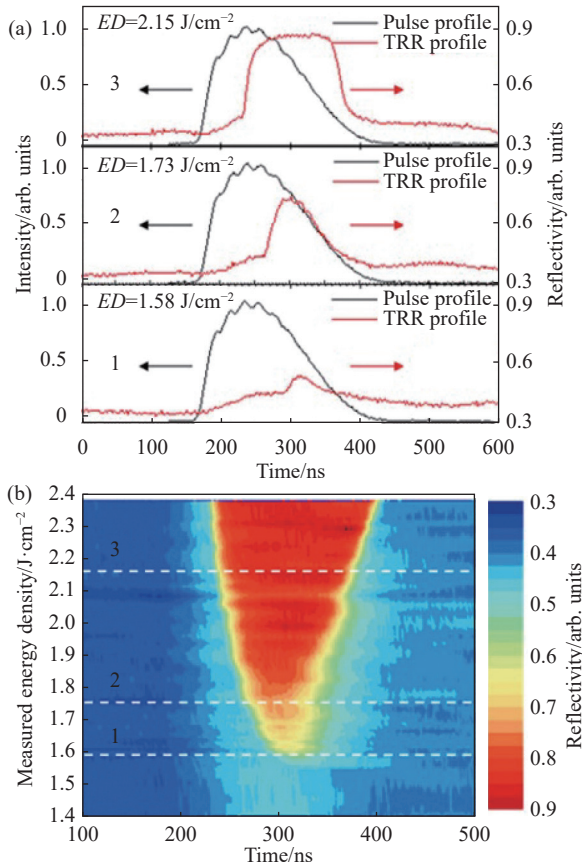


图 21 (a) 不同激光能量密度的时间分辨反射率 (TRR) 和激光脉冲剖面; (b) 反射率随时间和激光能量密度的关系^[75]

Fig.21 (a) Time resolved reflectance (TRR) and laser pulse profile at different laser energy densities; (b) The relationship between reflectance and laser energy density^[75]

1.80 J/cm² 时, 该层被划分为不同的区域, 从 Si/SiGe 表面约 5 nm 以下是结晶层, 而约 5 nm 内的近表面区域似乎是非晶态的, 且 L Dagault 还解释道, 通过图像分辨率差异可以观察到熔化层的面内应变曲线显示出比未熔化层更高的变形, 表明应力松弛主要发生在熔化部分。然而, 即使在未熔化的区域, 应变值也没有达到零, 这也表明了该层的部分弛豫。

Imen Karmous^[76] 等使用准分子纳秒激光退火对 Si 上 SiO₂/Si 堆叠褶皱的产生进行了研究。SiO₂/Si 堆叠结构对 308 nm 波长的光的反射率会随着 SiO₂ 厚度的变化产生周期性变化, 这是由不同界面的反射间的干涉导致的 (空气/SiO₂ 和 SiO₂/Si), 使得底层 Si 的融化能量密度阈值会随着 SiO₂ 厚度的变化而变化。此外, 对于一定的 SiO₂ 厚度, 较大的 Si 融化深度可能导致 Si 衬底表面保持熔融的时间增加, 进一步使得

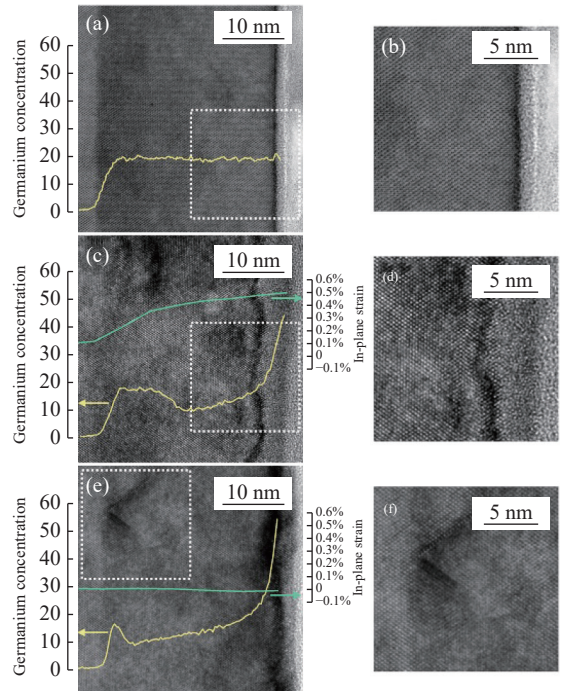


图 22 初始厚度为 30 nm 的 Si_{0.8}Ge_{0.2} 层在 (a)~(b) 1.59 J/cm², (c)~(d) 1.80 J/cm² 和 (e)~(f) 2.00 J/cm² 准分子激光退火后的截面 TEM 图^[75]

Fig.22 TEM images about 30 nm Si_{0.8}Ge_{0.2} thickness annealed by (a)~(b) 1.59 J/cm², (c)~(d) 1.80 J/cm² and (e)~(f) 2.00 J/cm² excimer laser^[75]

SiO₂ 薄膜变形或松弛, 导致褶皱形成。

3 金属层的准分子激光退火处理

复杂集成电路中层间互联的质量对集成电路的性能影响很大, 因此在新的工艺中引入了更多的金属层, 铜曾经就是其中比较典型的材料, 但是超过了 7 nm 节点。新的金属 (如: 钌) 开始作为铜的替代品, 因为它在线路电阻和可靠性方面都有潜在的好处。然而相比铜来说, 处理钌的热预算要远高于它, 高能量的纳秒准分子激光是较为理想的选择。

C. Fenouillet-Beranger^[77] 等在确定了结激活的退火窗口之后, 对脉冲宽度为纳秒级的脉冲激光退火对层间金属互连的影响进行了模拟。他们对器件进行建模, 然后在不同的激光能量密度条件下进行激光退火模拟。图 23 所示为模拟的能量密度 0.4 J/cm²、脉冲时间小于 200 ns、波长 308 nm 的准分子激光脉冲温度场和时间演化。模拟结果表明, 顶部氧化层厚度对损伤能量密度阈值没有影响, 且较大的顶部氧化层

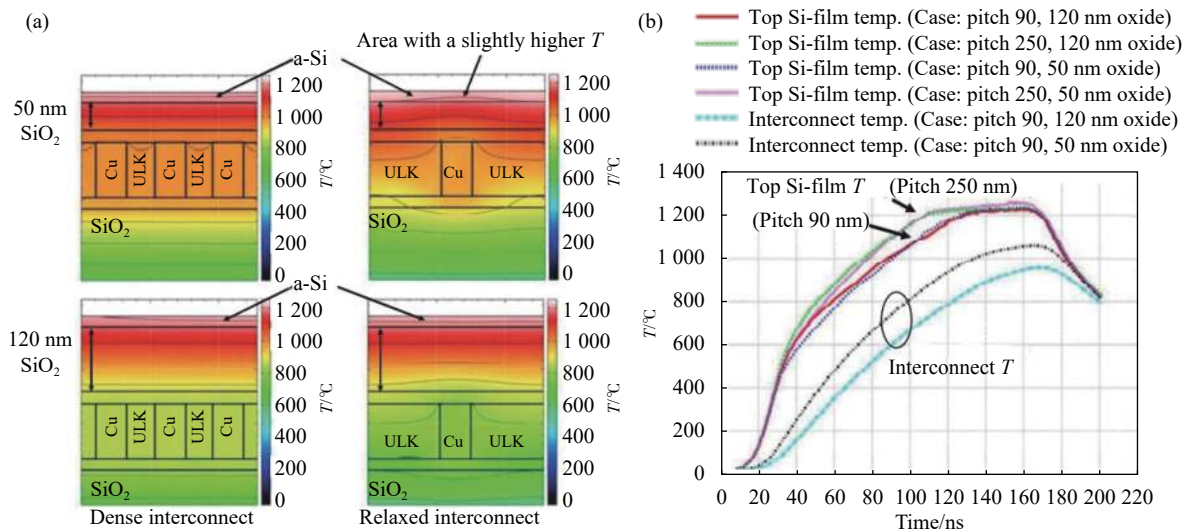


图 23 脉冲激光处理互连 (ULK/Cu) 结构的 (a) 温度场和 (b) 时间演化^[77]

Fig.23 (a) Temperature field and (b) time evolution of interconnect structures treated by pulsed laser (ULK/Cu)^[77]

厚度有助于降低铜互连的峰值温度。较厚的层间氧化层在激光退火中对底层互连完整性的保留,也使得高能量的纳秒准分子激光在三维集成中的应用前景进一步得到认可。

N. Jourdan^[78] 等研究了纳秒准分子激光退火下, 钎薄膜薄层电阻与晶粒生长之间的相关性。图 24 所示为 400 °C 下多次脉冲对薄层电阻的影响, 在其设定值的激光照射 10 次后, 逐渐增加激光照射次数, 薄膜电阻 (sheet resistance, R_{sq}) 会逐渐降低至 2.8 Ω/sq 。如图 25 所示, 对比 400 °C 持续 1 h 退火和纳秒准分子激光退火的材料截面 TEM 照片, 可以看到纳秒脉冲的准分子激光退火的材料晶粒明显增大, 平均晶粒尺寸

可以从约 23 nm 增加到 62 nm, N. Jourdan 解释道, 伴随着晶粒尺寸的变大, 薄膜电阻降低了约 20%, 相较于在纳秒准分子激光退火的情况下, 对样品 400 °C 持续 1 h 的退火几乎没有引起薄膜电阻的任何显著变化。

Y. Usami^[79] 等研究了 KrF 准分子激光退火对铜和钎半导体器件细金属线的电阻的影响。通过 KrF 准分子纳秒激光照射后, 铜的晶粒尺寸提高了一倍, 电阻率降低了 20% 左右。在钎中, 晶粒尺寸增大约 1.2 倍, 电阻率降低约 10%, 如图 26 所示。Y. Usami 等对实验结果的解释为, 激光照射增大金属晶粒尺寸可以抑制电子边界散射, 降低电阻率。

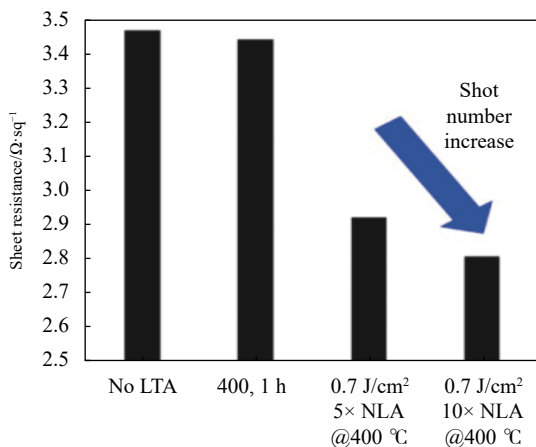


图 24 400 °C 下多次脉冲对薄层电阻的影响^[78]

Fig.24 Effect of multiple pulses on sheet resistance at 400 °C^[78]

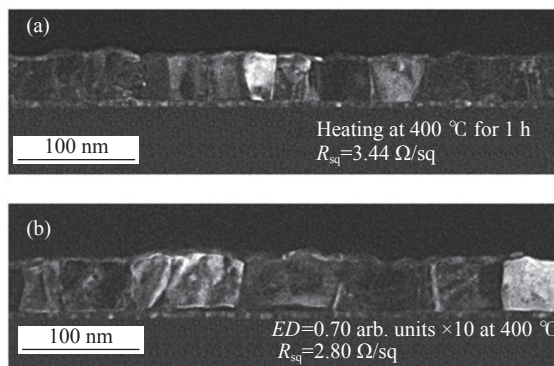


图 25 400 °C 持续 1 h 热退火和准分子激光退火的材料截面 TEM 照片^[78]

Fig.25 TEM images of cross sections of materials subjected to heat annealing at 400 °C for 1 hour or excimer laser annealing^[78]

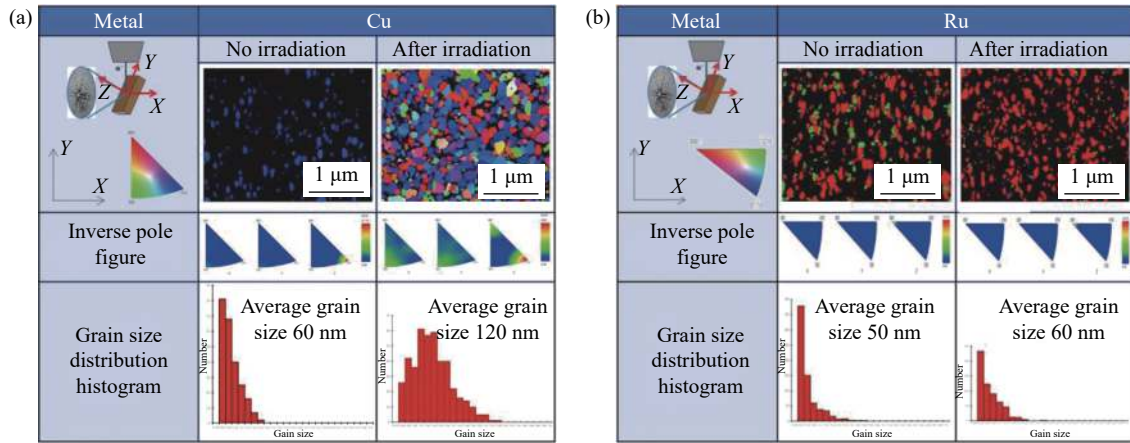


图 26 激光退火的电子背散射衍射图及金属晶粒尺寸直方图^[79]

Fig.26 Electron backscatter diffraction pattern of laser annealing And grain size of metal diagram^[79]

4 3D 结构器件的准分子激光退火

在 3D 集成电路中, 通过将有源晶体管层层叠加, 用介电层隔开, 并由金属互连线相互连接, 可能是在没有设备缩放的情况下延续摩尔定律的最佳方式。该方式结构的示意图^[80]如图 27 所示。

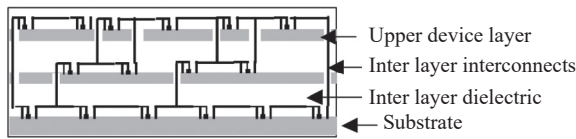


图 27 3D 集成电路结构示意图^[80]

Fig.27 Diagram of 3D integrated circuit structure^[80]

但是这种结构在制造时有一些问题, 在制造顶层器件时需要较高的热预算, 这可能会影响掺杂剂在下层的分布, 以及影响顶层以下金属丝的可靠性。晶体管制造中最重要的高热预算过程是高温退火, 以激活沟道和源漏区掺杂剂。然而, 在这一过程中, 下层金属和器件层可能也会被加热, 这是不希望产生的, 因此脉冲激光退火技术也作为一种有前途的掺杂活化技术被引入。超短、高强度激光脉冲可以使上层器件被融化, 而尽可能使下层器件不受影响, 在随后的再结晶过程中, 上层器件掺杂剂移动到晶格中的取代位点, 从而达到激活的目的, 为保留下层器件的完整性带来可能。

A. Vandooren^[81]等在三维顺序集成 (3D sequential integration) 的顶层器件中进行了准分子激光源漏的掺杂激活与晶格修复的研究, 证明了准分子激光退

火可以有效激活外延的硅薄膜器件中 n 型和 p 型掺杂, 与替代金属栅工艺流程和选择性源/漏外延完全兼容。图 28 所示为尖峰退火和准分子激光退火器件 TEM 对比图, 图像显示源漏外延层缺陷较小。此外, A. Vandooren 等还发现, 在经过准分子激光退火后的器件性能至少与经过尖峰退火的器件性能一样好。

C. Fenouillet-Beranger^[82]等首次在先进的原位掺杂源/漏全耗尽 SOI 技术上量化了底部 MOSFET 的最大热预算, 并且进行了模拟, 制作了当时最佳工艺结构模型, 提供了瞬时激光电场和二维结构中吸收功率密度的图像, 此外还做了一个顶部晶体管上添加一个 30 nm 的 SiN 盖层的模型, 与没有盖层的情况相比, 源漏吸收激光功率的数量和均匀性增加了, 如图 29 所示。

最终通过自制模拟软件 (custom simulator) 给出了温度场作为时间的函数, 得到了模拟器件栅极被激光退火时温度在 200 ns 内不超过 600 °C 的结果, 如

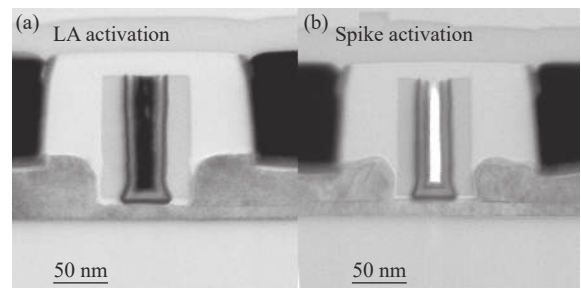


图 28 准分子激光退火器件 (a) 和尖峰退火 (b) TEM 对比图^[81]

Fig.28 TEM comparison of excimer laser annealing device (a) and spike annealing device (b)^[81]

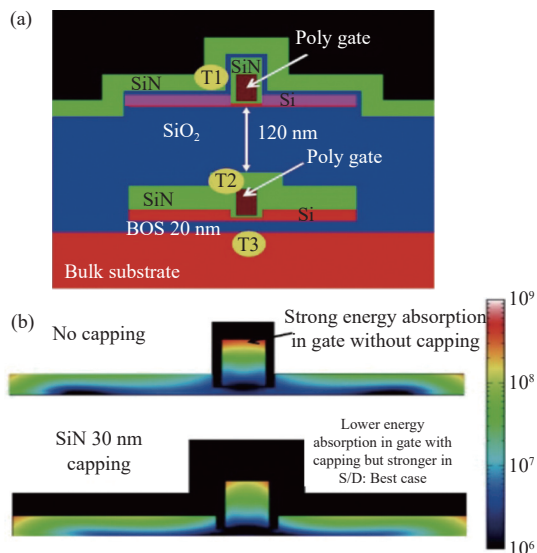


图 29 模拟结构及二维结构吸收功率密度对比图^[82]

Fig.29 Simulated structure and comparison of absorption power density of two-dimensional structure^[82]

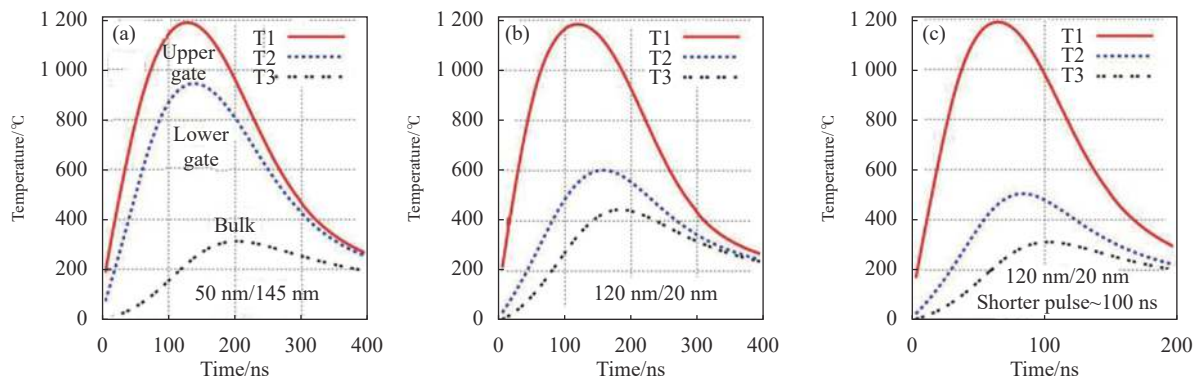


图 30 层间氧化物和底层氧化物的温度与时间的关系。T1: 上层栅极层的温度, T2: 下层栅极层的温度, T3: 体硅顶部的温度^[82]

Fig.30 The relationship between temperature and time of interlayer oxides and underlying oxides. T1: the temperature at the upper grid, T2: the temperature at the lower grid, and T3: the temperature at the top of the bulk silicon^[82]

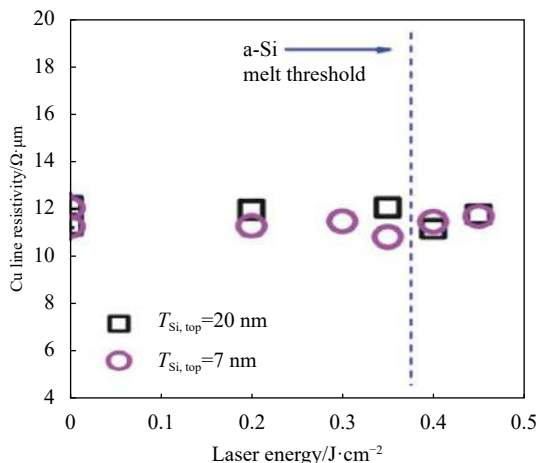


图 31 铜互连线电阻率随激光能量变化规律^[83]

Fig.31 The resistivity of copper interconnection wire changes with laser energy^[83]

图 30 所示。其中模拟使用了波长 308 nm、脉冲时间约 200 ns 的激光。参考文献 [82] 展示了激光退火在 3D 堆栈中的前景。

C. Cavalcante^[83] 等采用 160 ns、308 nm 的准分子激光对采用 FDSOI 技术的不同非晶硅厚度 28 nm Cu/ULK 器件 (7 nm 和 20 nm) 进行超快退火的模拟, 并且对底层设备和互连结构的抗扰度进行了评估。

在激光退火后, 两种非晶硅厚度的器件不管顶部温度如何, 即使超过了 a-Si 的熔体阈值, 铜互连线电阻率也保持不变, 如图 31 所示。C. Cavalcante 等人还使用 LIAB 软件进行二维数值模拟, 以确定底层所承受的温度。当非晶硅厚度为 20 nm 时, 铜互连线温度仍低于 500 °C, 如图 32 所示; 而当非晶硅厚度为 7 nm 时, 铜互连线温度达到 600 °C, 但仅为 100 ns。证明了使用 160 ns、308 nm 的准分子激光可

以在达到 a-Si 熔体阈值的条件下不对铜互连线产生影响。

3D 垂直沟道器件是新一代 NAND 非易失性存储器应用的优秀替代方案, 其中通心粉结构 (macaroni-type) 能够提高器件的可控性。在通心粉结构中, 完整的多晶硅沟道被薄的多晶硅管所取代, Si 的减小可能会转化为较低的串电流, 为了提高读取所需的电流, 必须对晶界处散射和界面缺陷进行处理。

J. G. Lisoni^[84] 等对使用准分子激光为全沟道 (full channel) 器件沟道退火进行了研究, 如图 33 所示。相比快速诱导退火得到的晶粒准分子激光退火 LTA 得到的晶粒更大, 并且在之后的实验中进一步证实, 在使用准分子激光退火后不仅会得到更大粒径的晶粒,

产生更少缺陷的晶界, 还能使得器件的可靠性得到提升。

G. Congedo^[85] 等使用准分子激光对通心粉结构和全沟道结构的沟道退火进行了研究。如图 34 所

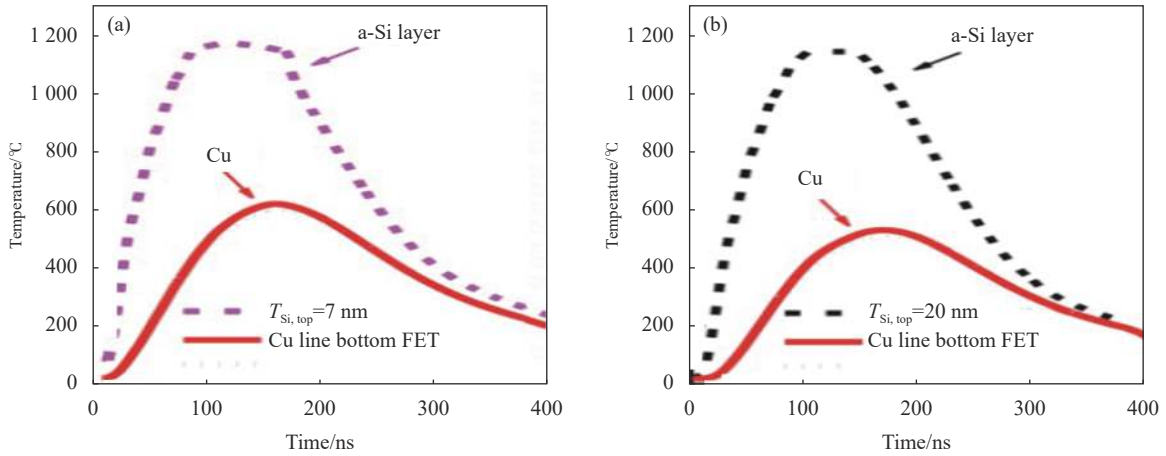
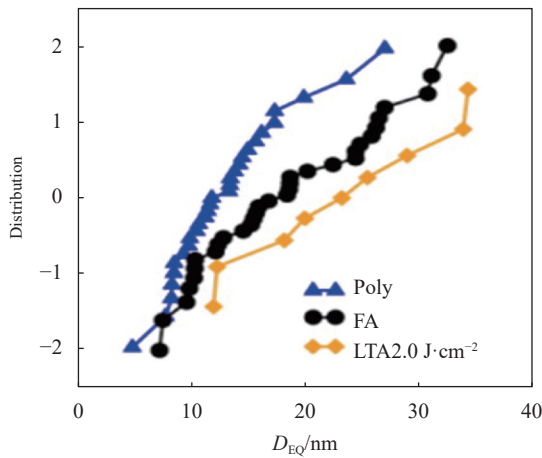


图 32 准分子激光退火后不同顶层厚度的器件 a-Si 层、铜互联线的温度随时间变化图^[83]

Fig.32 The relationship between temperature and time about devices's a-Si layer and Cu interconnection with different layers of thickness after excimer laser annealing^[83]



Si-channel type	Mean D_{EQ}/nm	Median D_{EQ}/nm
Poly	14	12
FA	22	19
LTA2.0 J·cm ⁻²	24	23

图 33 不同退火方式 Si 粒径大小^[84]

Fig.33 Si size with different annealing methods^[84]

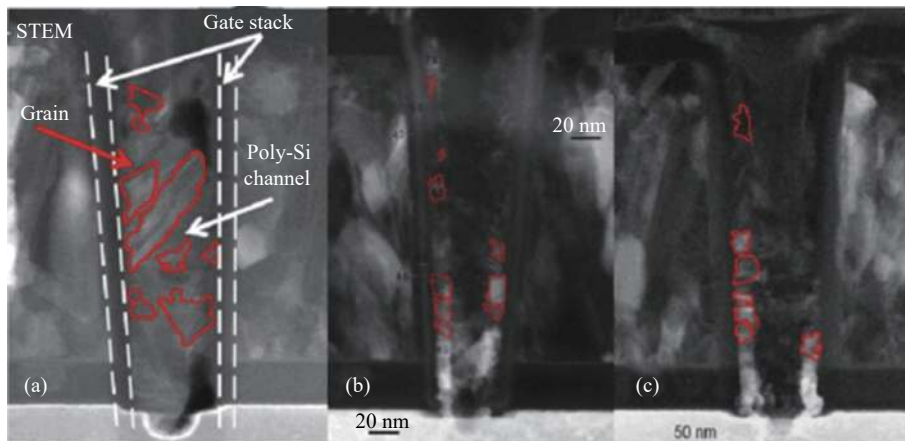


图 34 (a) 全沟道器件、(b) 通心粉结构器件、(c) 激光退火后的通心粉器件暗场 STEM 图^[85]

Fig.34 Dark field STEM diagrams of (a) full channel device, (b) macaroni-type device, and (c) macaroni-type device with excimer laser annealing^[85]

示,通心粉结构和全沟道结构中,全沟道器件的晶粒较大,通心粉器件的晶粒较小,而通过激光退火之后对比,未经过激光退火的通心粉器件晶粒结构没有明显改变。图 35 所示为三种不同情况等效晶粒直径的统计分布,G. Congedo 等给出的解释为,在通心粉结构的情况下,较小的可用体积阻止了晶粒向中心扩展,从而限制了等效晶粒直径。

在通心粉结构中,由于可用体积有限且沟道有两个接口,接口缺陷和沟道质量在 I_D-V_G 特性中起着极其重要的作用。图 36 显示,准分子激光退火后的器件缺陷大幅减少,与此同时,器件得到了更高的电流和更低的阈值电压。

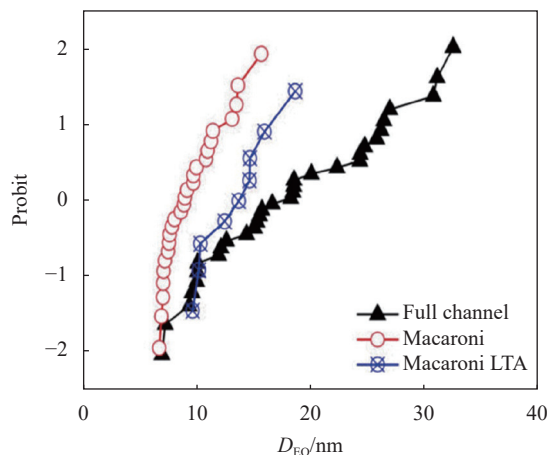


图 35 等效晶粒直径对比图^[85]

Fig.35 Comparison of equivalent grain diameter (D_{EQ})^[85]

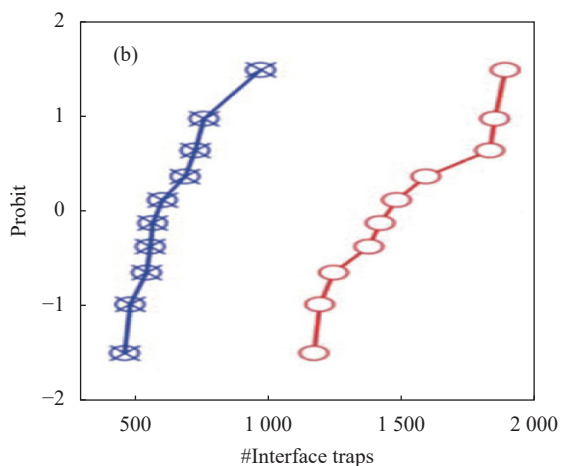
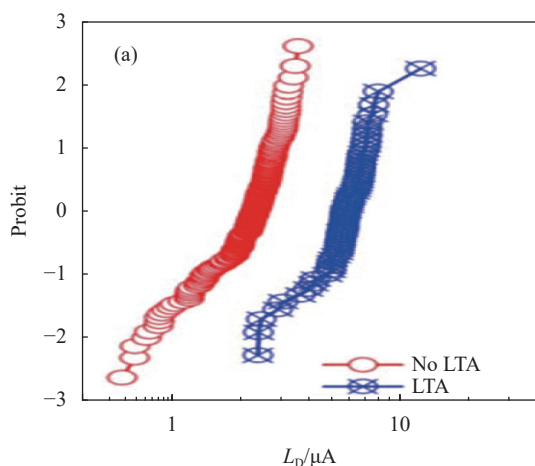


图 36 漏极电流统计分布和界面陷阱数量的分布^[85]

Fig.36 Drain current statistical distribution and interface traps distribution^[85]

5 总结与展望

与传统的退火炉退火以及快速热退火等退火工艺相比,准分子激光器输出激光峰值功率高,波长在紫外区,准分子激光作用于物质表面时能量能迅速地被物质表面吸收,便于对材料表面温度梯度的控制。在半导体集成电路制造的热处理工艺中具有一定优势:准分子激光退火能够有效降低退火热预算并更加精确地控制退火效果,因此,对于准分子激光退火在半导体集成电路制造中的应用已有大量的方法和实验研究结果;准分子激光退火有利于高密度掺杂,获得高的掺杂激活效率,并且能更好地使掺杂原子均匀地分布,控制结深度形成超浅结;准分子激光退火对金属层退火还可以增大金属晶粒尺寸,抑制电子边界

散射,降低电阻率,较好的热预算控制也会提高金属的可靠性,为新的工艺中引入高 k 金属层带来可能;在 3D 集成电路中,有效减少热预算、提高器件稳定性、解决顶层器件退火对下层掺杂剂分布影响等方面也具备较好的前景。

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Research progress of excimer laser annealing in semiconductor integrated circuit manufacturing

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Abstract:

Significance In the dynamic landscape of semiconductor device fabrication, continual advancements strive to enhance the process. As the density of transistors per unit area increases and chip components become progressively smaller, the challenges in chip production grow in both intricacy and difficulty. Traditional methods like furnace annealing are becoming inadequate for the evolving demands of chip manufacturing. To address the intricacies posed by shrinking device sizes, annealing techniques and process parameters undergo constant refinement. Pulsed laser annealing emerges as a noteworthy solution, capable of precisely irradiating specific

material areas in extremely brief intervals. This technique, harnessed by absorbing laser energy, rapidly elevates the material surface temperature to induce melting. The consequential reconstruction of the melt layer's crystal structure, coupled with redistributed doping in the crystal, serves the crucial purpose of eliminating defect-activated doping. The excimer laser, operating as a nanosecond pulsed ultraviolet laser, holds distinctive attributes that render it particularly meaningful in semiconductor manufacturing annealing technology. Its short wavelength, narrow pulse width, and minimal material penetration depth, especially in semiconductor materials like silicon, contribute to high absorption rates. Moreover, excimer lasers boast high resolution in focusing or projection, coupled with substantial single-pulse energy. This inherent flexibility allows for shaping the energy distribution of the pulse spot, offering adaptability to diverse requirements. These defining characteristics underscore the significance of excimer laser research in advancing semiconductor manufacturing annealing technologies.

Progress To optimize the annealing effect in semiconductor manufacturing, it is crucial to shorten the thermal annealing time window and carefully regulate peak temperatures. Controlling the temperature gradient from the material's surface to its interior is a pivotal consideration in annealing technology. Laser annealing is a superior alternative, offering more precise thermal budget control when compared to other methods, as illustrated in Fig.1. Additionally, the perspective of K. Huet et al. on laser thermal budget is presented. Researchers have explored the application of laser annealing in ion doping and epitaxial layer growth. The evolution of doping concentration across different substrates and dopants under excimer laser conditions has been thoroughly investigated. Brief insights into strain silicon technology and silicon on insulator technology are provided, showcasing their integration into semiconductor manufacturing for enhanced device performance. Excimer lasers have been employed by researchers to delve into devices utilizing strained silicon technology and silicon on insulator technology. In the continuous evolution of semiconductor manufacturing processes, there is ongoing innovation in the metal layer. Laser annealing treatment of the metal layer has garnered increased attention, with the reasons for this emphasis briefly explained. Notably, researchers have scrutinized the annealing of metal layers using excimer lasers. The paragraph concludes by briefly addressing the challenges associated with three-dimensional integrated circuit architecture (refer to Fig.27). Manufacturing three-dimensional integrated circuits poses difficulties, particularly in potential damage to the underlying metal and devices during upper-layer annealing. Excimer lasers have emerged as a research focus to address these challenges and optimize the annealing process for three-dimensional integrated circuits.

Conclusions and Prospects Excimer laser annealing stands out as a superior choice when compared to alternative annealing methods, particularly evident in the realm of semiconductor integrated circuit manufacturing. The distinct advantages of excimer laser annealing manifest in its exceptional ability to significantly reduce the thermal budget while enabling precise control over the annealing effect. This accuracy proves pivotal in semiconductor manufacturing processes. Moreover, excimer laser annealing brings noteworthy benefits to the table, including the facilitation of high-density doping with enhanced doping activation efficiency. Its unique capacity to distribute doping atoms more effectively and control junction depth contributes to its prominence in the semiconductor industry. The application of excimer laser annealing on metal layers introduces additional advantages. It effectively augments the grain size of the metal, curbing electron boundary scattering, thereby reducing resistivity. This not only enhances the reliability of the metal but also allows for superior thermal budget control. In the context of three-dimensional integrated circuits, excimer laser technology emerges as a transformative solution. It proves highly adept at reducing the thermal budget, a critical consideration in enhancing device stability within these intricate structures. Furthermore, its promising potential lies in addressing the challenges associated with annealing effects on the dopant distribution of the top layer. Excimer laser

annealing, with its multifaceted advantages, thus emerges as a promising and versatile solution for optimizing semiconductor manufacturing processes, particularly in the context of three-dimensional integrated circuits.

Key words: semiconductor manufacturing process; thermal budget; laser annealing; excimer laser

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