A high performance TDI readout circuit for scanning type infrared sensor

Wang Zhenxiang[1], Hu Kai[2]

(1. School of Microelectronics, Tianjin University, Tianjin 300072, China;
2. School of Integrated Circuit Science and Engineering, Tianjin University of Technology, Tianjin 300072, China)

Abstract: With the increased demand for long-range imaging systems such as remote sensing and satellite imaging, scanning type infrared sensors have been deployed extensively. To alleviate the problem of relatively poor SNR that would affect the image quality, a readout circuit with a time-delayed integration (TDI) technique was proposed and described. The readout circuit consisted of capacitor trans-impedance amplifier (CTIA) pixel circuits, paralleled TDI stages, multiplexer, and output buffer. CTIA based analog front-end circuit with optional gain and less than 0.3% nonlinearity was designed for processing large range photocurrent. The chip was manufactured with a 0.35 μm CMOS process and occupied an area of 1.3 mm×20 mm. With the 5 V power supply, the power consumption was less than 60 mW. To evaluate the function of the 1 024×3 TDI readout circuit, different voltages were injected into three terminals and the output from the TDI stage was captured. The measurement results validate the proposed design successfully.

Key words: infrared sensor; readout circuit; TDI

CLC number: TN453 **Document code:** A **DOI:** 10.3788/IRLA20210072

高性能 TDI 扫描式红外传感器读出电路研究

王祯祥[1], 胡 凯[2]

(1. 天津大学 微电子学院, 天津 300072;
2. 天津理工大学 集成电路科学与工程学院, 天津 300072)

摘 要: 扫描式红外成像传感器在遥测遥感、卫星成像等远距离成像领域具有广泛的应用。为了缓解信噪比相对较低而影响图像质量的问题,提出了一种时间延时积分 (TDI) 型读出电路。该读出电路由电容跨阻放大器 (CTIA) 像素电路阵列、并行 TDI 电路、多路开关选择电路和输出缓冲器等组成。为实现对宽动态范围光电流的处理,CTIA 电路设计有多档可选增益,且非线性度小于 0.3%。该读出电路采用 0.35 μm CMOS 工艺设计与制造,芯片面积约为 1.3 mm×20 mm,采用 5 V 电源时功耗小于 60 mW。为了评估 1 024×3 TDI 读出电路的功能,采用了对 TDI 输入端注入不同电压激励的方式进行测试,测试结果验证了所提出的设计方案。

关键词: 红外传感器; 读出电路; 时间延时积分 (TDI)

收稿日期:2021-01-27; **修订日期:**2021-04-12

作者简介:王祯祥, 男, 博士生, 主要从事光电器件及光电系统可靠性方面的研究。

0 Introduction

Scanning type infrared sensors have always been used in long-range imaging systems such as remote sensing systems, surveillance systems, satellite imaging systems, and so on[1−4]. In these imaging systems, the infrared detector is arrayed as one or more rows, the full image is taken depending on the scanning nature of the carrier itself, such as the satellite. For the long-range application, the image quality is always affected due to the relatively lower SNR[5−9]. TDI technique has been proposed and adopted to alleviate this problem[10−11]. The principle of the TDI technique is straightforward: the object is scanned by several rows of detectors in a time-delayed manner, then the signals produced by pixel stages, which are corresponding to the same specific image point, are added and averaged in the TDI stage. With the add operation, the output signal is increased with the factor of n (n is the number of scanning detectors), while the uncorrelated noise is increased with the square root of the n. Therefore, the SNR is also improved with the square root of the n. The TDI algorithm is often implemented in the analog domain or digital domain. In this design, the analog TDI is chosen for its simplified realization.

1 Readout circuit design

1.1 System architecture

To improve the resolution of the imaging system, the infrared detector chosen for the design is arrayed as shown in Fig.1. The odd and even columns are separated and placed in two different rows, enabling the horizontal overlap between the consecutive pixels. The pixel pitch between odd and even columns is designed as width as 20 μm. Two extra rows of detectors are added vertically with a 40 μm pitch. The detector is scanned with a step of 20 μm along the scanning direction. With this configuration, a scanning type infrared detector with 1 024 pixels is realized with the feasibility of implementing 3× TDI.

The detector is bonded to a readout circuit (ROIC) with an indium bump. The ROIC consists of an array of capacitor trans-impedance amplifier (CTIA) circuits located under each detector pixel, column paralleled TDI stages, switch matrix to multiplex the TDI outputs, and output buffer stage to drive the large capacitive load.

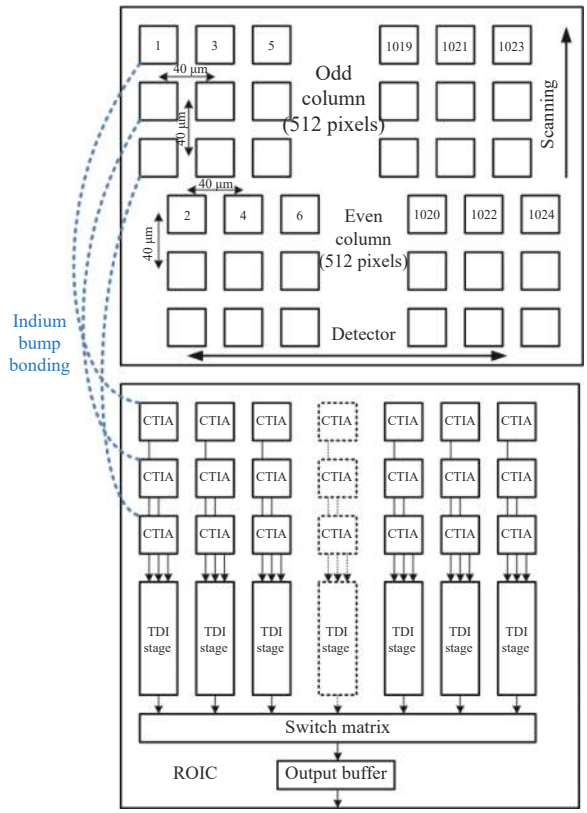

Fig.1 Block diagram of detector and ROIC

1.2 CTIA pixel stage

The CTIA architecture is chosen as the pixel circuit to convert the photocurrent into voltage for its superior linearity and detector bias stability compared to its competitor. The detailed circuit diagram is shown in Fig.2, which is comprised of one core operational transconductance amplifier (OTA), CMOS switches, and variable integration capacitor. The offset of OTA is the main source of fixed pattern noise (FPN) in the infrared image, therefore the offset cancellation technique is introduced in the design. The CTIA operates in two phases: the reset phase and the integration phase. INT and INT_N are two control clocks with opposite phases. In the reset phase, INT_N is high, the switches S1 and S2 are closed, S3 is opened. The CTIA is configured as a unity

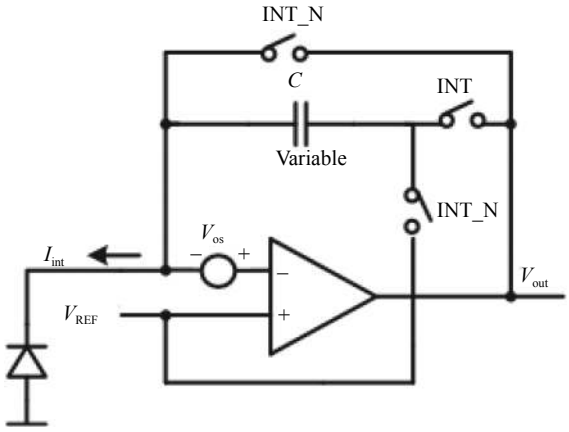

Fig.2 Detail circuit diagram of CTIA

gain buffer, the integration capacitor is reset and served to store the offset of OTA. Assuming limited voltage gain as A_v, the output voltage of CTIA is reset to

$$V_{out}=\frac{A_v(V_{REF}-V_{os})}{1+A_v} \tag{1}$$

Therefore, the charge stored on the left side of the capacitor can be expressed as:

$$Q_{reset}=C(V_{out}-V_{REF})=-C\frac{V_{REF}+A_vV_{os}}{1+A_v} \tag{2}$$

When switching to the integration phase, the INT turns high, the switches S1 and S2 are opened, S3 is closed. The capacitor is connected in the feedback path between the negative input terminal and output. Neglecting the effect of charge injection and clock feedthrough, the initial output voltage of CTIA right after the switching activity can be derived from the following equation base on the charge conservation for the left plate of the integration capacitor. The formula of the charge stored and the output voltage is given by Eqs.(3) and (4).

$$Q_{reset}=C\left(V_{REF}+\frac{V_{out}}{-A_v}-V_{os}-V_{out}\right) \tag{3}$$

$$V_{out}=\frac{(2+A_v)A_v}{(1+A_v)^2}V_{REF}-\frac{A_v}{(1+A_v)^2}V_{os} \tag{4}$$

It is convenient to get the conclusion that the offset-induced error would be greatly reduced as long as the voltage gain is large, eliminating the offset-induced FPN that would be happened in the conventional CTIA circuit.

The detector bias is held constant due to the virtual short characteristic of the feedback, facilitating the linear response of the detector. When the photocurrent produced by the detector flows through the capacitor within the integration timing window, the output voltage of CTIA will change linearly from the initial value derived in the previous equation.

For the limited pixel area as small as 40 μm×40 μm, the OTA is designed as a differential amplifier with only 5 transistors. To accommodate the large dynamic range with photocurrent, a variable integration capacitor ranging from 5 fF to 130 fF is designed. The simulated result in Fig.3 shows less than 0.3% nonlinearity, demonstrating the advantage of the chosen CTIA circuit.

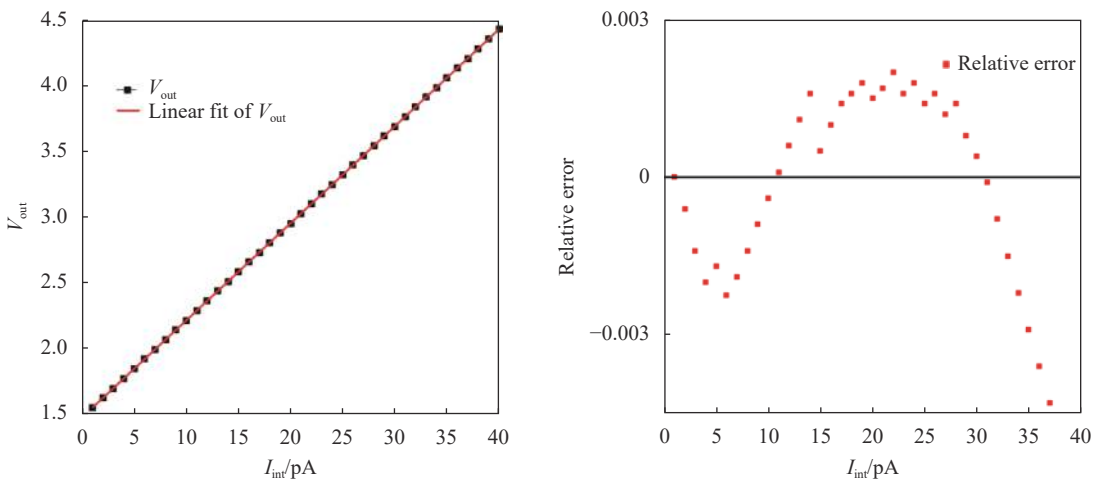

Fig.3 Simulated linearity of CTIA

1.3 TDI stages

The designed TDI schematic is shown in Fig.4, where the Vi<1>-Vi<3> is the output from the previous CTIA pixel stage. As is described in the previous section, because the detector is scanned with the step of the half-pitch, the image captured by the first detector will be captured after two steps by the second detector, and four steps by the third detector. For this purpose, 5/3 capacitors are needed to sample/store the pixel output originating from the first/second detector respectively.

The TDI circuit is also operated in two phases: sampling phase and charge transferring phase. In the sampling phase, three sampling switches are closed and all the other switches are opened, the output voltages from the CTIA pixel circuits are sampled into the storage capacitors connecting to the closed sampling switches. In the transferring switches, three specific transferring switches are closed and all the other switches are opened, the charges stored on the capacitors connecting to the closed transferring switches are averaged and transferred to the TDI output through the feedback capacitor.

To accomplish the scanning process of one image point, five steps are needed before the averaging operation can be applied for this specific point. With the detailed timing diagram in Fig.5, the needed five steps are shown as follows.

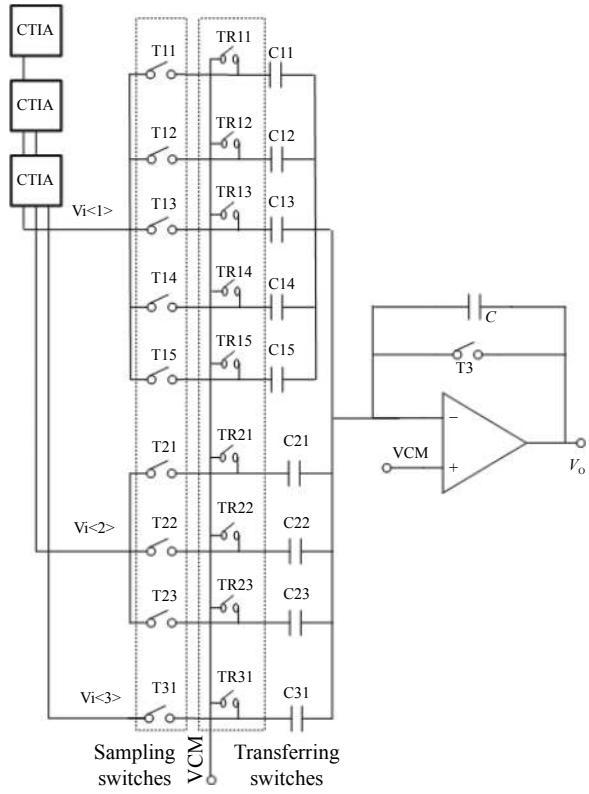

Fig.4 TDI schematic

Assuming the image point (donated as the red box in the diagram) is exposed to the first detector exactly in the first scanning step, sampling switches T11, T21 and T31 are closed, the output voltages from the three-pixel circuit are sampled on the corresponding capacitors. Specifically, the capacitor C11 captures the signal associated with the image point. The sampling switches are opened in the sub-

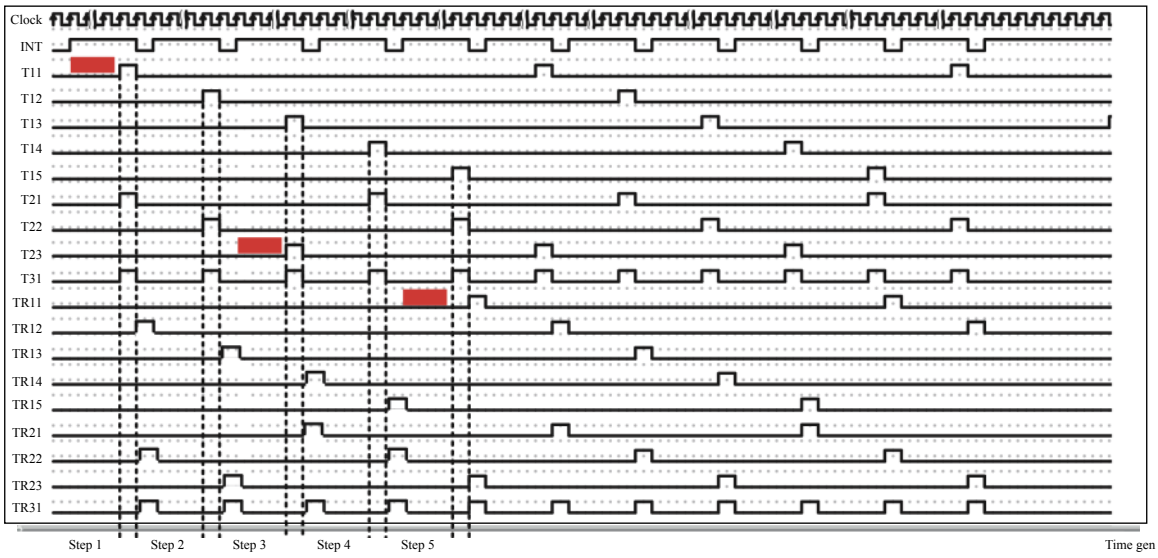

Fig.5 Timing diagram of TDI

sequent transfer phase, therefore the signal is frozen on the floating capacitor C11, which state is maintained for four steps until the averaging operation can be carried out.

In the second step, the sampling switches T12, T22, T31 are closed. But because the scanning step is limited to half the pixel pitch, none of the detectors can cover the image point.

In the third step, the image point is exposed to the second detector. At the same time, the sampling switches T13, T23, T31 are closed. Therefore, the signal associated with the image point can be sampled and frozen for two steps on the floating capacitor C23.

The operation in the fourth step is similar to that of the second step, except the sampling switches are changed to T14, T21, and T31.

In the fifth step, the image point is exposed to the third detector. With the closed switches of T15, T22, T31, the signal associated with the object can be sampled to the capacitor C31.

At this point, the signals sampled on the capacitor C11, C23 and C31 are available to enhance the SNR. The transferring switches TR11, TR23, and TR31 are closed, the stored signal is averaged and transferred to the TDI output.

For the next step, it is easy to infer that the signals sampled into the capacitor C12, C21, and C31 are just the right outputs resulting from the same exposed imaging point. Therefore, the averaging operation will be carried out continuously.

1.4 Output buffer

The output buffer is necessary to drive the highly resistive and capacitive load within the limited time for the multiplexed TDI output. As the TDI outputs are varied from different stages, the large-signal behavior, or slew rate characteristic is of importance for the output buffer.

To decrease the settling time, there are two feasible approaches. One can choose to increase the static bias current, or choose the push-pull output structure. The latter technique is adopted for the low power consideration. The simplified schematic is shown in Fig.6.

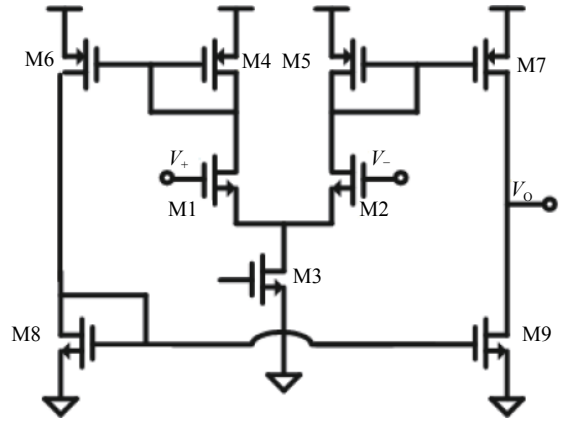

Fig.6 Simplified diagram of output buffer

2 Measurement Result

Part of the chip layout is shown in Fig.7. The chip was fabricated with a 0.35 μm CMOS process and occupies an area of 1.3 mm×20 mm. With the 5 V power supply, the power consumption is less than 60 mW.

To validate the CTIA pixel circuit, one external resistor is connected to the input, converting the applied voltage into the current. Fig.8 shows the voltage output directly from the CTIA circuit, it is clear to distinguish the reset phase and integration phases.

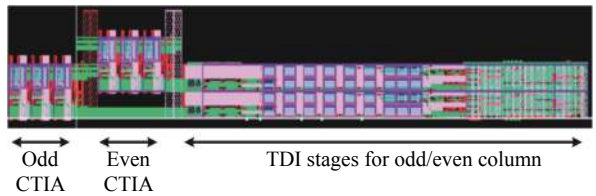

Fig.7 Odd and even column layout of ROIC

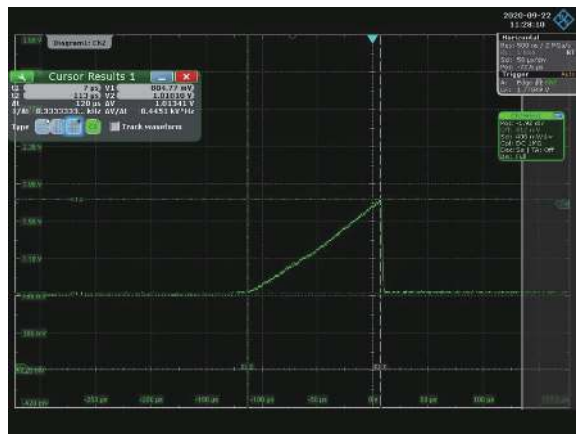

Fig.8 Captured output voltage from CTIA pixel circuit

To validate the TDI stages, three different voltages are injected into the terminals Vi<1>, Vi<2>, and Vi<3>. Tab.1 summarizes the different combinations of three voltages and TDI output voltage. The averaging operation is realized successfully under all conditions.

Tab.1 Injected input & captured output from TDI stage

Input 1/V	Input 2/V	Input 3/V	Output/V
0.5	0.5	1	0.66
0.8	0.8	1	0.86
1	1	1	0.99
1.2	1.2	1	1.13
1.5	1.5	1	1.16

3 Conclusion

In this paper, a 1024×3 TDI readout circuit is proposed and implemented. This readout circuit consists of capacitor trans-impedance amplifier (CTIA) pixel circuits, paralleled TDI stages, multiplexer, and output buffer. The chip was manufactured with a 0.35 μm CMOS process and occupies an area of 1.3 mm×20 mm. With the 5 V power supply, the power consumption is less than 60 mW. The measurement results validate the proposed design successfully.

References:

[1] Hsieh C C, Wu C Y, Jih F W, et al. Focal-plane-arrays and CMOS readout techniques of infrared imaging systems [J]. ***IEEE Transactions on Circuits and Systems for Video Technology***, 1997, 7(4): 594-605.

[2] Kim Byunghyuk, Lee Hee Chul. Smart TDI readout circuit for long-wavelength IR detector [J]. ***Electronics Letters***, 2002, 38(16): 854-855.

[3] Hanamura H, Aoki M, Masuhara T, et al. Operation of bulk CMOS devices at very low temperatures [J]. ***IEEE Journal of Solid-State Circuits***, 1986, 21(3): 484-490.

[4] Tsai Fukai, Huang Hongyi, Dai Likuo, et al. A time-delay-integration CMOS readout circuit for IR scanning[C]// International Conference on Electronics, Circuits and Systems, 2002, 1: 347-350.

[5] Sizov F F, Derkach Y P, Kononenko Y G, et al. Readout device processing electronics for IR linear and focal plane arrays[C]//Proceedings of SPIE, 1999, 3698: 816-825.

[6] Chen L P, Hewitt M J, Gulbransen D J, et al. Overview of advances in high-performance ROIC designs for use with IRFPAs[C]//Proceedings of SPIE, 2000, 4028: 124-138.

[7] Carvajal R G, Ramírez-Angulo J, López-Martín A J, et al. The flipped voltage follower: A useful cell for low-voltage low-power circuit design [J]. ***IEEE Transactions on Circuits and Systems I : Regular Papers***, 2005, 52(7): 1276-1291.

[8] Yavari M. Single-stage class AB operational amplifier for SC circuits [J]. ***Electronics Letters***, 2010, 46(14): 977-979.

[9] Kayahan Huseyin, Yazici Melik, Ceylan Omer, et al. Design of ROIC based on switched capacitor TDI for MCT LWIR focal plane arrays[C]//Proceedings of SPIE, 2011, 8012: 80120M.

[10] Ceylan Omer, Kayahan Huseyin, Yazici Melik, et al. Design of 90×8 ROIC with pixel level digital TDI implementation for scanning type LWIR FPAs[C]//Proceedings of SPIE, 2013, 8704: 870432.

[11] Kayahan Huseyin, Ceylan Omer, Yazici Melik, et al. Wide range, process and temperature compensated voltage controlled current source [J]. ***IEEE Transactions on Circuits and Systems I: Regular Papers***, 2013, 60(5): 1345-1353.