Design of ultra-low-power readout circuit for 1 024×1 024 UV AlGaN focal plane arrays

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Abstract: A novel ultra- low-power readout integrated circuit (ROIC) for 1 024×1 024 ultraviolet (UV) AlGaN focal plane arrays (FPA) with 18 μm-pitch was presented. In order to optimize power consumption for UVFPA readout circuit these methods were adopted, which including single-terminal amplifier under subthreshold region as CTIA amplifier, common current source load for source follow (SF) buffer in column pixels and level shift circuits, and time-sharing tail current source for column buffer. The smallest operational current of CTIA in pixel unit is only 8.5 nA with 3.3 V power supply by using single-terminal amplifier. The ROIC has been fabricated in SMIC 0.18 μm 1P6M mixed signal process and also achieved better performances with the novel design of bias current adjustable. Furthermore, the overall power consumption of the chip is 67.3 mW at 2 MHz in 8-outputs mode by the above methods according to the experimental results.

Key words: readout integrated circuit (ROIC); ultraviolet focal plane arrays (UVFPA); ultra- low-power; CTIA

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1 024×1 024 AlGaN 紫外焦平面读出电路的超低功耗设计

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摘 要: 提出了一种新型的超低功耗读出电路用于 18 μm 中心距 1 024×1 024 面阵规模的 AlGaN 紫外焦平面。为了实现低功耗设计紫外焦平面读出电路,采用了三种设计方法,包括:电容反馈跨阻放大器 CTIA 结构采用工作在亚阈值区的单端输入运算放大器,列像素源随缓冲器和电平移位电路共用同一个电流源负载以及列级缓冲器的分时尾电流源设计。由于像素单元内 CTIA 采用了单端输入运算放大器,在 3.3 V 供电电压下,每个像素单元最小工作电流仅 8.5 nA。该读出电路设计了可调偏置电流电路使读出电路能得到更好的性能并基于 SMIC 0.18 μm 1P6M 混合信号工艺平台进行了设计制造。测试结果表明:由于采用了上述设计方法,整个芯片的功耗在 2 MHz 时钟 8 路输出模式下仅 67.3 mW。

关键词: 读出电路; 紫外焦平面; 超低功耗; 电容反馈跨阻放大器

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0 Introduction

Recent technological advances, the photoelectric detectors based on GaN with unique optical, electrical and structural properties have gradually matured. Because of their wide tunable direct bandgap, good carrier transport properties, high breakdown fields chemical stability and high robustness, AlGaN based solar-blind UV detector have been studied extensively in ultraviolet (UV) photodetectors. And UV imaging systems have been widely used in defense, scientific research, missile warning, offshore oil monitoring, spectroscopy, chemical and biological threat detection, environmental monitoring, astronomy and so on[1–4].

Readout Integrated Circuit (ROIC) is one of the most important parts of UVFPA. And due to the amount of pixels increasing rapidly for large formats resulting in the power consumption of readout circuit increases speedy, the realization of low power consumption has become one of the key challenges for ROIC design. To realize low power, the dynamic windowing and transposition methods have been proposed with the columns outside the window and the unused buffers are powered down[5]. Through proper design of readout timing and using two operating modes in column amplifiers to reduce power consumption have also been proposed[6]. What 's more, direct injection (DI), source-follower per detector (SFD) structures in pixels widely used to decrease power consumption[7–9]. To reduce power consumption for larger and larger pixel arrays, the design of low power cell circuit is necessary. In this study, a readout circuit is represented for 1 024×1 024 UVFPA of low power consumption which fabricated in SMIC 0.18 μm 1P6M mixed signal process. The CTIA structure in pixels is adopted by a current adjustment single-terminal amplifier to realize low power consumption. This circuit supports several adjustments optimize power for better performances. The chip achieves a minimum power only 67.3 mW at 2 MHz all frame rate in a 1 024×1 024 FPA with 18 μm-pitch.

1 Circuit description

The system architecture of the ROIC with snapshot integration mode is shown in Fig.1, including pixel array,

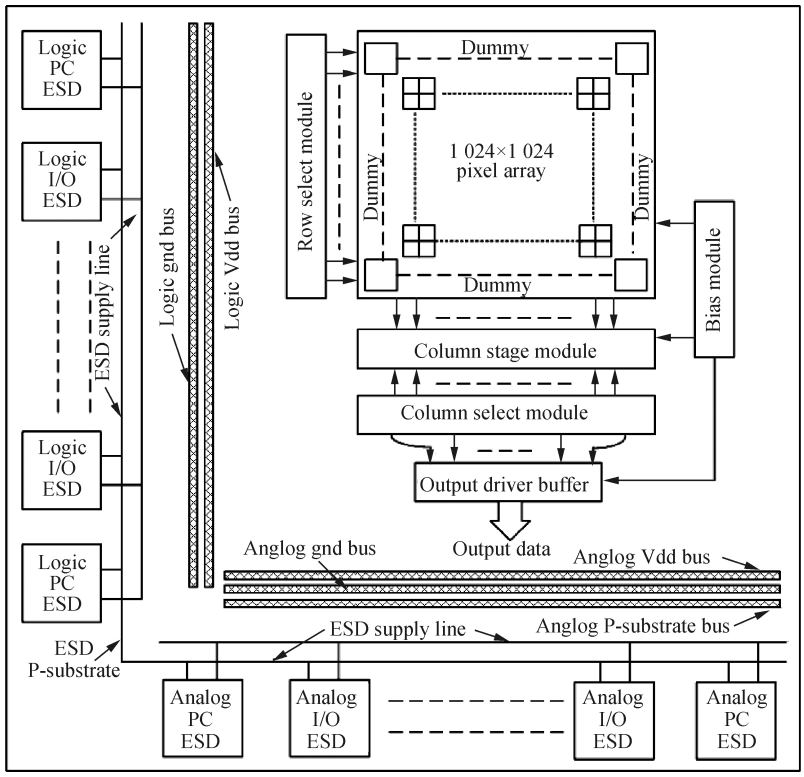

Fig.1 System architecture for UV AlGaN FPA readout circuit with whole chip ESD protection

column level shift, column buffer, output buffer, current bias, row and column select logic circuit, etc. The readout circuit mainly divides into analog modules, digital modules and whole chip ESD protection modules[10]. Analog modules consist of 1 024 × 1 024 pixel arrays, column stage, output driver buffer and bias modules. Digital modules consist of row select, column select and control logic modules. Analog and digital modules are supplied by different power buses part surrounding the chip respectively to prevent the cross-talk and noise between analog and digital signals.

Meanwhile, the whole chip ESD protection network mentioned in this paper are separated into logic and analog ESD protection modules. They are placed at the left and bottom part of the chip separately. The analog and Logic ESD modules are supplied by analog and digital supply lines, respectively, to decrease crosstalk effect. And various methods are adopted to improve robustness of the chip such as multi power clamps, dummy devices and top metal as light barrier covered the whole chip, etc.

This designed readout circuit has adjustable integration time, gain of CTIA and internal bias supplies, and has multi outputs. In addition, this circuit features snapshot mode with integrate-while-read (IWR) and integrate-then-read (ITR) operation that all pixels integrate simultaneously per integration period.

2 Low power implementation

Though direct injection (DI), source-follower per detector (SFD) structures in pixels widely used to decrease power consumption, but they can't provide constant bias voltage for photodiode resulting in lower conversion factor. Therefore, the CTIA is adopted with stable bias voltage, good linearity, high injection efficiency and wide detecting range. What's more, to realize larger format FPA of low power, the design of ultra-low-power pixel is the key point, so a single-terminal amplifier using the cascode configuration instead of two- terminal amplifier as pixel amplifier in this paper to optimize the power consumption as small as possible. What's more, it substantially reduces the power consumption by operating amplifier transistors under subthreshold region and the smallest operational current of CTIA in pixel unit is only 8.5 nA. The current can be expressed as:

$$I_{\mathrm{D}} = I_{\mathrm{DO}} \frac{W}{L} \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_{\mathrm{T}}}\right)\left[1 - \exp\left(\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right] \tag{1}$$

$$\eta \approx \frac{C_{\mathrm{ox}} + C_{\mathrm{si}} + C_{\mathrm{ss}}}{C_{\mathrm{ox}}} \tag{2}$$

$$V_{\mathrm{T}} = \frac{kT}{q} \tag{3}$$

The parameter η is subthreshold swing coefficient, and is calculated to between 1 and 3. The process parameters of oxide capacitance per unit area C_{ox}, surface depletion-layer capacitance C_{si} and interface-trapped capacitance C_{SS}. The parameter k is Boltzmann's constant, T is the absolute temperature in degrees Kelvin, and q is the absolute value of electron charge. In addition, transistor has a linear relationship between the transconductance and the drain current in subthreshold region. Thus, the transconductance to drain current ratio is maximized according to Eq. (5).

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} = I_{\mathrm{DO}} \frac{W}{L} \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_{\mathrm{T}}}\right) \times \left[1 - \exp\left(\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right] \frac{1}{\eta V_{\mathrm{T}}} = I_{\mathrm{D}} \frac{1}{\eta V_{\mathrm{T}}} \tag{4}$$

$$\frac{g_{\mathrm{m}}}{I_{\mathrm{DS}}} \approx \frac{1}{\eta V_{\mathrm{T}}} \tag{5}$$

Figure 2 shows the pixel arrays and column level circuits architecture with a level shift circuit. The photo current is integrated onto the integration capacitor which can be selected as 10 fF and 110 fF by S1 switch for different conversion gains in each pixel at the same time in snapshot mode. The CTIA transfers the charge in pixel to voltage signal, which will be sampled and held by the pixel S/H circuit consists of S2 and C3, and then be read out by the SF pixel buffer row by row with row pitch at 18 μm ×18 μm including a 6 μm × 6 μm mini pad, and the

minimum static current is even 8.5 nA per pixel in the proposed design due to single-terminal amplifier has one current branch. Thus, it benefits for realizing low power.

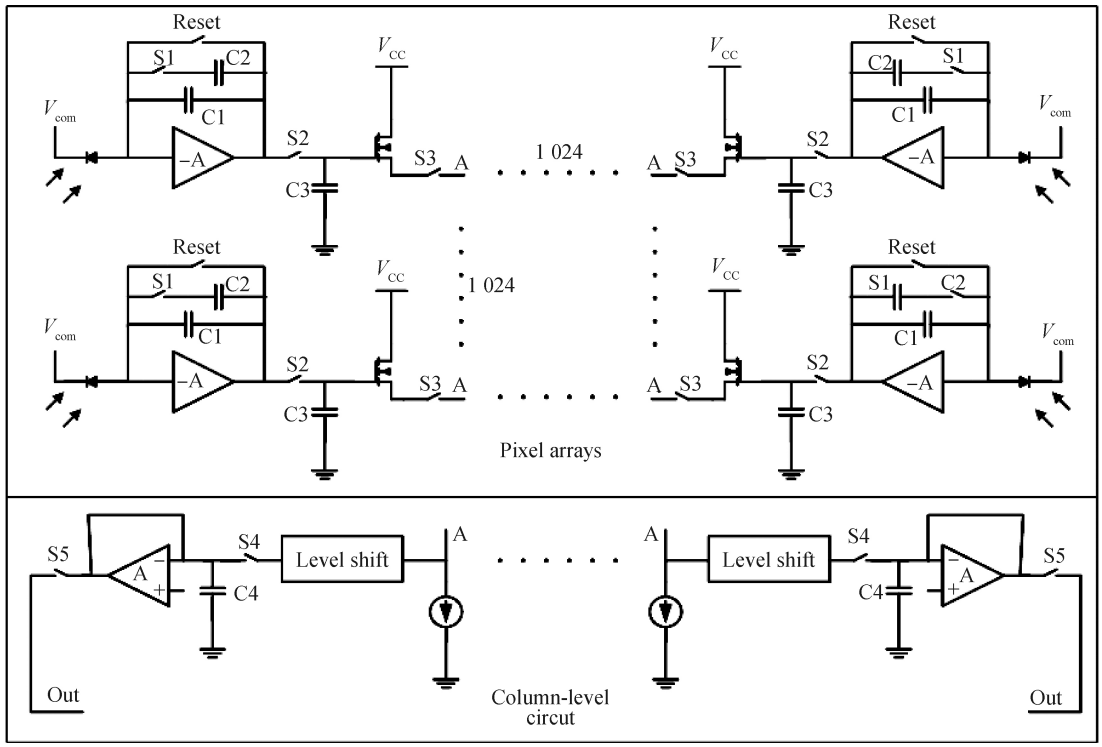

Fig.2 Pixel arrays and column level circuits

The column stage circuits include level shift, column S/H and column buffer circuit. The SF buffer in pixel unit shares a common current source load with other 1 023 pixel cells in the same column, and the pixel signal is transferred through SF buffer. Afterwards, the same current source is also used for level shift circuit, which compensates the voltage drop caused by SF buffer, to save lots of consumption, and thus becomes the second way to reduce power consumption. Compared to pixel S/H circuit which isolates outputs among pixels and get more flexible readout mode, the column S/H and column buffer circuits separate the column output from all pixel outputs to achieve low noise performance.

The third method to decrease power dissipation is the novel design of column buffer, which is shown in Fig.3. In the proposed design, the power control switch S6 is adopted, where is in the branch of current mirror to control the tail current I_0. The tail current source of column amplifier is divided into two parts, one is I0 and the other is I_1, which I_0 is much bigger than I_1. When the column selection switch is latched on and delivered pixel signal normally, the switch S6 is latched on simultaneously, both branches provided current with the sum of I_0 and I_1 to amplifier. When the column selection

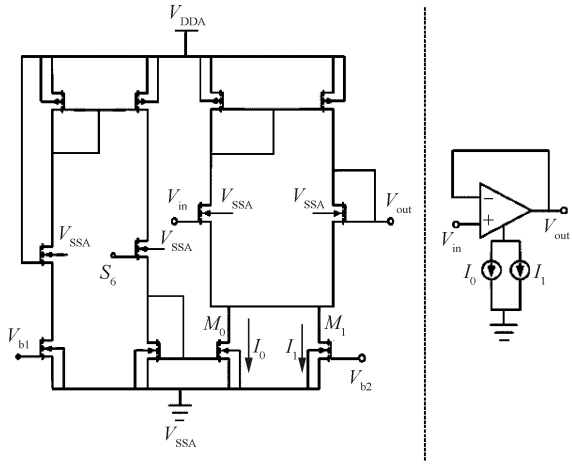

Fig.3 Design of column buffer circuit

switch is latched off and the switch S6 is latched off at the same time, the branch circuit of large tail current I_0 is closed, and only the small current I_1 is left to supply for amplifier. The value of I_1 is only 190 nA calculated by Eq.(1), and to make sure the NMOS transistor of M1 working in the saturation region, the bias voltage V_{b2} is a little bit higher than V_{TH} and the channel length is larger than the width of M1. In this way, the proposed column amplifier can greatly reduce the power consumption of the whole chip.

$$I=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs}-V_{TH})^2(1+\lambda V_{ds}) \tag{6}$$

Generally, these methods were introduced in UVFPA readout circuit to realize low power consumption for large format arrays. Meanwhile the ROIC also supports bias current adjustments to optimize power dissipation for better performances. The ROIC has a 3-bit digital-to-analog converter (DAC) on chip which generates adjustable bias-current for allover chip. Fig.4 shows the architecture of whole chip bias supply, DAC on chip decided the master bias supply by control bits B_{01}-B_{03}. Three switches B_{11}-B_{13} which is used to control power dissipation with the master bias current for the CTIA amplifier bias in the unit pixel. While another switches B_{21}-B_{22} to adjust bias currents for the analog signal path including level-shift, column buffer and output buffer circuits.

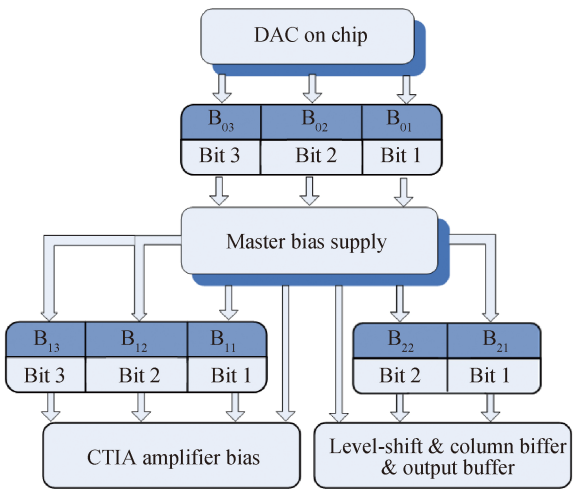

Fig.4 Architecture of whole chip bias supply

The total power consumption can be calculated in Eq. (2).

$$\begin{aligned}P_{total}=&M\times N\times P_{pixel}+M\times N\times P_{sf}+M\times\\&P_{column}+n\times P_{output}+P_{bias}+P_{logic}=\\&M\times N\times P_{pixel}+M\times N\times P_{sf}+M\times\\&(P_{ls}+P_{cb})+n\times P_{output}+P_{bias}+P_{logic}\end{aligned} \tag{7}$$

Where P_{pixel} is the power of per pixel; P_{column} is the power of output-stage; P_{bias} is the power of current bias circuit; P_{logic} is the power of digital control circuit which can be ignored; P_{column} refers to power of one column-stage circuit which contains SF power P_{sf}; level-shift power P_{ls} and column buffer P_{cb}. M is column and N is row that both of them are equal to 1 024 in this ROIC. There are totally 8 output buffers in this design and every 128 column shares an output buffer, so n equals 8 in this equation. As mentioned in this equation we can see that the most part of power dissipation comes from pixel arrays and the lower power of the pixel, the lower power of the whole chip.

$$\begin{aligned}P_{total}=&M\times N\times P_{pixel}+M\times P_{sf}+M\times\\&(P_{ls}+P_{cb})+n\times P_{output}+P_{bias}+P_{logic}=\\&M\times N\times P_{pixel}+M\times(P_{common}+P_{cb})+n\times\\&P_{output}+P_{bias}+P_{logic}\end{aligned} \tag{8}$$

The novel design of common current source load for SF buffer in pixels and level shift circuits is used to decrease power consumption for this ROIC, the total power consumption can be changed to calculated in Eq. (8). Compared to Eq.(7), the power of P_{sf} reduced significantly.

Table 1 gives a comparision of power consumption in the previous paper[11] and this paper.

Tab.1 Comparision of power consumption

Parameter	Previous[11]	This paper
Array format	128×128	1 024×1 024
Pixel current/nA	499	8.5
Total power consumption/mW	49.2	67.3

Compared to that, the pixel current reduces from 499 nA to 8.5 nA after optimizing design, which improved the power consumption for large pixel arrays

application. What is more, the total consumption is also reduced greatly in Tab.1.

3 Experimental results

The UVFPA readout circuit is designed and fabricated in SMIC 0.18 μm 1P6M mixed signal process with 3.3 V supply. Figure 5 shows the die photograph of 1 024×1 024 pixels format UV FPA ROIC chip, which the die size is 19.30 mm×20.17 mm. The 1 024×1 024 pixel detector arrays with 18 μm×18 μm pixel pitch would connect this ROIC chip that take the 2×2 pixels mirror symmetry layout as a unit layout, together through Indium with 6 μm× 6 μm mini pad.

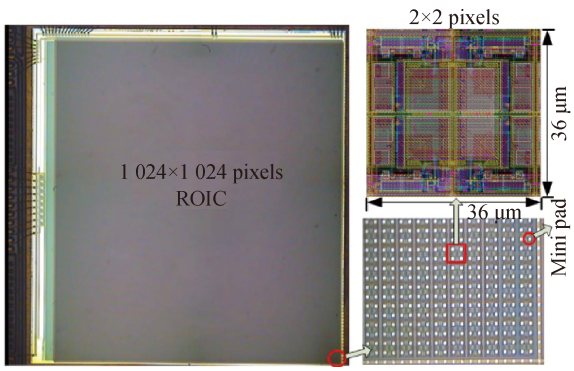

Fig.5 Die photograph of ROIC chip

Figure 6 shows the test platform, which consists of DC power supply, serial data timing generator, digital oscilloscope, acquisition card and PCB board of test. As mentioned in section2, the minimum current of the whole chip is 20.4 mA at 2 MHz readout rate with 3.3 V power supply, so the total power consumption is only 67.3 mW due to apply those modified design in ROIC.

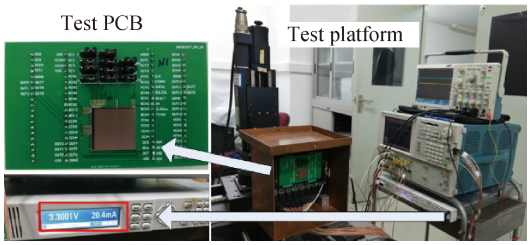

Fig.6 Test platform of the ROIC chip and test result

The measurement results of 1 024×1 024 ROIC with eight outputs by acquisition card NI6366 are shown in Fig.7. Meanwhile the raw data come from acquisition card are made in an intensity graph of all frame are also illustrated.

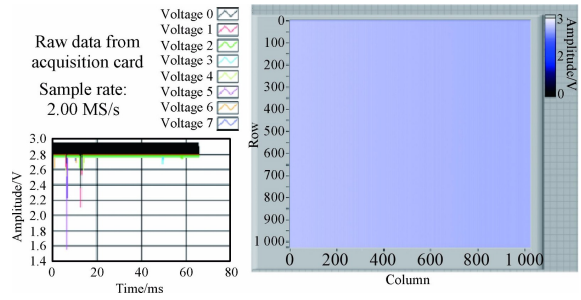

Fig.7 Measurement results of 1 024×1 024 ROIC with eight outputs by acquisition card

The performances include operate mode, output swing range, integration capacitor charge capacity and power supply, etc. The summarized specifications of the 1 024×1 024 readout circuit are detailed in Tab.2. It can be seen that the ROIC makes two gain selections with 10 fF and 110 fF integration capacitors which charge capacities are 0.11M*e*- and 1.23M*e*- respectively per pixel with 1.8 V output range.

Tab.2 ROIC of UVFPA specifications

Parameter	Measurement
Array format	1 024×1 024
Pixel size	18 μm×18 μm
Operate mode	Snapshot
Pixel current/nA	8.5
Power consumption	67.3 mW @2 MHz
Frame rate	15 Hz(limited by speed of acquisition card)
Integration capacitor Charge capacity	0.11 M*e*- at 10 fF &1.23 M*e*- at 110 fF
Output swing/V	1.8
Power supply/V	3.3
Chip area	19.30 mm×20.17 mm

4 Conclusion

In this paper, these methods are adopted to optimize power consumption for UVFPA readout circuit, which are single-terminal amplifier with static current 8.5 nA as CTIA amplifier, common current

source load for SF buffer in column pixels and level shift circuits, and time-sharing tail current source for column buffer. As well as, the UVFPA ROIC has a format of 1 024×1 024 and pixel pitch of 18 μm with 10 fF and 110 fF selectable integration capacitors with a variable integration time. Meanwhile, the ROIC operates in snapshot integration mode which has Integrate-Then-Read (ITR) and Integrate-While-Read (IWR) read modes respectively. Above all, the ROIC accomplished an ultra-lower power consumption of 67.3 mW at 2 MHz all frame rate in a 1 024×1 024 FPA with 3.3 V supply voltage. What's more, it has been fabricated in SMIC 0.18 μm 1P6M mixed signal process and achieved better performances.

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