Design of high-speed image transmission system based on FPGA

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Abstract: The high-speed digital image transmission method for high speed camera is proposed, in order to overcome the current approach to long distance image transmission technology by LVDS. It can decrease the requirement of cable quality and system complexity, and be unnecessary of data relay. FPGA was used as the main controller. The received image data of LVDS format was changed into the signal of TTL format, and then was stored into the appointed location. Then the image data was transmitted by optical fiber after the high-speed serial data was gotten by RocketIO. The bit-error number was zero when 32 Gbit data is transmitted at the rate of 1.6 Gbps. The result shows that the method has the advantage of low bit-error rate, simple system design, excellent performance and convenient expansibility.

Key words: high-speed image transmission; FPGA; RocketIO; LVDS

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基于 FPGA 的高速图像传输系统设计

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摘 要: 提出一种多相机的高速图像传输方法,以克服目前采用 LVDS 方式进行长距离图像传输技术存在的所需线缆数量大、同时需要进行数据中继、系统的复杂度高的缺陷。系统采用 FPGA 为主控制器,将接收到的高速相机发出的 LVDS 格式图像数据转换成 TTL 信号,并分别输入到指定的存储区中。将相应存储区中的图像数据进行打包处理,送入 RocketIO 中转换为高速串行数据后,利用光纤进行远距离传输。实验表明,该方法在 1.6 Gbps 的传输速率下,传输数据量为 32 Gbit 时,误码数为零,且系统设计简单、性能优良,具有较强的可扩展性。

关键词: 高速图像传输; FPGA; RocketIO; LVDS

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0 Introduction

With the continuous improvement of electronic technology, the current imaging mode has moved from film to digital development. The CCD(charge-coupled device) or CMOS image sensors have been adopted. The sensor pixel sizes are becoming smaller, while the image read speed is faster. Therefore, the image data amount generated by the camera is getting larger, which brings great pressure for the subsequent image transmission. Although their imaging and driving principles are different, their data processing methods are basically uniform. The CCD sensor in terms of imaging performance is better than the CMOS sensor, so they are applied extensively, especially high-tech domains. This paper will study complicated imaging transmission system based on CCD digital cameras.

The output interface of high-speed digital camera mainly adopts two ways, Camera link mode and LVDS (low voltage differential signal) mode. The LVDS transmission mode is widely used because of some advantages of simplification, low cost etc. Multiple CCD cameras are working at the same time in the precision measurement, industrial control, space remote sensing and other high-tech fields. The captured images need be analyzed and calculated totally, then the equipment is controlled according to the results. If the LVDS mode is adopted for long distance image transmission, the demands of the cable will be greatly increased, the complexity and development cost of the system will be greatly improved, but the reliability is greatly reduced. This paper presents a method of multiple digital cameras image transmission based on high-speed serial communication technology in order to overcome the existing defects of the LVDS mode for long distance image transmission[1–3].

1 High-speed digital image transmission system

1.1 High-speed serial communication technology

High-speed serial communication technology merges the clock and data to transmit and overcome the problem of clock jitter and data jitter. No clock controlling signal can greatly increase the transmission speed, reduce the peripheral IC pin count and power consumption, and obtain better signal integrity. There are two methods to realize high-speed serial communication technology, and their principles are the same. One is processor and dedicated SERDES chip, the other is FPGA with embedded SERDES module. This paper uses V Ⅱ P40 produced by Xilinx Inc , which is FPGA with SERDES module. This method can not only speed up the development progress, but also save development cost. And if the system is changed to use the way of the processor and dedicated SERDES chip, transplant procedure is very convenient[4–5].

1.2 System design

This paper studies an image data transmission method of six CCD cameras working simultaneously. The transmission rate of every CCD camera is 100 Mbps using three wire LVDS mode, namely through the clock signal(Clock), the data signal(Data) and enable signal (En) to complete the image signal transmission, as shown in Fig.1. After the system is reset, the image transmitting terminal has been sending clock signal to ensure that the image sender and the image receiver is synchronized. When the cameras are working, the enable signal is set, and immediately the image is sent in accordance with the image data transmission protocol.

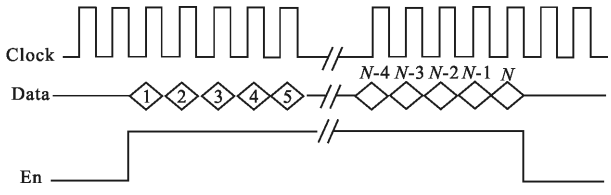

Fig.1 Image transmission format by LVDS

The image transmission system mainly consists of the LVDS receiving module, receiving data cache, control unit, MGT unit, fiber channel transmission module, communication unit and monitoring unit etc.,

the block diagram is shown in Fig.2. The receiving image of LVDS mode is converted to TTL signal by the LVDS receiving module. The receiving data cache adopts ping-pong structure to buffer the received image data using on-chip RAM of FPGA. When the receiving data reaches the set number of bytes, it sends a request signal to control unit. The control unit is the heart of whole system. The parameters are set according to the receiving data through external communication interface. It can complete the management of every data stream and the processing of packaging data stream, control the MGT unit. The MGT unit can convert 16 bit parallel data into high-speed serial data and encode the data. The fiber transmission module is to convert electrical signals into optical signals. The state monitoring unit is to monitor the status of system for system maintenance and remote diagnosis. The communication unit is that it sets the system parameters according to the communication protocol. The system uses the RS-422 communication mode[6].

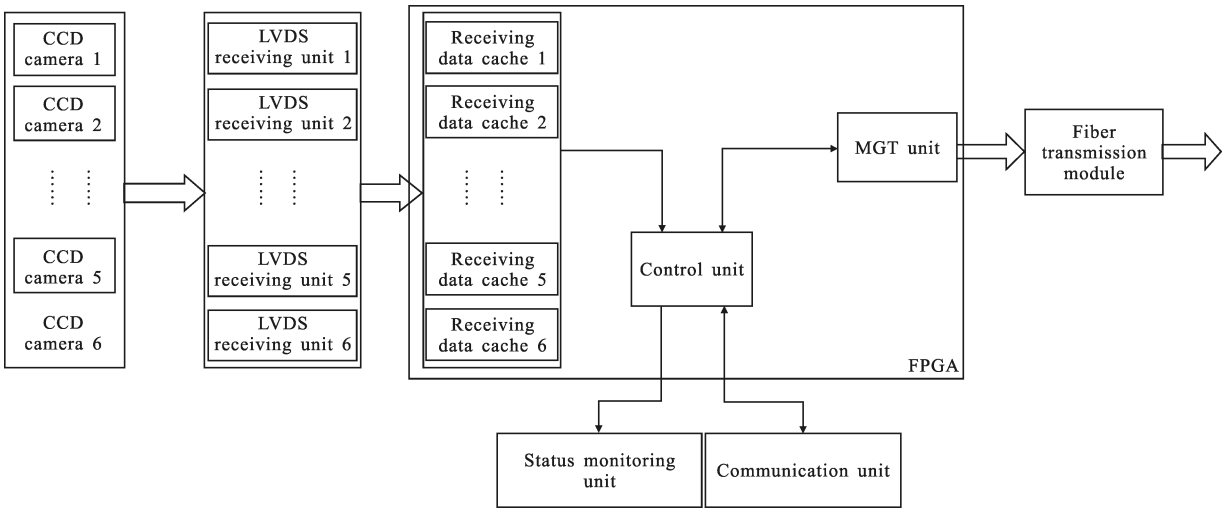

Fig.2 Function block diagram of image transmission system

When the digital cameras are transmitting the image data, the difference image data will be converted to TTL signal by the LVDS receiving module, and stored in the specified data receiving cache. When the receiving data achieve 64 bytes (according to the actual situation, the number of bytes of data cache is set), it sends the "full" request signal to the control unit. The control unit makes corresponding channel flag "1". According to the "first priority" principle, the request signals are queued, the data is sent into the MGT unit in turn. The MGT unit converts the image data into serial differential signals through 8B/10B encoding and clock correction, then sends the data into the fiber transmission module. The fiber transmission module converts the receiving signals into optical signals and transmits by optical fiber. After one frame is sent completely, the system will make the corresponding channels flag "0" and begin to deal with the next frame.

2 Experiments

FPGA is used as the controller of the experiment, which realizes the system configuration, data caching, data integration, high-speed serial-parallel conversion, encoding and other functions. The single mode fiber of 1310 nm is selected as transmission medium. The experiment 1 and experiment 2 are designed in order to verify the reliability and performance of system[7-8].

2.1 Experiment 1

A sequence of data is designed separately as the single data source. The data is continuously

transmitted for the bit error rate experiment. The block diagram of experiment is shown in figure 3. After the power initialization of FPGA is completed, the circle data packets by the sending data cache are transmitted continuously. The length is 2 KB. The MGT unit converts the data packet into high-speed serial data. Then the optical signals are gotten by the sending fiber module and sent through a single-mode fiber. The receiving fiber module converts the receiving optical signals to electrical signals, and sends into the MGT unit of the FPGA. Then they are transformed to 16 bit parallel data and stored in the receiving cache. The data checkout unit compares the receiving data with sending data. If they aren′t consistent, error register is accumulated automatically. The error number of the register is sent to the computer through the RS-422 bus when the experiment is over.

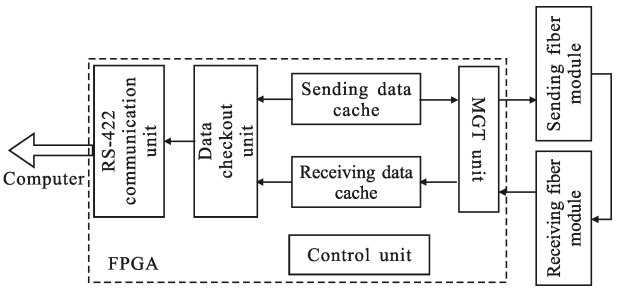

Fig.3 Block diagram of high-speed data communication experiment

The experiment conditions and results are as follows:

Data transferring rate: 1.6 Gbps;

Sending mode: continuous cyclic transmission;

Number of sending data: 32 Gbit;

Error number: 0.

2.2 Experiment 2

The simulation image is designed, and its format is consistent with the original image. A frame of image consists of 512 columns, a line includes 4 096 pixels[9]. Because the simulation image is very large, they are intercepted and the front are displayed, as shown in Fig.4 (a). The image is accepted and displayed by the image acquisition card of the computer. The receiving image is as shown in Fig.4(b)(The first 32 bytes are the image aided information). Comparing with two images, they are clear, coincident, satisfied with the design requirements.

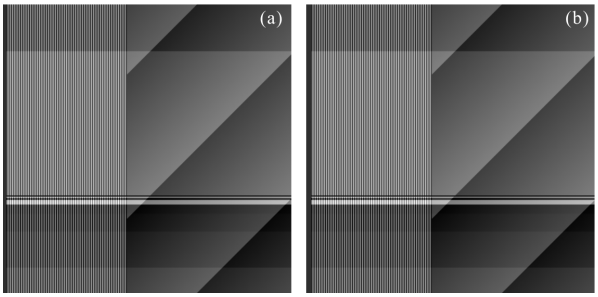

Fig.4 Experiment of high-speed image data transmission system

3 Conclusion

The output images of digital cameras (LVDS mode) are integrated and converted into high-speed serial data. Then they are sent by the optical fiber to realize long distance transmission. This method needn´t relay data, can reduce the quantity and quality of transmission cables, and lessen the bit error rate of complexity and data transmission. At the same time, it can improve the maintainability and expansibility of the system. Because of FPGA as the main control chip, using the on-chip SERDES module and block RAM resources, it can eliminate external chips, simplify the design of the system and save the time and cost of development system. Through the experiment, we found that the method can satisfy the requirements of complex high-speed data image transmission system, and have high practical value.

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