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Damage characteristics and physical mechanism of the CMOS inverter under fast-rising-edge electromagnetic pulse*

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Abstract: Ensuring the reliability of integrated circuits (ICs) has been a great challenge with the increasing complexity of the electromagnetic environment. On this basis, the fast-rising-edge electromagnetic pulse (EMP)-induced trap-assisted tunneling (TAT) effect is investigated by simulation and experiments of CMOS digital inverters. A detailed mechanism analysis is performed to explain the physical damage process. The EMP-induced field derives traps and leakage current in the oxide, which induces output degradation and thermal failure in the device. A theoretical model of degradation and failure is established to describe the dependency of the output deterioration and the heat accumulation on the EMP resulting signal features. The temperature distribution function is derived from the heat conduction equation in the semiconductor. Corresponding experiments performed based on the TLP test system substantiate the emerging performance deterioration, which is in agreement with the mechanism analysis. Simulated results from the Sentaurus TCAD indicate that EMP resulting voltage-induced damage is caused by the TAT current path occurring in the gate oxide, revealing the location susceptible to burnout. In addition, the dependency of the device failure on the pulse rising time is discussed. The mechanism analysis in this paper facilitates reinforcing the design and promotes EMP reliability research on other semiconductor devices, and the study contributes to the enhancement of EMP robustness in CMOS digital ICs.

Key words: CMOS inverter, electromagnetic pulse, trap-assisted tunneling, mechanism analysis

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With the increasing complexity of the electromagnetic environment, the risk to electronic systems from EMPs (electromagnetic pulses) is also increasing[1-4]. The same type of high-intensity electromagnetic radiation induced by a nuclear explosion or EMP weapon can affect electronic systems through nonartificial methods (such as electrostatic discharge, lightning strikes and internal switching surges) and cause degradation and damage to the chips[5-7]. CMOS digital circuits are widely used in ASIC (application specific integrated circuit) and FPGA (field programmable gate array) applications due to their advantages of low power and wide operating voltage. Therefore, the damage mechanism analysis of CMOS inverters under a complex electromagnetic environment is extremely significant.

In recent years, much attention has been paid to the EMP effect in ICs (integrated circuits). Kim *et al* studied high-power microwave-induced degradation in CMOS circuits[8-10]. Experiments on MOSFET devices and digital logic circuits under high-power microwave radiation were performed in Ref [11]. Studies in Refs.[12, 13] reported hard upsets and catastrophic physical failures in CMOS digital inverters under high-power microwave (HPM) interference. SPICE modeling and simulation of CMOS inverters has been carried out under high-power microwave radiation[14-15]. A study in Refs.[16-20] revealed the physical mechanism of the latch-up effect in a CMOS device under the interference of high-power microwaves. For circuits under a fast-rising EMP resulting signal, the damage mechanisms of bipolar and high-electron-mobility transistors (HEMTs) have been reported in Refs. [21-25]. There are few reports on rapidly rising EMP-induced degradation (or damage), and more attention has been paid to the damage effects of HPM-radiated CMOS devices. The study of EMPs favors bipolar and HEMTs due to the established gate-damage model. However, the damage effect of CMOS inverters under fast-rising-edge EMP resulting voltage

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signals must be studied because emerging defects and thermal failure occur in the oxide layer and determine the robustness of the ICs.

In this paper, an oxide-damage model of CMOS inverters is first established to perform damage mechanism analysis under an EMP resulting voltage signal. The paper is organized as follows. Section 1 presents the mechanism analysis and the theoretical damage model established with the built CMOS device model. Section 2 analyzes the experimental results and simulation results.

1 Damage mechanism analysis and theoretical damage model

1.1 Device structure and simulation setup

Fig.1 shows the schematic diagram of the studied cascaded CMOS inverters. A device model is established to approach the actual layout of CMOS digital chips. This model is built on CMOS-lambda-design rules, with λ = 0.175 μm. The device model has a thickness of 4 μm, a width of 10.5 μm, and the gate distance between NMOS and PMOS in the CMOS inverter of 5 μm. The NMOS gate width is 0.35 μm, and the PMOS gate width is 0.35 μm. The substrate and the N-well are lightly doped with boron (B) and arsenic (As), respectively, and the source and drain active regions are defined as heavily Gaussian doped. Q1 and Q2 indicate the parasitic bipolar transistors in the CMOS device, and R_{sub} and R_{well} represent the impedance of the p-type substrate and the N-well, respectively. The bottom edge of the model is set with an initial temperature of 300 K to imitate the actual heat dissipation conditions in the digital circuit, and the remaining boundaries are set as adiabatic. The corresponding electrode connection is plotted in Fig.1. In the simulation analysis, the input voltage (V_{in}) and the supply voltage (V_{DD}) are both set to 3.3 V. The CMOS inverters have a switching threshold voltage of 1.63 V, with a typical noise margin value of 0.4 V under normal operating conditions. The fast-rising-edge EMP resulting voltage signal is injected into the gate in NMOS and PMOS to simulate the back-door high power electromagnetic interference to the device[26].

1.2 The mechanism analysis of the TAT-induced damage

When the EMP resulting voltage signal is injected from the V_{in} port of the cascaded CMOS inverters, the trap-assisted tunnel (TAT) current[27] caused by quantum effects occurs in the oxide layer under an EMP resulting voltage signal-induced field, eventually leading to electrical property degradation and failure of the device. Fig.2 shows the mechanism of the TAT effect in the CMOS inverters under the impact of the fast-rising-edge EMP resulting voltage signal. Fig.2(a) explains the mechanism of the TAT effect in the energy band. In Fig.2(a), y indicates the distance between the defect level and the interface of the Au (M layer) and SiO_2 (I layer), and H is the thickness of the gate oxide layer. The emerging defect energy level E_{trap} increases the probability of tunneling. Low energy charge (Au) can reach high energy (Si) level through defect energy instead of direct tunneling. This process is called TAT effect. The physical process of TAT is shown in Fig.2(b). The EMP resulting voltage signal-induced strong vertical electric field in the gate causes defects in SiO_2, which causes extra E_{trap}. Thus, the electrons have a certain probability of tunneling from the M (Au) layer to the S (Si) layer with the intermediate defect energy level. Trap tunneling through the defect level causes the additional leakage current between the gate and the conditional channel of CMOS inverters, which is the so-called TAT effect. The current density of the tunneling current, $J_{leakage}$ is

$$J_{leakage} = \frac{I_{EMP}}{LW}\int_0^H \frac{P_{MI}(y,V_g)P_{IS}(H-y,V_g)}{P_{MI}(y,V_g)+P_{IS}(H-y,V_g)} N_T(y,E_{EMP})\sigma \mathrm{d}y \tag{1}$$

where I_{EMP} and E_{EMP} indicate the EMP resulting voltage signal-induced current and field, respectively, and L and W are the

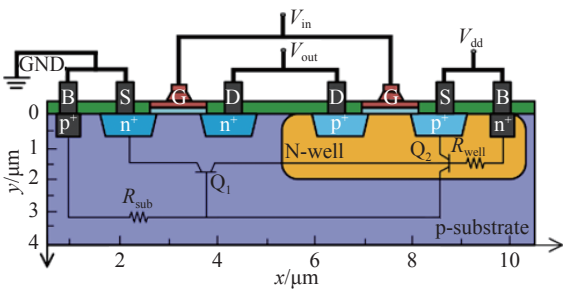

Fig. 1 Schematic diagram of the CMOS inverter

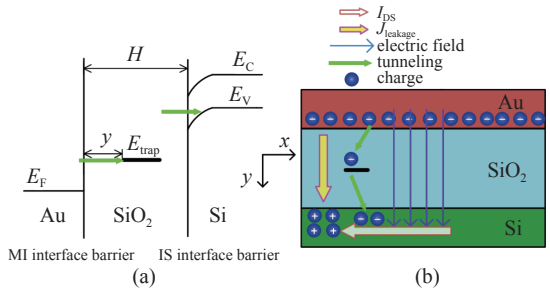

Fig. 2 The TAT effect in the oxide layer

width and length of the pMOSFET, respectively. P_{MI} indicates the TAT probability of the electrons from layer M to layer I, and P_{IS} is the tunneling probability from layer I to layer M. V_g is the input voltage. $N_T(y, E_{EMP})$ represents the defect distribution caused by EMP resulting voltage signal interference, which is considered a Gaussian distribution in energy and space. σ indicates the area of the single defect. The leakage current ($J^p_{leakage\text{-}S}$) in the NMOS region is derived by the gate-to-source field. The leakage current of the PMOS can be obtained by the gate-to-source and gate-to-drain fields, and the corresponding $J^p_{leakage\text{-}S}$ and $J^p_{leakage\text{-}D}$ occur in the source and drain. The EMP resulting voltage signal-induced TAT current causes an extra potential drop between the drain and source regions, ultimately leading to output level degradation of the CMOS device. The degradation in the output (high level) ΔV_{high} can be obtained according to the solution of $J^p_{leakage\text{-}S}$ and $J^p_{leakage\text{-}D}$,

$$\Delta V_{high} = \frac{L}{C'_{ox} W \mu_n \left(V_g - V_t\right)} \int \left(J^p_{leakage\text{-}D} + J^p_{leakage\text{-}S}\right) \mathrm{d}s \tag{2}$$

where C'_{ox} is the capacitance of the PMOS gate under the impact of EMP resulting voltage signal. μ_n indicates the mobility of the electrons, and V_t is the threshold voltage of the CMOS device. Similarly, the degradation in the output (low level) ΔV_{low} can be expressed by

$$\Delta V_{low} = \frac{L}{C'_{ox} W \mu_n \left(V_g - V'_t\right)} \int J^n_{leakage\text{-}S} \mathrm{d}s \tag{3}$$

where ΔV_{high} and ΔV_{low} describe the degradation in the output characteristics of the CMOS device. The increment in the leakage current under EMP resulting voltage signal induces worse degradation in the output level. Thus, the extra gate leakage current in the PMOS drain causes more severe degradation in the output high level than NMOS. Based on the extra leakage current ($J_{leakage}$) described above, the accumulated carriers in the source can be obtained, and they are the dominant factor for the thermal failure in the CMOS device with increasing EMP resulting voltage signal voltage. The TAT current and the drain-to-source current cause a charge to accumulate in the source of NMOS and PMOS, achieving rapid heat accumulation under a stronger EMP resulting voltage signal-induced field. Thus, the theoretical heat-accumulation[28, 29] model can be established as:

$$W(t, V_{EMP}) = (1+\beta)\overrightarrow{E_{EMP-y}} \int_0^H \left[\frac{\overrightarrow{V_{EMP-y}}}{LW} \frac{P_{MI}\left(y, V_g\right) P_{IS}\left(H-y, V_g\right)}{P_{MI}\left(y, V_g\right) + P_{IS}\left(H-y, V_g\right)} N_T\left(y, E_{EMP}\right) \sigma \right] \mathrm{d}y \tag{4}$$

where t represents the rising time of the pulse. V_{EMP} is the transient EMP voltage, and $E_{EMP\text{-}y}$ indicates the EMP resulting voltage signal-induced vertical electrical field in the gate. β is an experimental parameter to describe the charge provided by the drain-to-source current. Obviously, the heat accumulation of the PMOS source is the maximum because the extra leakage current path emerges between the gate and drain, providing extra charge density in the source. Under the impact of the fast-rising EMP resulting voltage signal, the speed of the heat accumulation can be approximately described by $\partial W/\partial t$. There is a rate discrepancy under rising and steady pulses. The rate in the rising phase can be expressed by $(\lambda + \chi t)$, where χ indicates the derivative of $E_{EMP\text{-}y}$ with respect to t. However, χ under a steady EMP resulting voltage signal decreases to 0. Thus, the heat accumulation in the rising process of the pulse is the most significant factor in thermal failure. The device under the EMP resulting voltage signal has dominant heat accumulation in the rising process of the pulse, considering the heat dissipation of the substrate. By substituting the heat accumulation Eq. (4) to the heat conduction equation (Eq. (5)), the temperature distribution function $T(\boldsymbol{r}, t)$ can be obtained.

$$W(t, V_{EMP}) = C(T) \frac{\partial T(\boldsymbol{r}, t)}{\partial t} - \kappa(T) \nabla^2 T(\boldsymbol{r}, t) \tag{5}$$

In Eq.(5), T indicates the lattice temperature in the device, and $C(T)$ and $\kappa(T)$ are the coefficients of melting and heat conductivity, respectively. Obviously, the failure of the device under EMP resulting voltage signal is determined by the EMP voltage and the rising edge, which are strongly related to V_{EMP} and t. A detailed analysis will be given in the following discussion.

2 Results and Discussion

2.1 Experiment setup and results

Based on the Celestron TLP test system of Thermo Scientific, a fast-rising-edge EMP resulting voltage signal experimental

environment is established. Fig.3 shows the schematic of the experiments. The EMP resulting voltage signal parameters and the relay status are set by the terminal-controlled PC, which monitors the injected EMP resulting voltage signal waveform. A high-voltage pulse power supply is used to produce the pulse to simulate the EMP resulting voltage signal. The fast-rising-edge (from 0.2 ns to 2 ns) EMP resulting voltage signal from transmission lines L1 (pulse forming line) and L2 (pulse transmission line) are injected into the input port. The injected EMP resulting voltage signal voltage and the corresponding current waveforms of the device are monitored on oscilloscope1 (Tektronix 3054C). To ensure that the CMOS device is under normal bias, the reserved port on the test PCB is supplied by the DC source (Agilent E3649A). Oscilloscope2 (Keysight 3054T) is used to monitor the corresponding output voltage and current of the CMOS inverter under EMP resulting voltage signal, assisting the failure analysis of the CMOS device during the experiment. The CMOS inverter CD4069UBCN6 is selected to be tested. The PCB design tool Altium Designer is utilized to design a single inverter test circuit dedicated to the EMP resulting voltage signal experiments, as shown in Fig.4(a). The output port is connected with a protective resistance and an LED (light-emitting diode), which directly reflects the output state of the CMOS inverter and is used for rapid judgment of failure during the experiment. The test scenario is shown in Fig.4(b), Fig.4(c) shows the physical drawing shall of the test circuit.

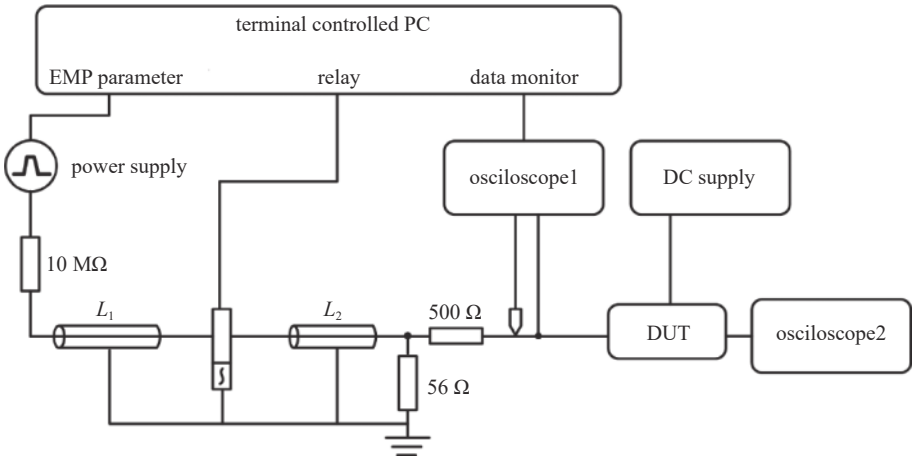

Fig. 3 Schematic of the fast-rising-edge EMP resulting voltage signal experiment based on the TLP testing system

(a) Photo of the tested PCB (b) Experimental platform and environment (c) The physical drawing shall

Fig. 4 Injection experiments of EMP resulting voltage signal with fast rising edges

The *I-V* chart of target chip using TLP test equipment is shown in Fig.5. The *I-V* chart is shown in the red curve. The leakage current dependency on the TLP voltage is shown with the green curve. When the EMP resulting voltage is small, the leakage current of the CMOS inverter will not change. When TLP voltage reaches a certain value, leakage current (green curve) surges. This phenomenon is consistent with the description of Eq. (1). When the voltage increases further, the gate-oxide of the inverter shows breakdown characteristics until the device burns out and the leakage current of the device drops to 0. The *I-V* characteristics of TLP pulses firstly drift in the negative direction and then in the positive direction during the pulse stepping process. Second, the reverse leakage current of the DUT will surge based on the increasing amplitude of the electromagnetic pluse.

According to the experimental environment described above, chip A is injected by EMP resulting voltage signal with a positive voltage of 650 V and a short current of 19 A, and chip B is injected by EMP resulting voltage signal with a 1200 V voltage and a 27 A short current, both sharing a rising edge of 0.2 ns. Chip C is injected by 650 V voltage EMP resulting voltage signal, with the rising edge of 2 ns, and the short current is 19 A. The supply voltage V_{DD} is set to 5 V, and the input of

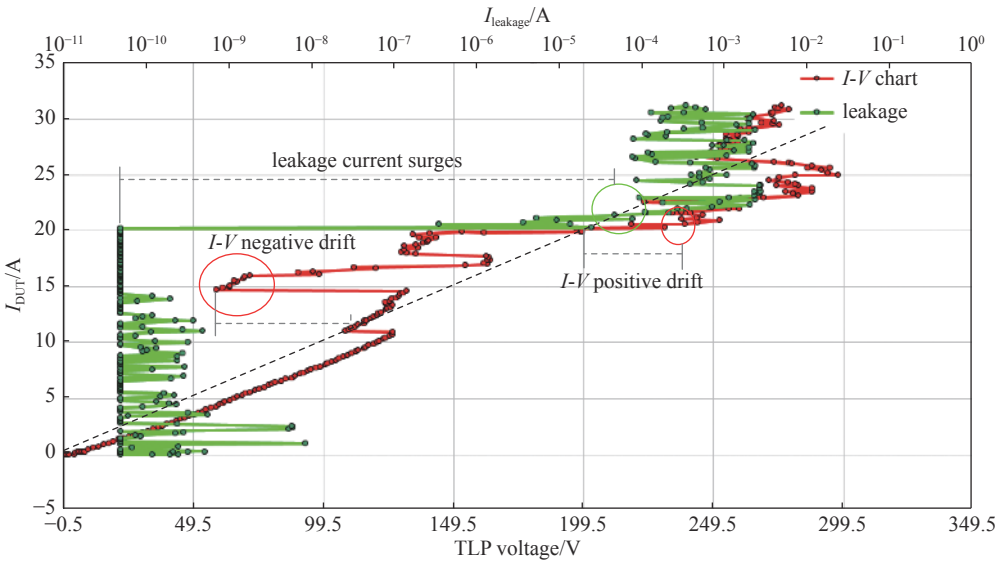

Fig. 5 Typical TLP current-voltage characteristic curve and reverse leakage current curve of type A sample

the inverters V_{in} is represented by a square wave to simulate the working state of the digital circuits, with a voltage of 5 V and a frequency of 100 kHz. Fig.6 shows the output damage transients of the target chip under fast-rising EMP resulting voltage signal. This can be described by $\Delta V_{A\text{-high}}$, $\Delta V_{B\text{-high}}$ and $\Delta V_{C\text{-high}}$ with the comparison of the chips under EMP resulting voltage signal (dark blue line, red line and light blue line) to the chip working well (black line). $\Delta V_{A\text{-high}}$ and $\Delta V_{A\text{-low}}$ indicate the degradation of the device under a 650 V EMP resulting voltage signal without losing the reverse function. However, poor reverse failure occurs with increasing fast-rising-edge EMP resulting voltage signal amplitude (1200 V). The output level degradation dependencies on the EMP resulting voltage signal rising edge is described by chip A and chip C ($\Delta V_{A\text{-high}}$ and $\Delta V_{C\text{-high}}$, $\Delta V_{A\text{-low}}$ and $\Delta V_{C\text{-low}}$). The more serious output level degradation emerges under EMP resulting voltage signal with shorter rising edge (light blue line). Therefore, there is a rising time discrepancy at the high and low levels, as marked by the dashed red lines. The faster rising time occurs in the reverse process of high-to-low level for the difference of the leakage current in PMOS ($J^{p}_{leakage\text{-}S}$ and $J^{p}_{leakage\text{-}D}$) and NMOS ($J^{n}_{leakage\text{-}S}$). The experimental results well support the previous damage mechanism of TAT in the CMOS device under EMP resulting voltage signal.

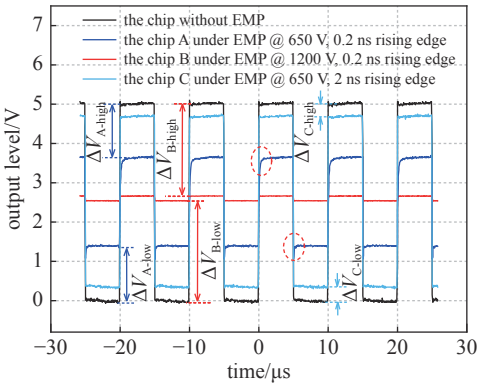

Fig. 6 Tested output level of the CMOS inverter

2.2 Simulation verification and discussion

2.2.1 The output degradation of the CMOS device

The output level transients of the CMOS circuits under EMP resulting voltage signal are simulated in a Sentaurus TCAD. Taking the 0.35 μm process-related CMOS inverters in Subsection 1.1 as a comparison (without EMP resulting voltage signal), the damage device model under EMP resulting voltage signal is established. The SiO_2 layer in the NMOS and PMOS is doped with traps (donor and acceptor traps) in the device to simulate the defects in the oxide. The peak concentration of the Gaussian is defined in the middle of the oxide layer. Fig.7 shows the influence of the trap concentration on the output level degradation under a lower EMP resulting voltage, with a rising edge of 1 ns, peak voltage of 3.3 V and frequency of 250 MHz. The EMP effect on the device can be represented by the extra trap density in the oxide layer. Based on the TAT model in Sentaurus TCAD, we carried out the output characteristics simulation with various trap concentrations. Fig.7(a) describes the input voltage V_{in} of the injected EMP resulting voltage. Fig.7(b) shows the output level of the CMOS inverters with various trap concentrations. The black line indicates the output level of the ideal device. The established circuit model works well without gate defects under lower EMP resulting voltage. The other plots describe the output transients of the damage device model

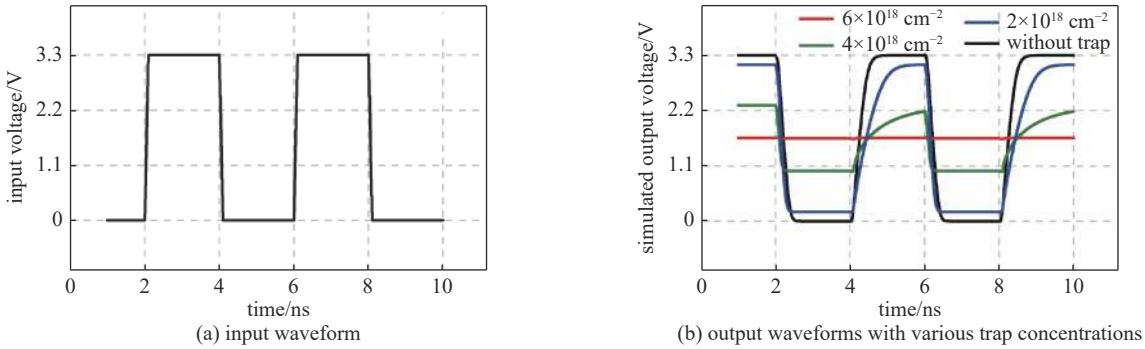

Fig. 7 Simulation results of the CMOS device under EMP resulting voltage signal

under EMP resulting voltage signal. As the trap concentration increases from 2×10^{18} cm^{-2} to 6×10^{18} cm^{-2}, the output level attenuation of the CMOS inverters rises. Sharing the same EMP resulting voltage, more injected defects in the oxide layer accelerate the output degradation due to the greater leakage current in Eqs. (2) and (3). The red line explains that the inversion of the device eventually fails. There is an obvious discrepancy in the output degradation of NMOS and PMOS because the bias (V_{dd}) derives extra leakage current in the drain. The simulation results basically coincide with the previous mechanism analysis in Fig.6, which indicates that the emerging traps of the oxide lead to degradation in the output level of the CMOS inverters under EMP resulting voltage signal.

Fig.8 shows the internal current density distribution of the CMOS inverters under EMP resulting interference, with a rising edge of 1 ns and various voltages. Figs.8(a), 8(c) and 8(e) describe the current density of the NMOS region under EMP resulting voltage signals of 0 V, 5 kV and 10 kV, respectively. Figs.8(b), 8(d) and 8(f) plot the corresponding current distribution in the PMOS region. Comparing Figs.8(a), 8(b) and 8(c), the gate current in the oxide layer continues increasing and derives the conductive current path between the gate and source under $E_{\text{EMP-S}}$ with increasing EMP resulting voltage. A similar conclusion can be drawn from the leakage current contrast in the PMOS gate. The carrier accumulated by the drain-to-source current IDS is observed with the maximum current density, as shown in regions R1 and R2. Therefore, the discrepancy referring to the output of NMOS and PMOS in Fig.6 can be explained by the difference in J_{leakage} of NMOS and PMOS. The gate-to-drain field $E_{\text{EMP-D}}$ in the PMOS region leads to extra leakage current between the gate and drain in the R3 region. Thus, poor degradation appears in the PMOS for the greater gate leakage current, and the output characteristics penalty is the maximum. This explains the longer rising time for the 0–1 transition in PMOS. The simulated threshold voltage is greater than the result (1200 V) in the experiment due to the established ideal model.

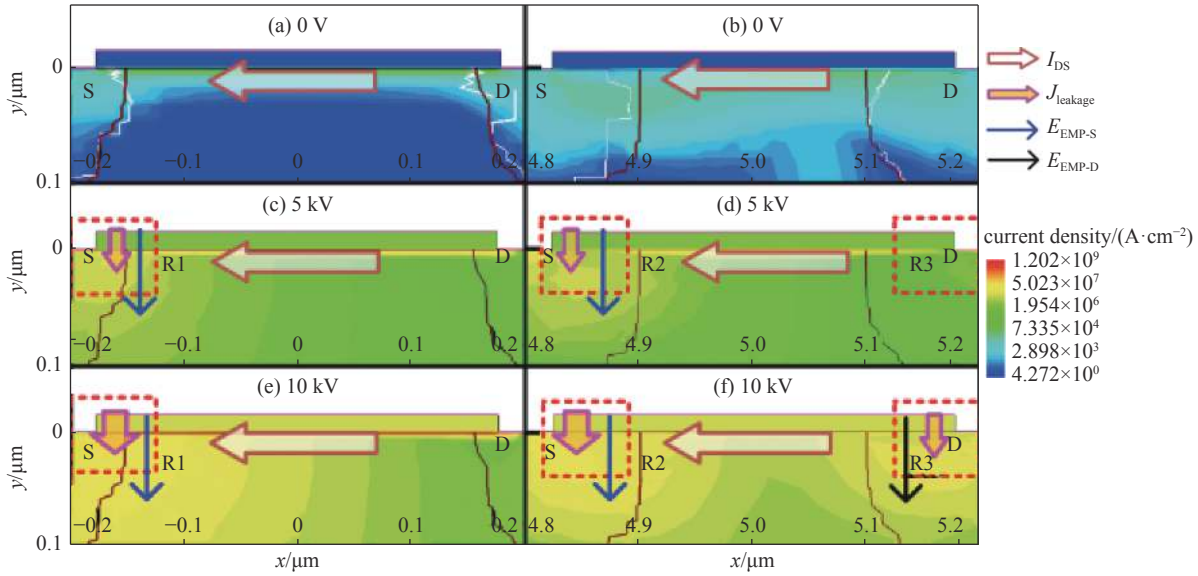

Fig. 8 Simulated current density under EMP resulting voltage signal. Detailed current distribution of the NMOS region under (a) 0 V, (c) 5 kV, and (e) 10 kV. The corresponding current of the PMOS region is shown in (b), (d) and (f)

2.2.2 The TAT effect-induced thermal damage

Fig.9 shows the thermal damage transient in the CMOS inverters under exponential pulse interference, with a rising edge of 0.2 ns and voltage of 12 kV. The threshold lattice temperature of the device is set to 1960 K, the melting point of the SiO_2 layer. The detailed temperature distributions of the NMOS and PMOS regions are shown in Fig.9. Because the gate-to-drain current provides extra charge in the PMOS source, both the carrier density and heat here are maximum rather than the source of NMOS. Thus, thermal failure occurs in the PMOS oxide layer first, close to the source, which is consistent with the previous analysis in Subsection 1.2. Therefore, the degradation-thermal failure transition occurs in the device with increasing EMP resulting voltage, as seen by comparing the damage transients of Figs.8 and 9. The hotspot of the oxide layer indicates that the irrecoverable damage of the oxide layer causes devastating failure in the circuits. Fig.10 plots the temperature transient dependency on the rising time (0.2 ns to 2 ns). Figs.10(a) and 10(b) show the peak lattice temperature of the device under EMP resulting voltage signal, which shares exponential voltages of 1 kV and 10 kV, respectively. The family of temperature curves in Fig.10(a) gives the "rising-falling" characteristics during the rising process of the pulse, with a voltage of 1 kV. Obviously, the rapid heat accumulation appears in a short rising time of the pulse and does not lead to hot spots, and the subsequent heat dissipation increases considerably due to the device characteristics. Because heat generation under steady voltage is much less than that during the rising process, the device recovers to the initial temperature (300 K). Fig.10(b) shows the tendency of "continued rising" in temperature characteristics under the rising edge of the 10 kV voltage pulse, with rising times of 0.2 ns, 0.5 ns and 1 ns. The CMOS devices suffer thermal failure (1960 K) in the rising process of the pulse contrast with the corresponding plots in Fig.10(a). This explains the analysis in Eq. (5) that the heat generation greatly increases to the burnout as the peak voltage rises (with the same rising edge). By comparing Figs.10(a) and 10(b), it can be found that the dominant heat accumulation emerges in the rising time of the pulse, and the lattice temperature subsequently falls to room temperature if the EMP resulting voltage is not high enough to cause the temperature to rise rapidly to burnout in the rising edge due to the nonnegligible body heat dissipation. The temperature transients under different rising time pulses show that there is more heat generation in the device under a faster-rising-edge pulse, as shown in Fig.10. Fig.10(b) indicates that the faster the rising edge of the pulse, the greater the accumulation in heat and the less time is needed to reach failure with increasing χ of the heat-accumulation process, matching the previous analysis of the heat accumulation in Eq. (5). Therefore, the rate of the heat increase under steady voltage is less than that during the rising time, and the lattice temperature decreases to the original temperature (300 K). The temperature characteristics under a pulse time of 2 ns (green lines in Fig.10(a) and 10(b)) indicate that the heat accumulation and pulse features (rising time and voltage) are strongly correlated. Both the fast rising time and high pulse voltage accelerate the heat accumulation in the device.

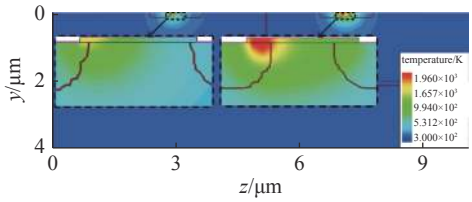

Fig. 9 Lattice temperature of the CMOS inverters under EMP resulting voltage signal

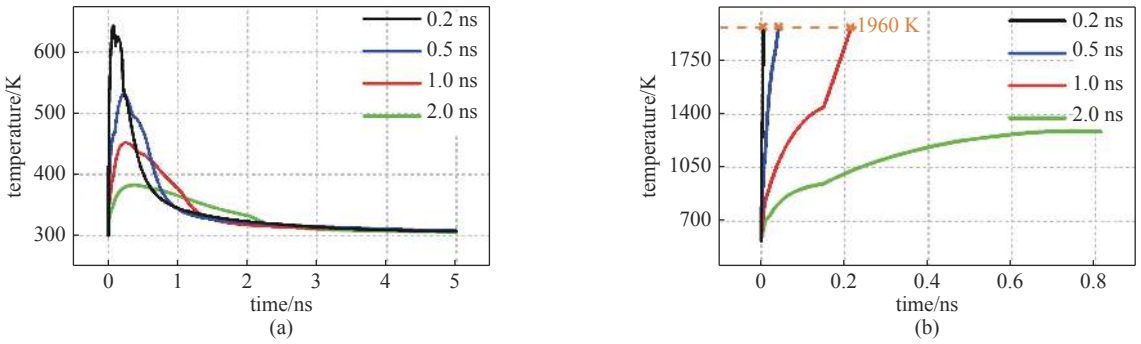

Fig. 10 Peak temperature of the CMOS inverter under EMP resulting interference with (a) 1 kV and (b) 10 kV amplitudes and 0.2 ns to 2 ns rising edges

3 Conclusion

This paper discusses the mechanism of the fast-rising-edge EMP resulting voltage-induced degradation and thermal damage effects in 0.35 μm-gate CMOS inverters. A theoretical damage model is established to explain the degradation and heat

accumulation dependencies on the characteristics of EMP resulting voltage signals. The degradation (or damage) is caused by the field-induced TAT effect, which creates a leakage current in the oxide layer. The extra charge accumulation in the channel induces deterioration in the output level, and thermal failure occurs as the pulse voltage rises. Correlated experiments and TCAD simulations are performed to validate our mechanistic analysis. Experiments based on TLP demonstrate that deterioration and failure emerge at the output level. The simulation indicates that different damage transients appear in the CMOS device under various EMP resulting voltage signals. Both degradation and hotspots in the gate oxide are observed, which is consistent with the mechanism analysis and experimental results. The temperature characteristic dependency on the pulse features (rising time and voltage) is carried out for further study. Mechanistic analysis is expected to facilitate the implementation of hardening measures to reinforce digital circuits.

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CMOS 反相器的快上升沿强电磁脉冲损伤特性

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摘 要： 随着电磁环境的日益复杂，保证集成电路（IC）的可靠性成为一个巨大的挑战。在此基础上，通过对 CMOS 反相器的仿真和实验研究，研究了快上升沿电磁脉冲（EMP）引起的陷阱辅助隧穿（TAT）效应。对此进行了详细的机理分析用于解释其物理损伤过程。EMP 感应电场在氧化层中产生陷阱和泄漏电流，从而导致器件的输出退化和热失效。建立了退化和失效的理论模型，以描述输出退化及热积累对 EMP 特征的依赖性。温度分布函数由半导体中的热传导方程导出。基于 TLP 测试系统进行的相应实验证实了出现的性能退化，与机理分析一致。Sentaurus TCAD 的仿真结果表明，EMP 引起的损坏是由栅极氧化层中发生的 TAT 电流路径引起的，这也是器件的易烧坏位置。此外，还讨论了器件失效与脉冲上升沿的关系。本文的机理分析有助于加强其他半导体器件的 EMP 可靠性研究，可以对 CMOS 数字集成电路的 EMP 加固提出建议。

关 键 词： CMOS 反相器；电磁脉冲；陷阱辅助隧穿；机理分析