引用格式：XU Wenjing, CHEN Jie, KUANG Zhangqu, et al. Design and Experiment of Low-voltage 4T-PPD Active Pixel [J]. Acta Photonica Sinica, 2022, 51(5):0523001
徐文静,陈杰,旷章曲,等.低压4T-PPD有源像素的设计与测试[J].光子学报,2022,51(5):0523001

低压4T-PPD有源像素的设计与测试

徐文静[1,2],陈杰[1],旷章曲[3],周莉[1],陈鸣[1],张成彬[1]
(1 中国科学院微电子研究所,北京 100029)
(2 中国科学院大学,北京 100049)
(3 上海韦尔半导体股份有限公司,上海 201210)

摘 要:针对应用于物联网及人工智能等领域的CMOS图像传感器功耗受限于传统高压四管钳位光电二极管(Four Transistors Pinned Photodiode, 4T-PPD)有源像素的问题,设计了低压4T-PPD有源像素。首先,基于热扩散、自诱导漂移及边缘场漂移理论,分析了PPD内部电荷转移机制的理论。其次,基于理论分析提出了用五指形像素层取代传统方形像素层,以解决低压PPD内部电荷不完全转移引起的图像拖尾。CMOS图像传感器采用0.11 μm 1P3M标准CMOS工艺流片,测试结果表明:设计的五指形4T-PPD有源像素在低压1.5 V下,与传统方形像素相比残余电荷下降了80%,满阱容量为4 928e^-,动态范围可达67.3 dB,随机噪声仅为1.55e^-_{rms},性能指标可与传统高压4T-PPD有源像素相比拟。

关键词:CMOS图像传感器;4T有源像素;电荷转移;图像拖尾;低功耗
中图分类号:TN202 **文献标识码**:A **doi**:10.3788/gzxb20225105.0523001

0 引言

CMOS图像传感器(CMOS Image Sensor, CIS)主要应用于智能手机、安防监控及汽车领域,近年来逐步扩展到物联网(Internet of Things, IoT)及人工智能(Artificial Intelligence, AI)领域。IoT及AI设备通常使用电池供电,一次充电往往需要使用一周甚至数周,这对CIS的功耗提出了挑战,因此开展超低功耗CIS的研究具有重要意义[1-2]。降低功耗最显著的手段是降低电源电压,CIS读出电路的电源电压受限于像素阵列的电源电压。四管钳位光电二极管(Four Transistors Pinned Photodiode, 4T-PPD)有源像素是当今CIS业界最广泛采用的像素结构,其传统实现方式电源电压均大于2.8 V[3-4]。2016年CHOI J团队对有源像素的时序进行了改进,使得4T-PPD有源像素可以工作在0.9 V,但其读出噪声高达83e^-_{rms},动态范围仅有50 dB,只能满足低品质成像[4]。

4T-PPD有源像素设计的关键点在于光生电荷的转移。在传统高压4T-PPD电荷转移特性的研究中,2003年,FOSSUM E R采用热电子发射理论模拟了电荷从PPD到电荷存储节点(Floating Diffusion, FD)的转移[5];2016年,HAN Liqiang等在这一基础上,加入了FD向PPD的反向电荷注入等非理想因素[6];2019年,CAPOCCIA R等在上述基础上加入了热电子发射势垒高度的估算[7]。然而,这些理论均不能完全适用于低压4T-PPD,这是因为上述理论都假定光生电荷在PPD内部是完全转移的,然而,低压4T-PPD与高压的最大区别是PPD内部电荷的不完全转移,当电压下降时,PPD内部远离传输管的电子缺乏横向电场,滞留在感光区域,造成图像拖尾,从而会严重影响成像品质。

本文设计了低压4T-PPD有源像素,基于热扩散、自诱导漂移及边缘场漂移理论,提出了PPD内部电荷

基金项目:国家重点研发计划(No. 2019YFB2204304)
第一作者:徐文静(1989—),女,助理研究员,博士研究生,主要研究方向为CMOS图像传感器技术。Email: xuwenjing@ime.ac.cn
导师(通讯作者):陈杰(1963—),男,研究员,博士,主要研究方向为SoC设计及数模混合电路设计。Email: jchen@ime.ac.cn
收稿日期:2021-12-30;**录用日期**:2022-01-25

转移机制的理论分析,并基于理论分析提出了五指形像素层取代传统方形像素层,以解决低压PPD内部电荷不完全转移引起的图像拖尾。

1 PPD内部电荷转移机制的理论分析

图1(a)为4T-PPD有源像素结构图[8],4T PPD有源像素在3T有源像素的基础上增加了一个传输管M_{TG}和一个电荷存储节点FD,并在光电二极管的表面注入了一层深度很浅,但浓度较高的P+型隔离层,从而形成了PPD光电二极管。P+隔离层能够隔离光生电子收集区N区与硅表面的接触,从而大大减小了表面态引起的暗电流。此外,P+隔离层的加入组成了一种P-N-P型的三明治结构,使得N区上下都形成了耗尽区,当PPD复位时,N区两侧的耗尽区共同扩展,可以实现N区的完全耗尽,这样不仅有益于电荷收集还能够消除残余电荷。因此4T-PPD有源像素是当今CIS业界最广泛采用的像素结构。图1(a)中虚线标识方向为光生电子移动方向,虚线方向的电势分布如图1(b)所示。与传统高压4T-PPD不同,在低压4T-PPD中,光生电子除正常从PPD向FD转移外,由于传输管开启栅电压V_{TG}变低,PPD内部远离传输管的光生电子缺乏横向电场,会滞留在感光区域,形成残余电荷,造成图像拖尾,现对PPD内部光生电子从距离传输管最远端处A点到传输管处C点的转移机制进行理论分析。

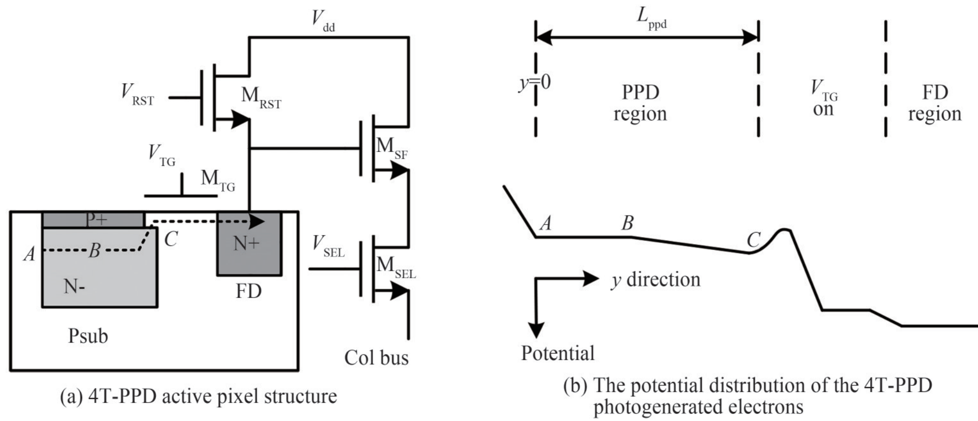


图1 4T-PPD有源像素结构及光生电子移动方向的电势分布

Fig.1 4T-PPD active pixel structure and the potential distribution of the 4T-PPD photogenerated electrons

PPD内部的电荷转移有3种机制:热扩散、自诱导漂移、边缘场漂移[9-11]。热扩散机理为当没有外加电场时,载流子由浓度高处向浓度低处扩散。如图1(b)所示,由于C点光生电子不断向FD点移动,从而形成了由A点向C点的电子浓度梯度,电子基于热扩散机理从A点向C点运动。由热扩散引起的电流密度为

$$J_{d}=D_{n}\frac{\partial Q_{n}(y,t)}{\partial y} \tag{1}$$

式中,D_n为电子扩散系数,将式(1)带入连续性方程并求解,可得热扩散时间常数τ_d表达式为

$$\tau_{d}=\frac{4L^{2}}{\pi^{2}D_{n}}\approx\frac{L^{2}}{2.5D_{n}} \tag{2}$$

$$D_{n}=\mu_{n}V_{T} \tag{3}$$

式中,L为扩散长度,μ_n为电子迁移率,V_T为热电压。

自诱导漂移机理为当没有外加电场时,载流子浓度梯度导致表面势梯度,从而形成表面势电场,载流子在表面势电场作用下进行自诱导漂移运动。如图1(b)所示,由于C点光生电子不断向FD点移动,从而形成了由A点向C点的电子浓度梯度,导致表面势从A点至C点逐渐升高,则电子从A点向C点做自诱导漂移运动,由自诱导漂移引起的电流密度为

$$J_{s}=Q_{n}\mu_{n}E_{s} \tag{4}$$

式中,E_s为自诱导漂移电场,E_s的表达式为

$$E_{\mathrm{s}}(y)=\frac{\partial\phi_{\mathrm{s}}}{\partial y}=\frac{\partial\phi_{\mathrm{s}}}{\partial Q_{\mathrm{n}}}\frac{\partial Q_{\mathrm{n}}}{\partial y} \tag{5}$$

$$\phi_{\mathrm{s}}=\phi_{\mathrm{sdd}}+\frac{Q_{\mathrm{n}}}{C_{\mathrm{ppd}}} \tag{6}$$

式中,ϕ_{s}为PPD内部表面势,ϕ_{ssd}为空阱表面势,C_{ppd}为PPD耗尽区电容。将式(3)、(5)、(6)带入式(4),并与式(1)类比,可得自诱导漂移时间常数τ_{s}的表达式为

$$\tau_{\mathrm{s}}=\frac{4L^2}{\pi^2 D_{\mathrm{n,s}}}\approx\frac{L^2}{2.5D_{\mathrm{n,s}}} \tag{7}$$

$$D_{\mathrm{n,s}}=\frac{Q_{\mathrm{n}}}{C_{\mathrm{ppd}}V_{\mathrm{T}}}D_{\mathrm{n}}=\frac{Q_{\mathrm{n,sat}}}{C_{\mathrm{ppd}}}\frac{1}{V_{\mathrm{T}}}\frac{Q_{\mathrm{n}}}{Q_{\mathrm{n,sat}}}D_{\mathrm{n}}\approx\frac{V_{\mathrm{pin}}}{V_{\mathrm{T}}}\frac{Q_{\mathrm{n}}}{Q_{\mathrm{n,sat}}}D_{\mathrm{n}} \tag{8}$$

式中,$D_{\mathrm{n,s}}$为自诱导漂移等效电子扩散系数,$Q_{\mathrm{n,sat}}$为满阱电荷量,V_{pin}为PPD的钳位电压。

边缘场漂移机理为当传输管$\mathrm{M_{TG}}$栅电压V_{TG}为高电平,会形成从传输管到PPD内部的边缘场,光生电子在边缘场的作用下从A点向C点进行边缘场漂移运动,其沿y方向的边缘场强大小为[9]

$$E(y)=\frac{2\pi}{3}\varepsilon'\frac{x_{\mathrm{ox}}}{L_{\mathrm{f}}}\frac{V_{\mathrm{TG}}}{L_{\mathrm{f}}}\approx 6.5\frac{x_{\mathrm{ox}}}{L_{\mathrm{f}}}\frac{V_{\mathrm{TG}}}{L_{\mathrm{f}}} \tag{9}$$

式中,ε'为$\mathrm{SiO_2}$的相对介电常数,x_{ox}为传输管$\mathrm{SiO_2}$的厚度,$L_{\mathrm{f}}=L_{\mathrm{ppd}}-y$,$L_{\mathrm{ppd}}$为$A$点到$C$点的距离。沿$y$方向的边缘场漂移时间常数为

$$\tau_{\mathrm{f}}=\frac{L_{\mathrm{f}}}{\mu_{\mathrm{n}}E(y)} \tag{10}$$

将式(3)、(9)带入式(10),可得τ_{f}及边缘场漂移等效电子扩散系数$D_{\mathrm{n,f}}$的表达式为

$$\tau_{\mathrm{f}}=\frac{L_{\mathrm{f}}^2}{2.5D_{\mathrm{n,f}}} \tag{11}$$

$$D_{\mathrm{n,f}}=2.6\frac{x_{\mathrm{ox}}}{L_{\mathrm{f}}}\frac{V_{\mathrm{TG}}}{V_{\mathrm{T}}}D_{\mathrm{n}} \tag{12}$$

若$V_{\mathrm{TG}}=0$,则无边缘场,由式(8)可得:当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}<V_{\mathrm{T}}/V_{\mathrm{pin}}$,$D_{\mathrm{n,s}}<D_{\mathrm{n}}$,载流子运动以热扩散为主;当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}>V_{\mathrm{T}}/V_{\mathrm{pin}}$,$D_{\mathrm{n,s}}>D_{\mathrm{n}}$,载流子运动以自诱导漂移为主。

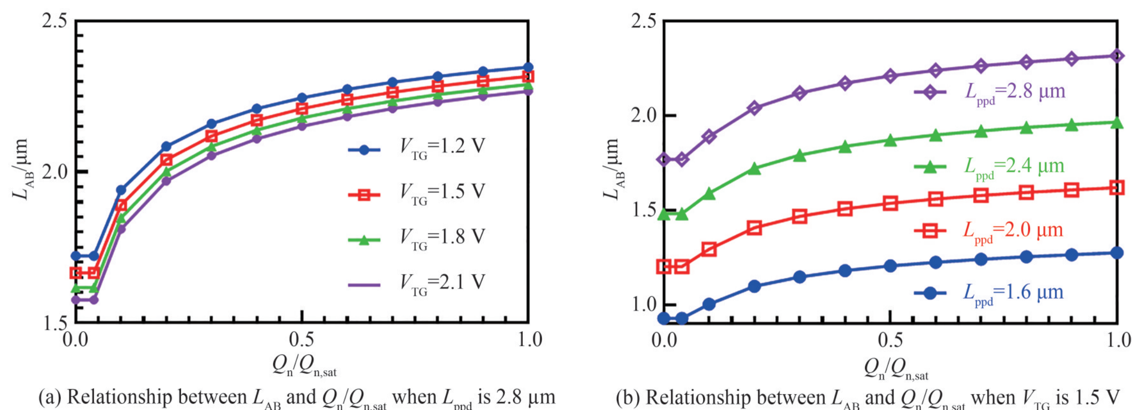
若$V_{\mathrm{TG}}>0$,有边缘场时,当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}<V_{\mathrm{T}}/V_{\mathrm{pin}}$,载流子从$A$运动到$B$以热扩散为主,从$B$运动到$C$以边缘场漂移为主,因此在$B$点处,热扩散时间常数与边缘场漂移时间常数相等,即$\tau_{\mathrm{d}}=\tau_{\mathrm{f}}$,据式(2)、(11)、(12)可得

$$\frac{L_{\mathrm{AB}}^2}{\left(L_{\mathrm{ppd}}-L_{\mathrm{AB}}\right)^3}=\frac{1}{2.6x_{\mathrm{ox}}}\frac{V_{\mathrm{T}}}{V_{\mathrm{TG}}} \tag{13}$$

若$V_{\mathrm{TG}}>0$,有边缘场时,当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}>V_{\mathrm{T}}/V_{\mathrm{pin}}$,载流子从$A$运动到$B$以自诱导漂移为主,从$B$运动到$C$以边缘场漂移为主,因此在$B$点处,自诱导漂移时间常数与边缘场漂移时间常数相等,$\tau_{\mathrm{s}}=\tau_{\mathrm{f}}$,据式(7)、(8)、(11)、(12)可得

$$\frac{L_{\mathrm{AB}}^2}{\left(L_{\mathrm{ppd}}-L_{\mathrm{AB}}\right)^3}=\frac{1}{2.6x_{\mathrm{ox}}}\frac{V_{\mathrm{pin}}}{V_{\mathrm{TG}}}\frac{Q_{\mathrm{n}}}{Q_{\mathrm{n,sat}}} \tag{14}$$

由于载流子从B运动到C以边缘场漂移为主,时间很短,因此PPD内部的电荷转移时间主要取决于载流子从A运动到B的时间。在低压4T-PPD中,令$x_{\mathrm{ox}}=3.515\ \mathrm{nm}$、$V_{\mathrm{pin}}=0.65\ \mathrm{V}$,根据式(13)、(14)可得$L_{\mathrm{AB}}$与$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}$的关系如图2所示。由图2可得:当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}<4\%$时,$AB$段以热扩散为主;当$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}>4\%$时,$AB$段以自诱导漂移为主,且$Q_{\mathrm{n}}/Q_{\mathrm{n,sat}}$越大,$L_{\mathrm{AB}}$越长,即光生电荷越多,则在PPD内部转移时间越长。由图2(a)可知,当V_{TG}增大,边缘场覆盖范围增大,则L_{AB}变短;由图2(b)可知,当像素感光区尺寸L_{ppd}减小,则L_{AB}随之变短,且L_{AB}随L_{ppd}变化明显。



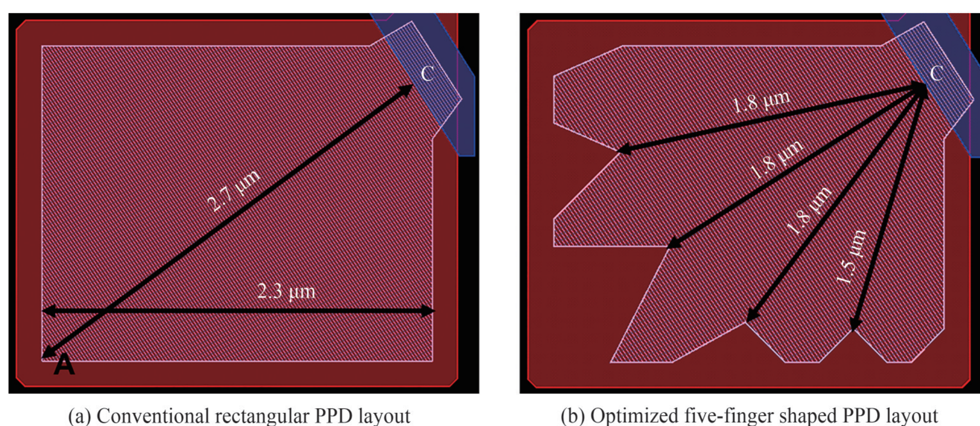
(a) Relationship between L_{AB} and $Q_n/Q_{n,sat}$ when L_{ppd} is 2.8 μm (b) Relationship between L_{AB} and $Q_n/Q_{n,sat}$ when V_{TG} is 1.5 V

图2 非边缘场主导区长度L_{AB}和PPD内光生电荷量与满阱电荷量之比$Q_n/Q_{n,sat}$的关系

Fig.2 Relationship between the length L_{AB} of the distance without fringing field and the photogenerated charge to the full-well charge $Q_n/Q_{n,sat}$

2 五指形低压PPD的设计

由上述理论分析可知，为了加速低压PPD内光生电荷的转移，需重点减小非边缘场主导区L_{AB}的长度。由图2(a)可得，L_{AB}随V_{TG}增大而减小，为了适应IoT及AI等领域对超低功耗CIS的需求，本设计V_{TG}采用低压1.5 V。由图2(b)可得，L_{AB}随L_{ppd}减小而明显减小，因此本设计采用2.8 μm小尺寸像素。传统2.8 μm方形像素的PPD版图如图3(a)所示，其中红色为有源区层，粉色为光电二极管N型（Photodiode N，PDN）注入层，蓝色为多晶硅栅层。当电压下降时，远离传输管的光生电子缺乏边缘场漂移运动，会滞留在像素中，造成图像的拖尾，从而会严重影响成像品质。



(a) Conventional rectangular PPD layout (b) Optimized five-finger shaped PPD layout

图3 两版PPD版图

Fig.3 Layouts of two shaped PPDs

由图2(b)可知，L_{AB}随L_{ppd}减小而明显减小，因此为了加快低压PPD内部的电荷转移，不改变工艺步骤并满足条件易于实现，可以改变光电二极管区PDN层的形状，以便减小非边缘场区的长度。文献[12-16]的PDN层采用了三角形、W形、梯形、L形，然而这些设计裁剪面积较大，只适用于大尺寸像素。对于小尺寸像素，不能将PDN层裁掉太多，否则会影响满阱容量，从而减小动态范围。因此，像素设计将传统方形的PDN层改进为五指形状的PDN层，如图3(b)所示，由于尖端处的场强较弱，因此五指形状不仅可以减小非边缘场区的长度，而且可形成从指尖到手掌的电场梯度，从而进一步加速了光生电子的转移。具体裁剪方法为：传输管的中心位置在C点，A点为距离C点最远的区域，因此首先将A点附近的PDN层裁掉；其次，4条箭头线将90°五等分，且每条箭头线的长度基本相同，该设计是为了保证每个区域的光生电荷运动到传输管处的时间基本相当。五指的角度基本为110°，是基于文献[13]的测试结果。最终裁掉的PDN层面积为0.61 μm²，占总面积4.27 μm²的14%。

3 测试结果与分析

本文CIS芯片采用0.11 μm标准CMOS工艺流片，有效像素阵列为1 288×728，像素类型为低压4T PPD有源像素，像素尺寸为2.8 μm×2.8 μm，整体版图面积为4 755 μm×2 870 μm。芯片版图及封装后的照片如图4所示。

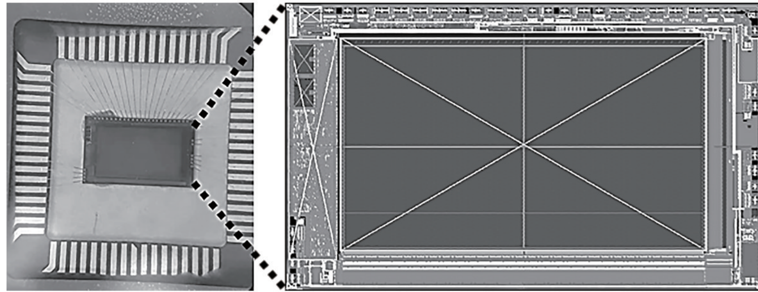


图4 芯片版图及封装后照片

Fig.4 Chip photograph and layout

为了验证优化后的五指形像素特性，本次流片像素有两个版本，像素PPD版图如图3所示。两版芯片的光电响应曲线测试结果如图5(a)所示，其中 $V_{TG}=V_{RST}=V_{SEL}=V_{DD}=1.5$ V，低光照段，改进的五指形像素线性度更好，原因在于五指形像素不仅减小了非边缘场区的长度，而且形成了从指尖到手掌的电场梯度，从而加速光电子转移，减少了残余电荷；高光照段，由于五指形像素的PDN层裁掉了14%，因此满阱容量会有略微下降，但由于CIS只工作于光电响应曲线的线性区域，因此满阱容量的略微下降并不会对CIS造成影响。图5(b)为两版芯片残余电荷曲线测试结果对比，残余电荷测试时的光通量与光电响应曲线保持一致，可见，传统方形像素的残余电荷随光强的增强逐渐增多，而改进五指形像素的残余电荷基本不随光强变化，在最大曝光处，五指形像素的残余电荷与传统方形像素相比下降了80%。两版芯片在60 ℃下的暗电流测试结果如图6(a)所示，五指形像素及传统方形像素的暗电流分别为5.01 mV/s与5.06 mV/s，暗电流基本相同。两版芯片在不同入射光波长下的量子效率(Quantum Efficiency, QE)测试结果如图6(b)所示，其中五指形像素的峰值QE为38%，而传统方形像素的峰值QE仅为29%，原因在于五指形像素减小了残余电荷，读出了更多的电子，因此测试时QE表现更佳。

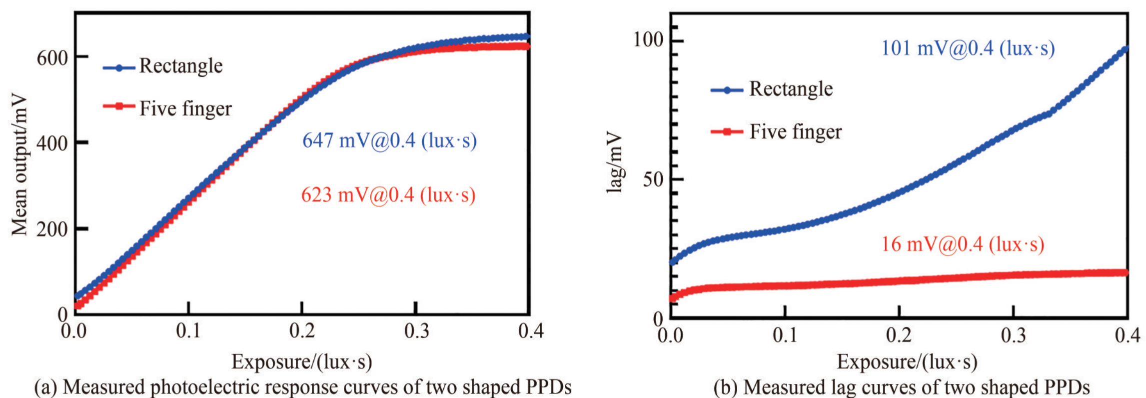
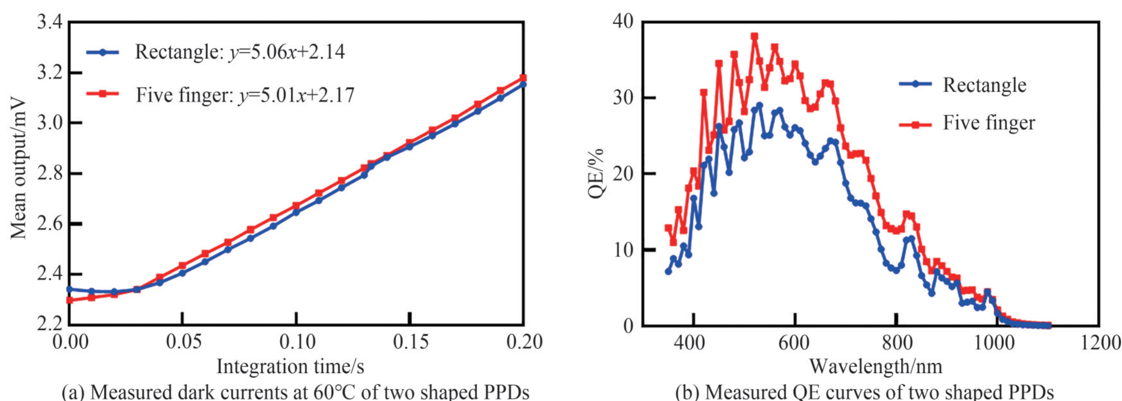


图5 两版芯片光电响应曲线及残余电荷测试

Fig.5 Measured photoelectric response curves and lag curves of two shaped PPDs

为了进一步减小残余电荷，增大光生电荷读出阶段传输管的开启时间。图7为五指形像素在不同传输管开启时间下的光电响应曲线灵敏度测试结果，该测试结果表明，低光照段光电响应曲线灵敏度随传输管开启时间的增加而变好，原因在于增大传输管的开启时间可进一步实现光生电荷的完全转移。

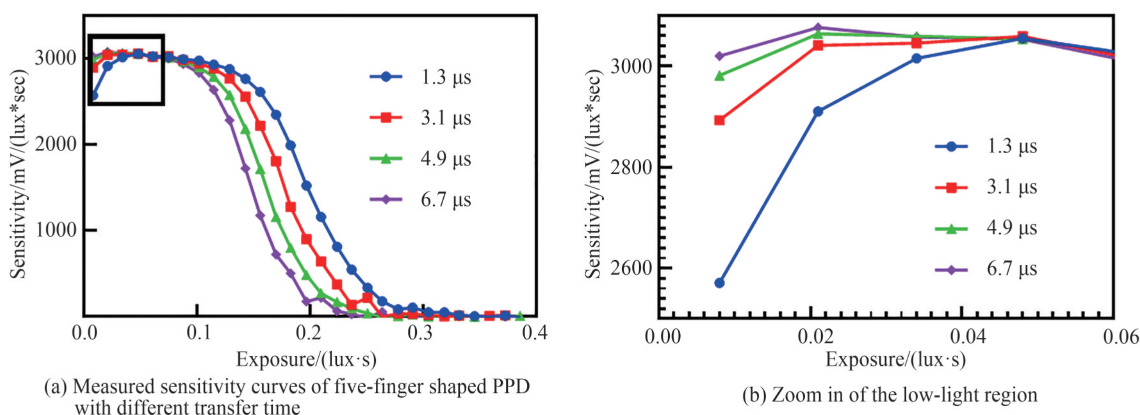
图8为五指形像素转换增益测试，其转换增益为126.4 μV/e^-，由图5(a)可得五指形像素光电响应的饱和电压为623 mV，将该值除以转换增益，可得满阱容量为4 928e^-。暗态随机噪声测试结果为196 μV，将该



(a) Measured dark currents at 60°C of two shaped PPDs
(b) Measured QE curves of two shaped PPDs

图6 两版芯片暗电流及量子效率的测试

Fig.6 Measured dark currents and QE curves of two shaped PPDs



(a) Measured sensitivity curves of five-finger shaped PPD with different transfer time
(b) Zoom in of the low-light region

图7 不同传输管开启时间下五指形像素光电响应曲线灵敏度测试

Fig.7 Measured sensitivity curves of five-finger shaped PPD with different transfer time

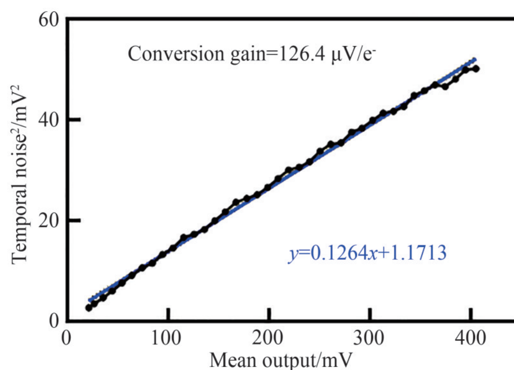


图8 五指形像素转换增益测试

Fig.8 Measured conversion gain of the five-finger shaped PPD

值除以转换增益，可得暗态随机噪声为1.55e^-_{rms}。满阱容量与随机噪声之比即为动态范围，可得动态范围为67.3 dB。

图9为五指形像素芯片在强弱光下拍摄的照片，拍摄时像素及模拟电压均为1.5 V，数字电压为1.2 V，可见本文芯片采用低压1.5 V五指形4T-PPD有源像素可实现高质量成像，且在强光和暗光下的拍摄照片均无拖尾。

五指形低压4T-PPD有源像素性能与参考文献对比如表1所示，其中文献[17]采用同样工作在1.5 V电源电压下的3T有源像素，但其动态范围与高品质成像需求的60 dB以上相比仍有差距，且读出噪声依然非常大。文献[18]像素为传统低压像素设计时采用的数字像素，该像素虽然可工作在0.5 V电源电压下，但其

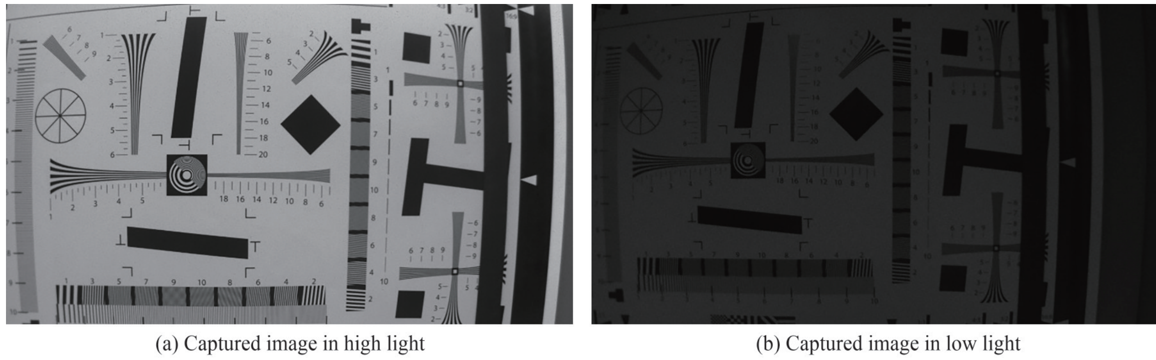

(a) Captured image in high light　　(b) Captured image in low light

图9　五指形像素芯片在强弱光下拍摄的照片

Fig.9　Captured images from the five-finger shaped chip in high and low light

动态范围只有42 dB,读出噪声高达416e^-_{rms}。文献[4]中采用的4T-PPD有源像素可工作在传统高压3.3 V模式及低压0.9 V模式,当工作于0.9 V低压模式时,其图1(a)中的V_{TG}一直为高电平,传输管保持常开,PPD和FD联通,从而将4T像素转变为3T像素使用,由于PPD和FD联通,因而扩大了满阱容量,但由于其转变为3T像素使用,读出噪声高达83e^-_{rms},动态范围仅有50 dB,只能满足低品质成像;当工作在传统高压3.3 V模式时,其动态范围为69 dB,读出噪声为5.5e^-_{rms},本文设计的1.5 V五指形4T-PPD有源像素在动态范围指标上可与之相比拟,读出噪声指标更优。

表1　本文五指形低压4T-PPD有源像素性能与参考文献对比

Table 1　Comparison of the proposed five-finger shaped PPD with other references

Parameter	This work	Ref. [4]		Ref. [17]	Ref. [18]
Process/nm	110	110		350	65
Pixel pitch/μm	2.8	5.0		5.0	4.0
Pixel type	4T PPD	4T PPD		3T Active	Digital
Pixel power supply/V	1.5	3.3	0.9	1.5	0.5
Conversion gain/(μV/e^-)	126.4	64	19	34	N/A
Full-well capacity/e^-	4 928	15 600	26 000	26 065	N/A
Dynamic range/dB	67.3	69	50	49.5	42
Random noise/e^-_{rms}	1.55	5.5	83.7	88	416

4　结论

为了解决应用于物联网及人工智能等领域的CIS功耗受限于传统高压4T-PPD有源像素的问题,本文设计了低压4T-PPD有源像素。首先,基于热扩散、自诱导漂移及边缘场漂移理论,提出了PPD内部电荷转移机制的理论分析。其次,基于理论分析提出了五指形像素层取代传统方形像素层,以解决低压PPD内部电荷不完全转移引起的图像拖尾。CIS采用0.11 μm 1P3M标准CMOS工艺流片,测试结果表明:设计的五指形4T-PPD有源像素在低压1.5 V下,与传统方形像素相比残余电荷下降了80%,满阱容量为4 928e^-,动态范围可达67.3 dB,随机噪声仅为1.55e^-_{rms},性能指标可与传统高压4T-PPD有源像素相比拟。研究成果可被应用于超低功耗CIS的设计制作。

参考文献

[1]　TOMOKI H, HIRONOBU M, HIDEAKI M, et al. A 1-inch 17Mpixel 1000fps block-controlled coded-exposure back-illuminated stacked CMOS image sensor for computational imaging and adaptive dynamic range control[C]. International Solid State Circuits Conference, 2021.

[2]　INJUN P, WOOJIN J, CHANMIN P, et al. A 640×640 fully dynamic CMOS image sensor for always-on operation [J]. IEEE Journal of Solid-State Circuits, 2020, 55(4): 898-907.

[3]　CHIHIRO O, KOUSHI U, LUONG H, et al. A high-speed back-illuminated stacked CMOS image sensor with column-parallel kT/C-cancelling S&H and delta-sigma ADC [C]. International Solid State Circuits Conference, 2021.

[4]　JAEHYUK C, JUNGSOON S, DONGWU K, et al. Always-on CMOS image sensor for mobile and wearable devices[J].

IEEE Journal of Solid-State Circuits, 2016, 51 (1): 130-140.

[5] ERIC R F. Charge transfer noise and lag in CMOS active pixel sensors[C]. International Image Sensor Workshop, 2003.

[6] LIQIANG H, SUYING Y, ALBERT J P T. A charge transfer model for CMOS image sensors [J]. IEEE Transactions on Electron Devices, 2016, 63 (1): 32-41.

[7] RAFFAELE C, ASSIM B, FARZAN J, et al. Compact modeling of charge transfer in pinned photodiodes for CMOS image sensors[J]. IEEE Transactions on Electron Devices, 2019, 66 (1): 160-168.

[8] ØYVIND J, ROBERT J, TORE M, et al. A 1.17-megapixel CMOS image sensor with 1.5 A/D conversions per digital CDS pixel readout and four in-pixel gain steps[J]. IEEE Journal of Solid-State Circuits, 2019, 54 (9): 2568-2578.

[9] JAMES E C, WALTER F K, EDWARD G R. Drift-aiding fringing fields in charge-coupled devices [J]. IEEE Journal of Solid-State Circuits, 1971, 6 (5): 322-326.

[10] JAMES E C, WALTER F K, EDWARD G R. Free charge transfer in charge-coupled devices [J]. IEEE Transactions on Electron Devices, 1972, 19 (6): 798-808.

[11] ALBERT J P T. Solid-state imaging with charge-coupled devices[M]. New York: Kluwer Academic Publishers, 2002.

[12] BHUMJAE S, SANGSIK P, HYUNTAEK S. The effect of photodiode shape on charge transfer in CMOS image sensors[J]. Solid-State Electronics, 2010, 54: 1416-1420.

[13] YANG X, ALBERT J P T. Image lag analysis and photodiode shape optimization of 4T CMOS pixels[C]. International Image Sensor Workshop, 2013.

[14] XUEZHOU C, DANIEL G, CHRIS L, et al. Design and optimisation of large 4T pixel[C]. International Image Sensor Workshop, 2015.

[15] FABIO A, MANUEL M G, GÖZEN K, et al. Transfer-gate region optimization and pinned-photodiode shaping for high-speed ToF applications[C]. International Image Sensor Workshop, 2017.

[16] TERRENCE C M, NAVID S, KYROS K, et al. The effect of pinned photodiode shape on time-of-flight demodulation contrast[J]. IEEE Transactions on Electron Devices, 2017, 64 (5): 2244-2250.

[17] KWANG-BO C, ALEXANDER I K, ERIC R F, et al. A 1.5-V 550-μW 176 × 144 autonomous CMOS active pixel image sensor[J]. IEEE Transactions on Electron Devices, 2003, 50(1): 96-105.

[18] NUMA C, GUERRIC D S, FRANÇOIS B, et al. A 65 nm 0.5 V DPS CMOS image sensor with 17 pJ/frame pixel and 42 dB dynamic range for ultra-low-power SoCs[J]. IEEE Journal of Solid-state Circuits, 2015, 50(10): 2419-2430.

Design and Experiment of Low-voltage 4T-PPD Active Pixel

XU Wenjing[1,2], CHEN Jie[1], KUANG Zhangqu[3], ZHOU Li[1], CHEN Ming[1], ZHANG Chengbin[1]

(1 *Institute of Microelectronics of the Chinese Academy of Sciences*, *Beijing* 100029, *China*)

(2 *University of Chinese Academy of Sciences*, *Beijing* 100049, *China*)

(3 *Will Semiconductor Co. Ltd.*, *Shanghai* 201210, *China*)

Abstract: The 4T Pinned Photodiode (4T-PPD) active pixel is the most widely used pixel structure for CMOS Image Sensor (CIS). In recent years, as the application of CIS has gradually expanded to the Internet of Things (IoT) and Artificial Intelligence (AI) fields, there is an increasing demand for low energy consumption. The basic theory and commonly adopted approach to reduce power consumption are to lower the power supply voltage, while the supply voltage of 4T-PPD is traditionally greater than 2.8 V. In 2016, the study published in JSSC suggested that by improving the timing, the 4T-PPD active pixels could work at 0.9 V, but the readout noise was as high as $83e^{-}_{rms}$ and the dynamic range was only 50 dB, which could only meet low-quality imaging.

Several studies have been conducted on the charge transfer characteristics of traditional high-voltage 4T-PPD. In 2003, FOSSUM E R simulated the charge transfer from PPD to Floating Diffusion (FD) node based on thermionic emission theory. Based on this work, in 2016, HAN Liqiang et al. included non-ideal factors such as the reverse charge injection from FD to PPD. Additionally, in 2019, CAPOCCIA R et al. added an estimate of the thermionic emission barrier height based on the findings of the aforementioned studies. However, these theories were not fully applicable to low-voltage 4T-PPD, since they all assumed a complete photo-generated charge transfer inside the PPD. When the voltage drops, the electrons far away from the transfer gate lack a lateral electric field and stay in the photosensitive area, causing image lag, which will seriously affect the imaging quality.

In this paper, a low-voltage 4T-PPD active pixel was designed. First, a theoretical analysis of the internal charge transfer mechanism of PPD was proposed. Three charge transfer mechanisms operate inside the PPD, namely thermal diffusion, self-induced drift, and fringe-field drift. As the charge transfer by fringe-field drift is much faster than thermal diffusion or self-induced drift, the charge transfer time inside the PPD depends predominantly on the distance where the fringing field is absent. According to the derived equations, when the photogenerated charge to the full-well charge is less than 4%, thermal diffusion is the main mechanism for the no-fringing-field section, and the length of the no-fringing-field section is almost the same. When the photogenerated charge to the full-well charge is larger than 4%, self-induced drift is the main mechanism for the no-fringing-field section. Moreover, when the transfer gate voltage increases, the length of the no-fringing-field section becomes shorter. As the PPD size decreases, the length of the no-fringing-field section becomes shorter significantly.

When the transfer gate voltage drops, the electrons far from the transfer gate lack fringing field and could not be pulled out of the PPD within transfer time, thus resulting in image lag. To solve image lag caused by low-voltage 4T-PPD, and easily achieve it without changing the process steps and conditions, the shape of the PPD layer might be changed. In previous studies, triangle, W-shape, trapezoid, and L-shape PPD have been reported, but all these designs aim at large-sized pixels. For small-sized pixels, the PPD layer should not be cut too much, otherwise, it would affect the full-well capacity and reduce the dynamic range. Therefore, a five-finger pixel layer was proposed to replace the traditional square pixel layer. Compared with conventional rectangular PPD, the five-finger shaped PPD not only reduces the length of the no-fringing-field section but also creates an extra electrical field in the direction of the charge transfer by the narrow width effect. This causes more electrons to be pulled out of the PPD. The proposed five-finger shaped PPD not only can accelerate the electrons transfer from PPD to TG but also meets the requirements of full-well capacity and dynamic range due to the small cut-off area.

A prototype sensor was fabricated using a 0.11 μm 1P3M CMOS process. The experiment results show that the residual charge of the designed five-finger 4T-PPD is reduced by 80% compared with the traditional rectangle pixel. The performance of the designed five-finger 4T-PPD with 1.5 V voltage supply is as follows, the full well capacity is 4 928e^-, the dynamic range is 67.3 dB, and the random noise is only 1.55e^-_{rms}, which are comparable to traditional high-voltage 4T-PPD. The findings presented in this paper provide important guidance for the design of low-voltage 4T-PPD.

Key words: CMOS image sensor; 4T active pixel; Charge transfer; Image lag; Low power

OCIS Codes: 230.5170; 130.5990; 280.4788; 220.3740

Foundation item: National Key Research and Development Program of China (No. 2019YFB2204304)