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传输栅掺杂对CMOS有源像素满阱容量及暗电流的影响

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摘　要：研究了传输栅掺杂，即N+TG和P+TG，对满阱容量以及暗电流的影响。沟道电势分布受传输栅与衬底功函数差的影响，随着钳位光电二极管和浮动扩散节点之间的势垒高度的增加，feedforward效应被抑制，满阱容量增加。另一方面，处于电荷积累状态的沟道可以降低暗电流。基于四管有源像素工作过程进行仿真，结果表明，在曝光期间不加负栅压的情况下，基于P+TG的像素的满阱容量相对N+TG的提高了26.9%，其暗电流为N+TG的0.377倍。当电荷转移效率大于99.999%时，N+TG的开启电压需高于2.3 V，而P+TG的开启电压需高于3.0 V。

关键词：图像传感器；CMOS有源像素；仿真；光电二极管；满阱容量；暗电流；电荷转移效率
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0 Introduction

In recent years，Pinned Photodiode（PPD）CMOS Image Sensors（CISs）are widely used in consumer electronics and other fields due to their high performance and low cost [1]. CMOS active pixels play an important role in CISs. The design of the Transfer Gate（TG）affects image quality，which is related to Full Well Capacity（FWC）and dark current [2-4]. TG affects the feedforward effect by channel potential. The feedforward effect directly influences FWC as the charges in PPD can flow into Floating Diffusion（FD）by thermal emission [5]. In addition，due to the existence of interface states，the dark current generates at the interface of the TG channel，which flows into PPD during the integration period [6].

Several papers have analyzed the influence of TG on FWC and dark current，and have proposed different improvement techniques and designs. A negative bias operation of TG is an effective method to reduce dark current under TG [7-9]. When a negative bias is added to TG，the channel is in a state of accumulation，isolating the interface state of the channel from the depletion region of PPD so that dark current is greatly reduced. Furthermore，adopting a negative bias to TG increases the channel barrier，inhibiting the feedforward effect and increasing FWC. A positive voltage adopted to TG is also beneficial to reduce dark current due to the sharing mechanism [6]，but will make FWC decrease. To reduce dark current，Ref.[10] has proposed a method to change the position of the potential barrier under TG by adjusting the doping length of p-type impurities so that dark charges could flow to FD. This paper investigates the influence of two types of doped transfer gates，named N+TG and P+TG，on FWC and dark current. P-type doping is shared with p+ doping used in PMOS transistors，so no additional steps need to be introduced. The channel potential is affected by the work function difference between TG and the substrate. A higher potential barrier between the TG channel and PPD can effectively suppress the feedforward effect and increase FWC. In addition，accumulated channels can reduce dark current.

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1　Impact of TG doping on FWC and dark current

1.1　Work function influence on TG channel potential

To analyze the influence of TG doping on FWC and dark current, a typical 4T-PPD pixel structure is used in this paper. The device cross section is shown in Fig. 1, which consists of a PPD, a "special" TG transistor whose drain is a Floating Diffusion (FD) node, and three conventional transistors named Reset Transistor (RST), Source Follower (SF), and Row Select (RS) transistor. P+ TG and N+ TG are adopted in this paper. The p-type heavy doping range is in the middle region of TG, 0.1 μm away from the TG edge. The n-type heavy doping edge of FD is next to the p+ doped boundary on the right side of TG. The upper left corner of Fig. 1 shows the N+ TG structure, and the two kinds of TG have the same structure except for different doping types. To ensure the smooth transfer of charges from PPD to FD, PPD implantation usually extends slightly under TG to assist charge transfer. At the same time, two p-type implantations are carried out under TG, named TG_PD and TG_FD, for threshold adjustment and anti-punch-through respectively. Before illumination, RST opens to reset PPD and FD. The photo-generated electrons are collected and stored by PPD during illumination. After an exposure period, the photoelectric charges in PPD are transferred to FD by switching on TG, where the signal in the charge domain is converted to the voltage domain. When RS is switched on, the signal is buffered to the column bus by SF.

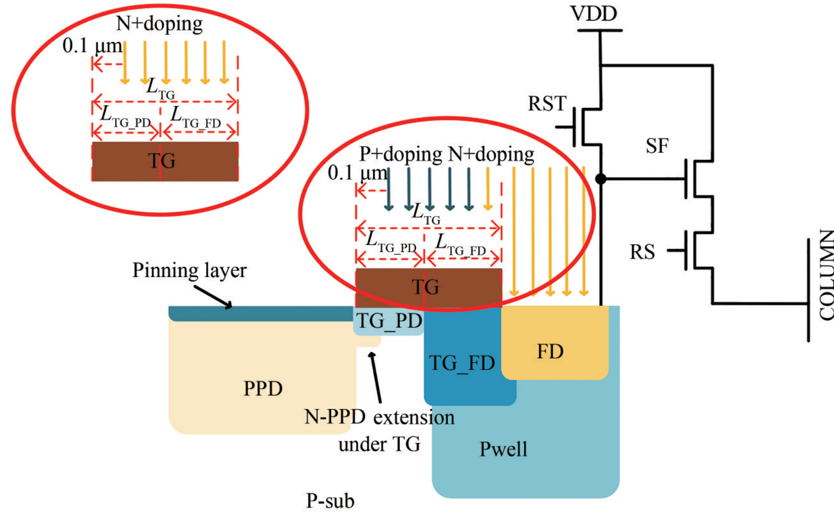

Fig. 1　4T-PPD pixel structure profile of P+ TG and N+ TG

The impact of TG doping on FWC and dark current is achieved by channel potential, which is affected by the work function of TG and the substrate. P+TG is proposed in the paper. Fermi energy level of P+TG is near the valence band. The work function difference (W_{ms-p}) between P+TG and the p-type substrate is calculated by

$$W_{ms-p}=\frac{E_g}{2}-KT\ln(\frac{N_a}{n_i})\tag{1}$$

where E_g is the silicon forbidden bandgap, $KT\ln(N_a/n_i)$ represents the difference between the central bandgap energy of the substrate and Fermi energy level, K is the Boltzmann constant, T is the absolute temperature, N_a is the doping concentration in the channel region of the substrate, n_i is the intrinsic carrier concentration in silicon at room temperature (300 K). According to the physics of semiconductors [11], part of the voltage caused by the work function difference and traps falls on the oxide layer, while the other part falls on the channel interface.

$$-\frac{W_{ms-p}}{q}+\frac{q\times N_{trap}\times\sigma_s}{C_o\times W\times L}=V_{sp}-\frac{Q_{space}}{C_o}\tag{2}$$

where N_{trap} is the density of traps, the typical value of N_{trap} is 1×10^{10} traps·cm^{-2}, σ_s is the effective capture cross-section (In the simulation, σ_s is set to 1×1^{-14} cm^2), C_o is the gate capacitance per unit area, $C_o=\varepsilon_o\times\varepsilon_r/d$, V_{sp} is the interface potential of P+TG channel, Q_{space} is the density of interface space charge. Substituting the

parameters in Table 1 into Eqs.(1) and (2), the left side of the formula is negative after calculation. The work function difference has a higher effect than traps, and the channel interface is in an accumulated state. Q_{space} uses the metal-insulator-semiconductor model to calculate according to the formula in the accumulative state [11].

Table 1 The design parameters in this paper

Parameter	Value	Unit
Absolute temperature, T	300	K
Silicon forbidden bandgap, E_g	1.12	eV
Boltzmann constant, K	1.38×10^{-23}	J/K
Doping concentration in channel region of substrate, N_a	1.5×10^{17}	cm^{-3}
Intrinsic carrier concentration, n_i	1.5×10^{10}	cm^{-3}
Thickness of oxide layer, d	6	nm
Width of TG, W	1	μm
Length of TG, L	0.6	μm
Dielectric constant, ε_o	8.85×10^{-12}	F/m
Relative dielectric constant of the silicon, ε_s	11.9	—
Relative dielectric constant of the oxide layer, ε_r	3.9	—

$$Q_{space}=\frac{\sqrt{2}\,\varepsilon_s\varepsilon_o KT}{qL_D}\times e^{(-\frac{qV_{sp}}{2KT})} \tag{3}$$

where L_D is the Debye length, $L_D=((\varepsilon_o\varepsilon_s KT)/(q^2N_a))^{1/2}$, ε_s is the relative dielectric constant of silicon. Combined with Eqs. (1), (2) and (3), we can get that V_{sp} is -0.03 V. Generally, traditional TG is heavily doped with n-type impurities. The Fermi energy level of N+TG is near the conduction band. The work function difference is $W_{ms-n}=-E_g/2-(KT)\ln(N_a/n_i)$. In the same analysis as above, the interface potential of the N+TG channel, named V_{sn}, is calculated by using the depletion approximation method, and V_{sn} is 0.66 V. Therefore, the channel potential of P+TG is lower than that of N+TG. A higher barrier between the TG channel and PPD is conducive to inhibiting the feedforward effect.

1.2 TG doping influence on FWC and dark current

FWC is an important parameter of CIS. The feedforward effect is the main reason for the decrease in FWC. Fig. 2 shows the potential diagram along the emission current path with TG off. The lower potential of the channel, the more difficult it is for the electrons in PPD to enter FD through thermal emission. In Ref.[12], when PPD reaches FWC, there is an equilibrium of three main currents in PPD: the light current $I_{ph}=\eta\Phi_{ph}$, the sub-threshold current I_{DS} (mainly caused by the feedforward effect), and the forward current I_{fw} of PPD.

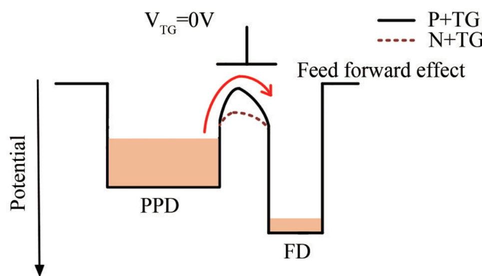

Fig. 2 Potential diagram along the emission current path of P+ TG and N+ TG

$$I_{DS}=I_0 e^{-\frac{V_{Bx}}{\nu_{th}}} \tag{4}$$

$$I_{fw}=I_{sat}(e^{\frac{-V_{FWx}}{\nu_{th}}}-1) \tag{5}$$

$$I_0 e^{-\frac{V_{Bx}}{\nu_{th}}}+I_{sat}(e^{\frac{-V_{FWx}}{\nu_{th}}}-1)=\eta\phi_{ph} \tag{6}$$

where I_0 is the current coefficient, depending on the Richardson constant, the cross-sectional area of the transfer

path (PPD-TG interface), and temperature. The subscript x in the symbols mentioned below represents different doping types of TG, taking n and p respectively. V_{Bx} is the height of the potential barrier between the TG channel and PPD at the full well, which is represented as $V_{Bx} = V_{FWx} - V_{sx}$ here, V_{FWx} is the PPD voltage at the full well, and I_{sat} is the reverse saturation current through PPD. According to the analysis in Section 1.1, we know that V_{sn} is greater than V_{sp}. Combined with Eqs. (4), (5) and (6), it can be concluded that V_{FWp} is smaller than V_{FWn}. In addition, $V_{Bn} < V_{Bp}$ can also be obtained. The higher barrier can effectively inhibit the feedforward effect. Ignoring the generation and recombination process of the PPD region, FWC can be approximately expressed as the maximum voltage swing of PPD multiplied by C_{PPD}:

$$Q_{FWx} = -(V_{FWx} - V_{pin}) \times C_{PPD} \tag{7}$$

where V_{pin} is the maximum potential variation of hole and electron quasi-Fermi level [13], in general, the voltage after PD reset is V_{pin}, Q_{FWx} is the FWC of PPD. Obviously, $Q_{FWn} < Q_{FWp}$, the FWC of P+TG is improved compared with that of N+ TG.

In a 4T-PPD pixel, the main dark current contributor is the traps at the silicon-oxide interface under TG [6]. Dark current caused by traps can be expressed as Ref.[14].

$$I_{dark} = qn_i \left(\frac{\sigma_s \nu_{th} N_{trap}}{2} \right) \tag{8}$$

where ν_{th} is the thermal velocity. Combined with the previous analysis, the P+TG channel is in a state of accumulation, isolating the depletion region of PPD from the interface states below TG. The dark current generated by traps is compensated, resulting in the reduction of dark current.

2 Simulation results

A 4T-PPD is simulated in Technology Computer Aided Design (TCAD). The same trap model as Ref.[6] is added to the simulation. We set the concentration of traps to 1×10^{10} traps·cm^{-2} and the capture cross-section to 1×10^{-14} cm^2 [10,15-16]. PPD of two doping types of TG integrates for 10 ms in dark conditions. In addition, the light intensity is set to 2×10^{-3} W/cm^2 when testing the FWC of PPD. This paper compares P+ TG and N+ TG under the same channel and substrate doping conditions. FWC and dark current characteristics are simulated when the turn-off voltage (V_{TG_off}) is 0 V.

To prevent punch-through, L_{TG_PD} and L_{TG_FD} are set to 0.3 μm by default. We set the left side coordinate of TG to 5.0 μm. Given FWC and charge transfer problem, the length of TG is set to 0.6 μm. Fig. 3 shows the simulation cross-section with two doping types of TG. The white line is the depletion zone boundary. As shown in Fig. 3, the N+ TG channel is depleted. For a more intuitive view of the results, Fig. 4 shows the one-dimensional electrostatic potential distribution intercepted by two doping types of TG along the X-X' (X-X' is 0.01 μm away from the channel interface) and along the Y-Y' (Y-Y' is located in the middle of TG), respectively. It is obvious that V_{sn} of N+TG is greater than zero. V_{sp} obtained by the simulation is −0.032 V, which is slightly different from the previous theoretical calculation of −0.03 V, due to the simulation deviation. P+TG has a higher potential barrier which can better inhibit the feedforward effect. The potential distribution fully indicates that the channel of P+TG is in the state of hole accumulation. FWC with two types of doped TG is shown in Fig. 5(a). The values are normalized using FWC of N+TG as the standard. Due to the lower channel potential of P+TG, the ability to suppress the feedforward effect is stronger, and FWC is higher. Compared with N+TG, the FWC of P+TG is increased by 26.5%. Furthermore, Fig. 5(b) shows the number of dark charges integrated by PPD of two types of doped TG in 10 ms, which is normalized based on the dark charges (N_{dark}) of N+TG. Dark current of P+TG is 0.377 times that of N+TG. According to the above analysis, P+TG has better FWC and dark current characteristics when V_{TG_off} is 0 V. In practical engineering, a negative voltage is usually applied to N+TG during exposure to obtain good full well capacity and dark current characteristics. As shown in Fig. 6, FWC and dark current for two types of TG at various V_{TG_off} are obtained. With the decrease of negative voltage, channel potential decreases, so the feedforward effect is inhibited, and the FWC of two types of TG increases. When V_{TG_off} is less than −0.8 V, the FWC of N+TG is higher than that of P+TG at 0 V. As the negative voltage added to N+TG is less than −0.2 V, the depletion zone of PPD is disconnected from the depletion zone of TG channel, and the channel of N+TG accumulates gradually. Dark current of N+TG reduces with V_{TG_off} decreases. When V_{TG_off} is greater than −0.2 V,

dark current of N+TG decreases due to the sharing mechanism. For P+TG, the negative voltage has little effect on the dark current because the channel is accumulated. The introduction of negative voltage can improve the full well capacity and dark current characteristics of N+TG, increasing in power consumption.

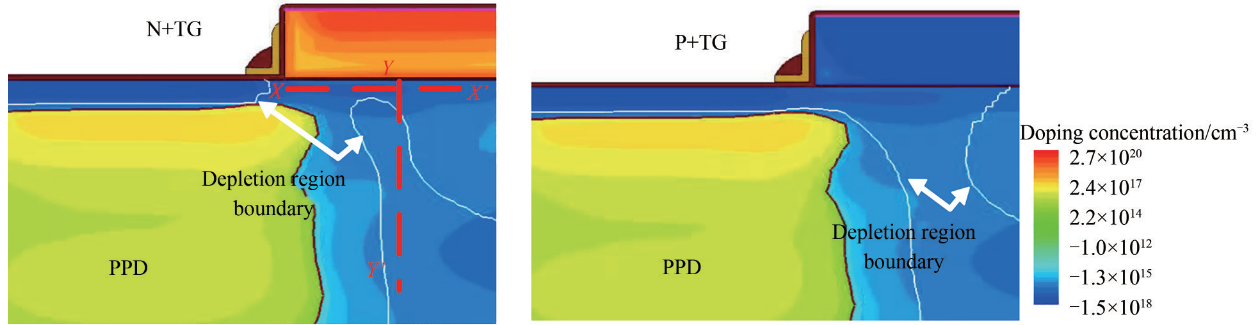

Fig. 3 Two-dimensional simulation profiles

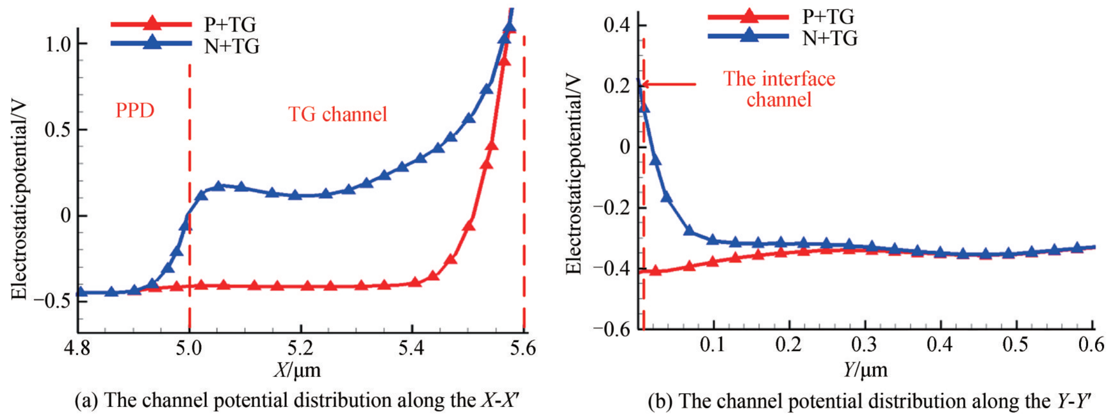

Fig. 4 One-dimensional potential diagrams under TG

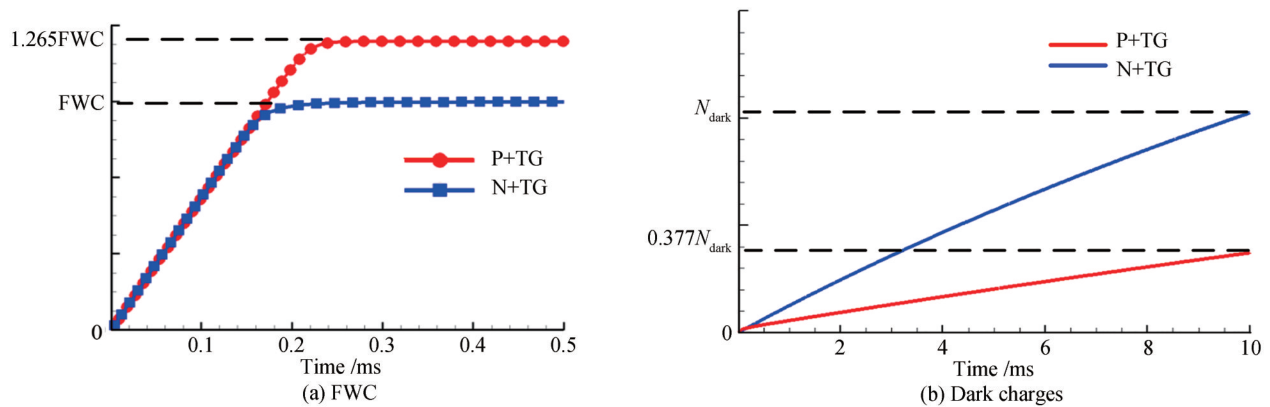

Fig. 5 Simulation results of FWC and dark charges with two types of doped TG at 0 V

The opening characteristics of TG affect image lag, which plays an important role in imaging quality and is usually determined by Charge Transfer Efficiency (CTE) [17].

$$\mathrm{CTE}=\frac{Q_{\mathrm{OUT}}}{Q_{\mathrm{FW}x}} \tag{9}$$

where Q_{OUT} is charges transferred from PPD to FD. The TCAD tool is used to study the CTE of P+TG and N+ TG. In the simulation, the charge transfer characteristic with opening voltage ($V_{\mathrm{TG_on}}$) of TG from 0 V to 3.3 V is simulated. As shown in Fig. 7, when $V_{\mathrm{TG_on}}$ increases, CTE improves and finally tends to be stable, approaching 100%. Before $V_{\mathrm{TG_on}}$ is 3.0 V, the transfer characteristic of N+TG is better than that of P+TG

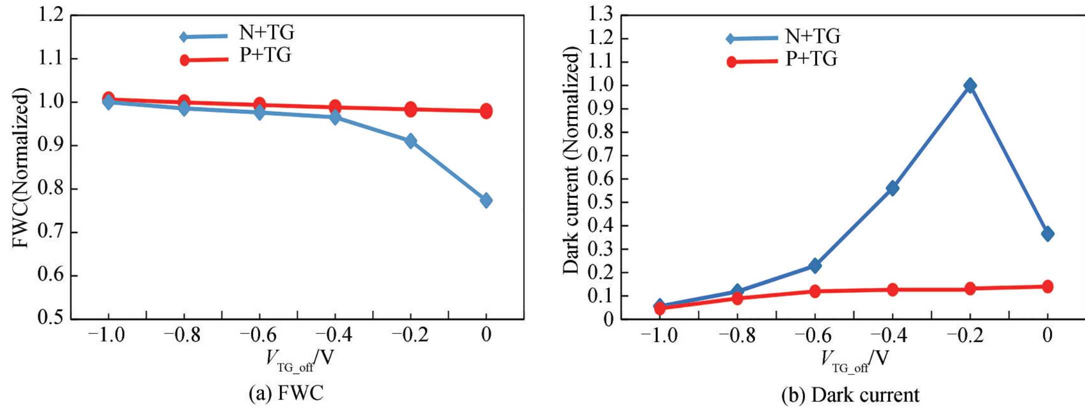

Fig. 6 Simulation results of FWC and dark current with two types of doped TG at various $V_{\mathrm{TG_off}}$

because of the higher channel potential. The charge transfer characteristic is controlled by $V_{\mathrm{TG_on}}$. Specially, the CTE of N+TG is greater than 99.999% at 2.3 V, while P+TG requires 3.0 V. As $V_{\mathrm{TG_on}}$ (> 3.0 V) continues to rise, the CTE of N+TG and P+TG shows no difference, suggesting that charges can be completely transferred from PPD to FD. Universally, the opening voltage of TG is 3.3 V, Fig. 8 shows the potential profile with TG on. The channel potential of N+TG is higher than that of P+TG. Moreover, the potential gradually increases from the left side to the right side, and charges can be transferred smoothly along the transfer path. This is the ideal situation for simulation. In actual devices, CTE may be lower than the simulation results because of process deviation and annealing process. When the FWC of PPD is high, CTE will be negatively affected, resulting in image lag. At this point, the positive charge pump needs to be introduced to ensure transfer characteristics. Under the simulation conditions in this paper, two doping types of TG have good transfer characteristics at 3.3 V.

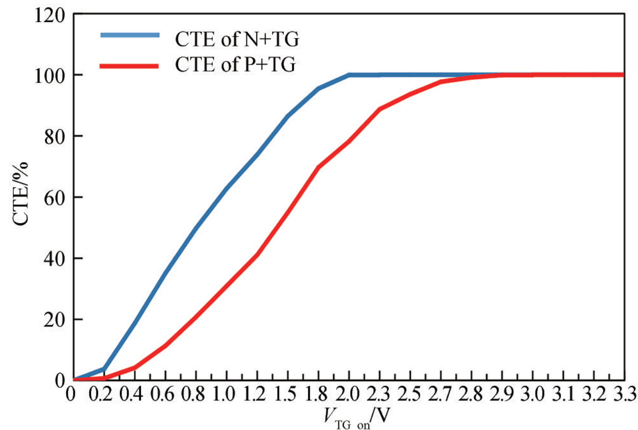

Fig. 7 Simulation results of CTE with P+TG and N+TG

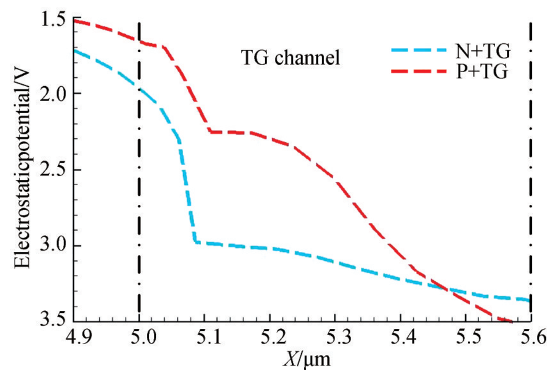

Fig. 8 One-dimensional potential diagram under TG channels with TG on

3 Conclusion

The influence of TG doping on FWC and dark current is analyzed in this paper. The channel potential of P+TG is lower than that of N+TG because of the work function difference between TG and substrate. The higher barrier inhibits the feedforward effect and increases FWC. On the other hand, the channel of P+TG is in a state of accumulation. The interface state under P+TG is isolated from PPD and dark current decreases. Device level simulation using TCAD is performed, when $V_{\mathrm{TG_off}}$ is 0V, the full well capacity of the photodiode based on P+TG is 26.5% higher than that of N+TG, and the dark current is 0.377 times that of N+TG. N+TG can optimize FWC and dark current performance by adding negative voltage. In addition, the CTE of N+TG is greater than 99.999% at 2.3 V, while P+TG requires 3.0 V. The voltage applied to P+TG is higher than that to N+TG for complete charge transfer.

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Effect of Transfer Gate Doping on Full Well Capacity and Dark Current in CMOS Active Pixels

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Abstract: In recent years, Pinned Photodiode (PPD) CMOS Image Sensors (CISs) are widely used in consumer electronics, medical, and other fields due to their advantages of high integration, low power consumption and low cost. CMOS active pixels play an important role in CISs. The design of the Transfer Gate (TG) affects image quality, which is related to Full Well Capacity (FWC) and dark current. TG affects the feedforward effect by channel potential. The feedforward effect directly influences FWC as the charges in PPD can flow into Floating Diffusion (FD) by thermal emission. In addition, due to the existence of interface states, dark current generates at the interface of the TG channel, which flows into PPD during the integration period. Several papers have analyzed the influence of TG on FWC and dark current, and have proposed different improvement techniques and designs. When a negative bias is added to TG, the channel is in a state of accumulation, isolating the interface state of the channel from the depletion region of PPD so that dark current is greatly reduced. Furthermore, adopting a negative bias to TG increases the channel barrier, inhibiting the feedforward effect and increasing in FWC. A positive voltage adopted to TG is also beneficial to reduce dark current, but will make FWC decrease. Adjusting the doping length of p-type impurities can change the position of the potential barrier, so that dark charges flow to FD. In this paper, the influence of two types of doped transfer gates, named N+TG and P+TG, on full well capacity and dark current are investigated. Channel potential is affected by the work function difference between TG and substrate. As the barrier height between pinned-photodiode and floating diffusion increases, the feedforward effect is inhibited and the full well capacity increases. On the other hand, the channel in charge accumulation can reduce dark current. To analyze the influence of TG doping on FWC and dark current, a typical 4T-PPD pixel structure is used in this paper. The device consists of a PPD, a "special" TG transistor whose drain is a FD node, and three conventional transistors named Reset Transistor (RST), Source Follower (SF), and Row Select (RS) transistor. The two kinds of TG have the same structure except for different doping types. P-type doping is shared with p+doping used in PMOS transistors, so no additional steps need to be introduced. Device level simulation using Technology Computer Aided Design (TCAD) is performed based on 4T pixels working process, trap model is added to the simulation. The concentration of traps is set to 1×10^{10} traps·cm^{-2} and the capture cross-section to 1×10^{-14} cm^2. PPD of two doping types of TG integrates for 10 ms in dark conditions. In addition, the light intensity is set to 2×10^{-3} W/cm^2 when testing the FWC of PPD. This paper compares P+ TG and N+ TG under the same channel and substrate doping conditions. FWC and dark current characteristics are simulated when the turn-off voltage ($V_{\mathrm{TG_off}}$) is 0 V. Simulation results demonstrate that the full well capacity of photodiode based on P+TG is 26.5% higher than that of N+TG. The dark current is 0.377 times that of N+TG without negative voltage during the exposure. In practical engineering, a negative voltage is usually applied to N+TG during exposure to obtain good full well capacity and dark current characteristics. The opening characteristics of TG affect image lag, which plays an important role in imaging quality and is usually determined by Charge Transfer Efficiency (CTE). CTE of N+TG is greater than 99.999% at 2.3 V, while P+TG requires 3.0 V. P+TG requires a higher voltage to ensure excellent charge transfer. When the FWC of PPD is high, CTE will be negatively affected, resulting in image lag. At this point, the positive charge pump needs to be introduced to ensure transfer characteristics. Under the simulation conditions in this paper, two doping types of TG have good transfer characteristics at 3.3 V.

Key words: Image sensors; CMOS active pixels; Simulation; Photodiodes; Full well capacity; Dark current; Charge transfer efficiency
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