引用格式：ZHANG Xisheng，YAN Chunyu，WANG Jingzhou，et al. Optimizing Processes of Silicon Heterojunction Solar Cell[J]. Acta Photonica Sinica，2021，50(12)：1223001
张喜生，晏春愉，王景州，等．硅异质结太阳能电池工艺优化[J]．光子学报，2021，50(12)：1223001

硅异质结太阳能电池工艺优化

张喜生，晏春愉，王景州，马紫微，姚陈忠
（运城学院 物理与电子工程系，山西 运城 044000）

摘　要：硅异质结太阳能电池的制作过程中，所有工艺步骤都会影响其性能。通过扫描电镜、反射率、量子效率及少子寿命测试，逐步优化硅异质结太阳能电池的性能。结果表明，单晶硅片钝化的最佳锥体尺寸约为6～9 μm。利用高质量的本征氢化非晶硅(a-Si:H)薄膜钝化硅片，获得了超过5 ms的少数载流子寿命。采用大带隙p型a-SiC_x:H薄膜替代p型a-Si:H薄膜作为发射层，提高电池在较短波长范围内的光响应。通过降低铟锡氧化物的自由载流子吸收，显著改善了长波长区域光响应。综合优化后硅异质结太阳能电池功率转换效率达到21.68%。

关键词：太阳能电池；硅异质结；钝化；光响应；功率转换效率
中图分类号：TM914.4　　**文献标识码**：A　　**doi**：10.3788/gzxb20215012.1223001

Optimizing Processes of Silicon Heterojunction Solar Cell

ZHANG Xisheng，YAN Chunyu，WANG Jingzhou，MA Ziwei，YAO Chenzhong
（*Department of Physics and Electronic Engineering*，*Yuncheng University*，*Yuncheng*，*Shanxi* 044000，*China*）

Abstract：All process steps in the fabrication process affect the performance of silicon heterojunction solar cells. In this contribution，we optimize the performance of SHJ solar cells by step-by-step analysis including scanning electron microscope，reflectivity，quantum efficiency and minority carrier lifetime measurement. It is indicated that the optimum pyramid size for c-Si wafer passivation is about 6～9 μm. More than 5 ms of minority carrier lifetime was obtained by passivating silicon wafer with high quality intrinsic hydrogenated amorphous silicon (a-Si：H) film. Large band gap p-type a-SiCx：H was used as emitter layer alternative to p-type a-Si：H film，which will increase the photoresponse in the short wavelength range. A significant improvement of photoresponse in the long wavelength range was also improved by reducing the free carrier absorption of indium tin oxides. Based on this optimization silicon heterojunction solar cells with power conversion efficiencies exceeding 21.68% were prepared on c-Si wafers textured in alkaline solution.

Key words：Solar cell；Silicon heterojunction；Passivation；Photoresponse；Power conversion efficiency
OCIS Codes：230.2090；040.6040；160.6000；350.6050

0　Introduction

Advantages of Silicon Heterojunction (SHJ) solar cells are its symmetrical structure and low temperature process，a very high energy conversion efficiency potential (＞25%)[1-4]，a low temperature coefficient and a

Foundation item：National Natural Science Foundation of China (No. U180110)，Science and Technology Innovation Project of Shanxi Province (No. 2019L0850)，Scientific Research Project of Yuncheng University (Nos. CY-2018014，YQ-2019002)
First author：ZHANG Xisheng (1982—)，male，associate professor，Ph.D. degree，mainly focuses on the performance optimization of crystalline silicon and perovskite-based optoelectronic devices. Email：zhangxisheng@ycu.edu.cn
Received：Apr.22，2021；**Accepted**：Jul.22，2021

good stability under light and thermal exposure. Optical and electrical enhancements are two typical ways to enhance the conversion efficiency of the solar cells. Over the past few years, many researchers joined this field, which accelerated and deepened the fundamental knowledge about this structure[5-7]. SHJ solar cell technology involves many processes, from wafer wet-chemical treatment, passivation to electrode fabrication. The recombination loss affect significantly solar cell performances, more particularly the Fill Factor (FF), but also the open-circuit voltage (V_{OC}). Intrinsic hydrogenated amorphous silicon layer i-a-Si:H passivation quality have an impact on the interface recombination and thus affect the open circuit voltage (V_{OC}) of the final solar cell[8-10]. As the window layer of the SHJ solar cells, the p-type amorphous film also requires a wide band gap to reduce the parasitic absorption and improve the short wavelength photo-response of the solar cells. Low carrier concentration and high carrier mobility of Indium Tin Oxides (ITO) (Sn:In_2O_3) film are also necessary for reducing the free carrier absorption, thereby increasing photo-response in the longer wavelength range[11]. So far, there are few systematic studies on SHJ solar cells by step-by-step analysis.

Here, starting from the saw damage and pyramid etched Si wafer to the complete device, we optimize the performance of SHJ solar cells by step-by-step analysis. Optimum pyramid size for passivation of surface was obtained. Silicon wafer was passivated with high quality amorphous silicon layer. To reduce the parasitic absorption and improve the short wavelength response of the solar cells, large band gap p-type a-SiC_x:H was applied as emitter layer alternative to p-type a-Si:H film. By regulating ITO Physical Vapor Deposition (PVD) process, low carrier concentration and high carrier mobility was obtained. We optimized the carrier concentration of ITO, as low as half value of ordinary ITO, obviously reducing the free carrier absorption and boost the External Quantum Efficiency (EQE) in the longer wavelength range. Based on these optimizations, SHJ solar cells with a high conversion efficiency were prepared.

1 Experimental

As-cut c-Si wafer (Czochralski grown, mono-crystalline, n-type, Si(100), diameter 5 inch (1 inch=2.54 cm), initial thickness 130~150 μm, resistivity 1~5 Ω·cm) was handled by wet-chemical processes, including removal of saw damage and a random pyramid surface texture etching. For the removal of saw damages, the as-cut samples were etched in aqueous solution of KOH (wt. 20%) at 75℃ for 10 s. Subsequently, random pyramid textured substrate surfaces were prepared in a lower concentration of KOH solution at 80℃ with TS45 as an additive. Afterward, the wafers were cleaned according to the modified Radio Corporation of American (RCA) process. Owing to its property of being easily oxidized, the prepared c-Si wafer was dipped in diluted hydrofluoric acid (5%, 1 min) immediately. Hydrogenated amorphous silicon (a-Si:H) layers were deposited by the standard Plasma Enhanced Chemical Vapor Deposition (PECVD) process at different temperatures (180, 200, 220 and 240℃). The n-type and p-type a-Si:H films were deposited by doping PH_3 or B_2H_6 diluted with H_2 and SiH_4, respectively. Thus, heterojunctions with emitter layer, intrinsic layers and a-Si:H Back Surface Field (BSF) of the sequence (n) a-Si:H/(i) a-Si:H/(n) c-Si/(i) a-Si:H/(p)a-Si:H were formed.

For the solar cell preparation of Transparent Conductive Oxides (TCO) layers, ITO film (100 nm) were prepared by DC magnetron sputter deposition on both side of wafer with addition of $<$ 1.0% oxygen to the Ar sputter gas without additional sample heating[11]. The rear contact was prepared by evaporating a 500 nm Ag film. The preparation of 1 cm×1 cm solar cells was completed by evaporated 1 μm Ag front grid lines.

A Field Emission Scanning Electron Microscopy (FESEM, HITACHI, SU-8020) was used to investigate morphological of the textured solar cell substrates. The thickness of the film has been measured by using Veeco Profiler (Dektak 150). WCT-120 lifetime tester from Sinton Instruments was applied for minority carrier lifetime test. The photovoltaic performance was characterized under a simulated sunlight illumination generated by a SAN-EI ELECTRIC XES-40S2-CE Solar Simulator (AM 1.5 G filter at 100 mW/cm^2), which was calibrated using a certified silicon photodiode before used. $J-V$ characteristics were obtained by using Keithley 2 400 source meter.

2 Results and discussion

2.1 Structure and process flow of SHJ solar cell

Fig. 1(a) shows the schematic structure of the SHJ devices, which is the sequence of Ag grid/ITO/

(p) a-Si: H/(i) a-Si: H/(n) c-Si/(i) a-Si: H/(n) a-Si: H/ITO/Ag back contact. Fig. 1(b) shows the process flow of the SHJ solar cell. The full device processing sequence for SHJ solar cells comprises wet chemical treatments of the c-Si substrate and subsequent layer deposition. The n-type crystalline silicon (100) with a resistivity of 1～5 Ω·cm and thickness of 150 μm was acted as absorbing layer, ultra thin (i) a-Si: H film function as passivation layer, and (p) a-Si: H was employed as emitter layer, as well as forming p-n heterojunction with (n) c-Si, and (n) a-Si: H was as BSF. ITO target material (Sn: In_2O_3 resistivity≦0.14 mΩ·cm, purity 99.99%) was sputtered as transparent conductive oxide layer. Siver (Ag) was used as grid line and back contact.

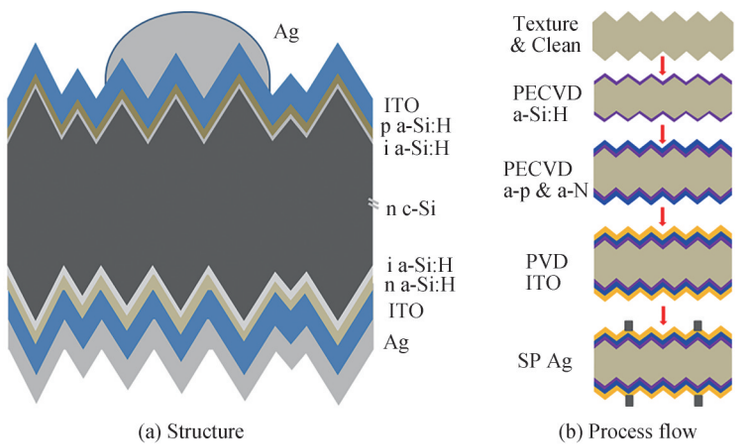
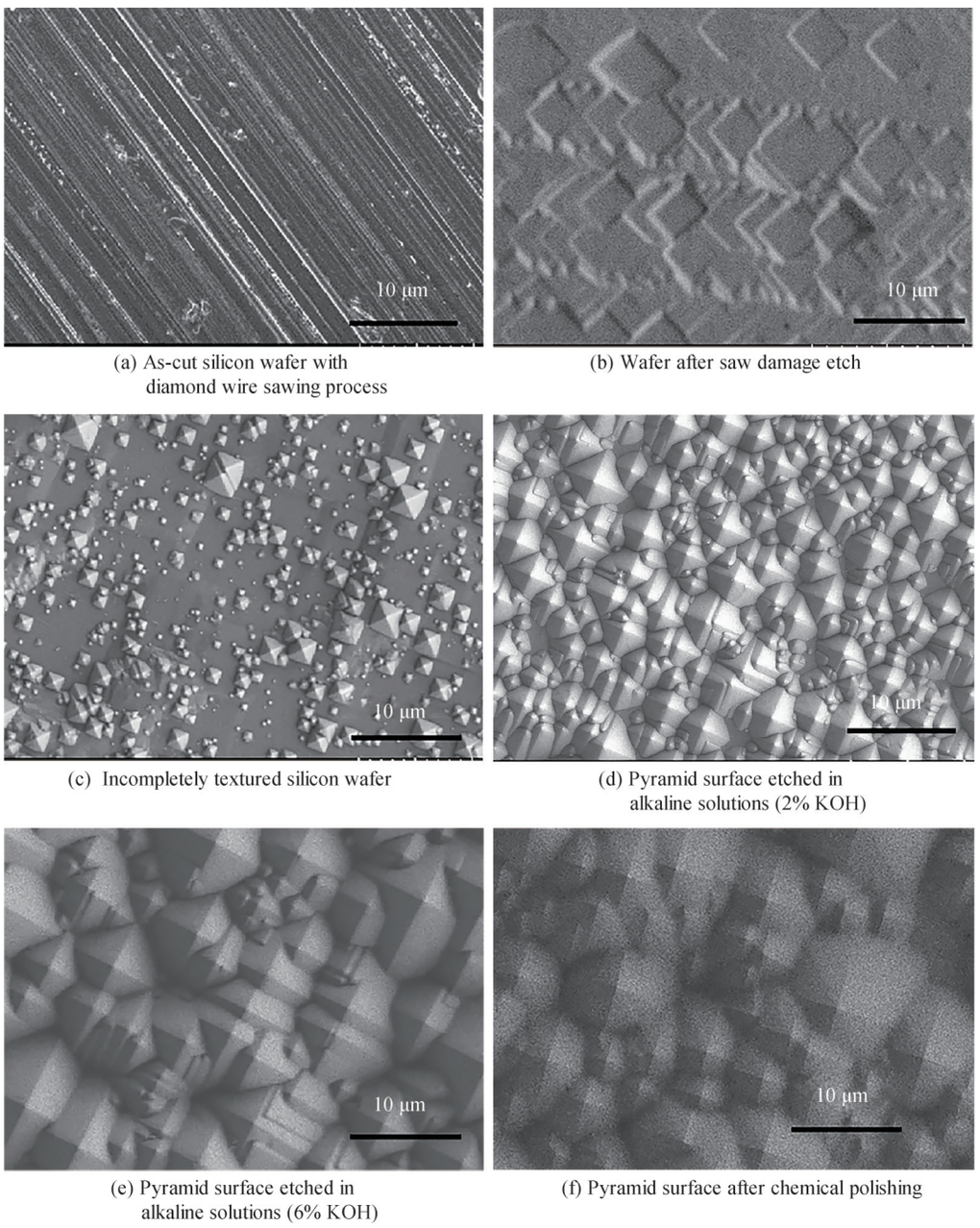


Fig. 1 Structure and process flow of SHJ solar cell

2.2 Wet-chemical treatment

Wet-chemical processes include removal of saw damage and a random pyramid surface texture etching. Sawing of the monocrystalline Si ingot into wafers contaminates the surfaces with the cutting slurry and creates crystal damages at the surfaces, as seen in Fig. 2(a). Thorough cleaning of the wafer and the complete removal of such saw damages are essential prerequisites for the reduction of recombination losses in Si solar cell. Fig. 2(b) shows an etching removal of at least 10 μm on each side to decrease effectively the surface roughness and to obtain the characteristic crystallographic features of the Si (100) surface[12].

To improve the light trapping and thereby enhance the short-circuit current densities of the SHJ solar cell, particular emphasis is put on the wet-chemical random pyramid texturization of the solar cell substrates. Moreover, defects and contaminations on the surface can already be drastically reduced during the texturing process. Surface texturing is conventionally achieved by anisotropic wet-chemical etching of Si(100) wafers in alkaline solutions containing Isopropyl Alcohol (IPA) as an additive. Pyramid formation is due to the anisotropic reaction of alkali and silicon. In a certain concentration of alkaline solution, the reaction speed of OH^- with the (100) surface of silicon is faster than that of the (111) surface. That is why the pyramid structure is formed[13]. Fig. 2(c) shows the etched surface of silicon wafer possibly due to low concentration KOH, short time etching or too much IPA additive. The typical process temperature is 70～80℃ below IPA boiling temperature, the nature of IPA is a stronger wetting function of the surface. This feature promotes a more homogeneous surface structure and allows to tune the pyramid size distribution. It is found the main factor that influence on the pyramid size is concentration of KOH in alkaline solutions. This behaviour can be explained by the morphological differences shown in the sequence of Scanning Electron Micrographs (SEM). Fig. 2(d) and (e) show the pyramid surface of wafers etched for 20 min in alkaline solutions with 2 wt% and 6 wt% KOH. The average pyramid sizes etched with 2 wt% KOH alkaline solution is around 2～4 μm, which increased to in the range of 6～9 μm etched with 6 wt% KOH alkaline solution. To smooth pyramid valleys and edges and increase crystallographic imperfections, the textured wafer was chemically polished with mixture solution of 95% HNO_3 and 5% HF. Fig. 2(f) shows the morphological structure of textured surface after chemical polishing process. The distribution of the pyramids become more homogeneous, which is beneficial for wafer passivation by depositing intrinsic hydrogenated amorphous silicon film.



(a) As-cut silicon wafer with diamond wire sawing process

(b) Wafer after saw damage etch

(c) Incompletely textured silicon wafer

(d) Pyramid surface etched in alkaline solutions (2% KOH)

(e) Pyramid surface etched in alkaline solutions (6% KOH)

(f) Pyramid surface after chemical polishing

Fig. 2 SEM image of as-cut silicon wafer, wafer after saw damage etch, incompletely textured wafer, pyramid surface etched in 2% and 6% alkaline solutions and after chemical polishing

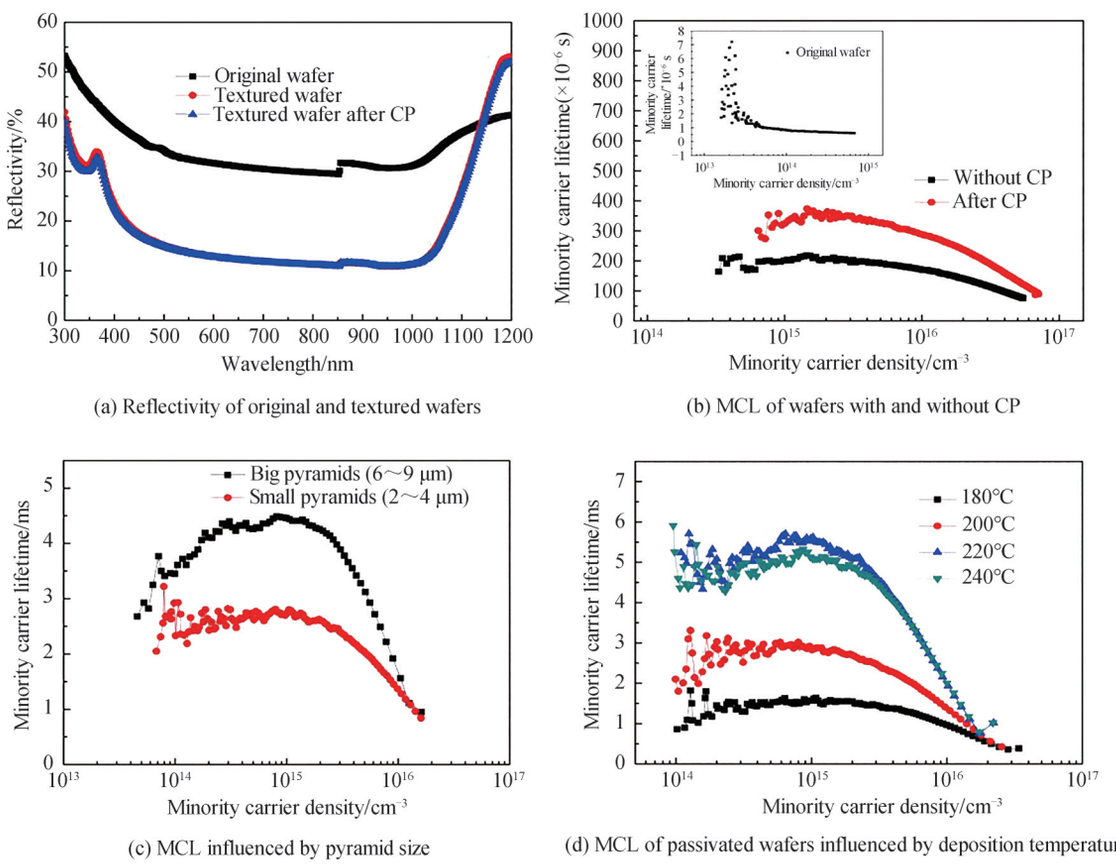
2.3 Interface passivation

Key feature of SHJ solar cell concept is a thin intrinsic amorphous hydrogenated silicon ((i) a-Si:H) layer which forms the heterocontact with a crystalline silicon (c-Si) wafer, provides passivation of the a-Si:H/c-Si interface, thus enables high open-circuit voltages (Voc). Further optimization of the a-Si:H/c-Si interface lead to an increase of the Voc, thereby an improvement of the solar cell performance[14]. A common technique to characterize the interface quality is to measure the carrier lifetime τ_{eff} as a function of the minority excess charge carrier density Δn by means of Transient Photoconductance Decay (TrPCD)[15].

Fig. 3(a) shows the reflectivity spectra of original, untreated textured wafers and textured wafers due to Chemical Polishing(CP). Obviously, the reflectivity of the textured c-Si wafer is around 10%, much lower than the raw wafer. Consequences of the texture-related improvement of the optical properties are both increase of the effective surface area and improved light trapping. After chemical polishing, the pyramid size distribution become more uniform, yielding lower reflection (Fig. 3(a)) than untreated textured wafer. After optimizing

the texturization, the following process step is the cleaning of the wafer with RCA method. The Minority Carrier Lifetime (MCL) of textured wafer after cleaning was measured. As shown in Fig. 3(b), the MCL of as-cutting raw wafer is only 0.8 μs (inset of Fig. 3(b)), but the MCL of the textured wafer after cleaning and terminating with HF was more than 200 μs at an injection level of 1×10^{15} cm^{-3}, which increased to 300 μs for the wafer underwent CP process. It is the fact that the wafer treated with CP was cleaner than the untreated wafer, because too small pyramids were eliminated and surfaces of the pyramids became smoothing after chemical polishing.

Optimization of texturization and cleaning was followed by intrinsic a-Si:H layers deposition, which are known to provide excellent passivation of the c-Si surfaces, causing a decrease of interface state density, mainly by hydrogenation of silicon dangling bonds. The a-Si:H thin film samples were prepared in a Radio Frequency (RF) 13.56 MHz and power density of 0.16 W/cm^2 capacitive-coupled PECVD system. We deposited the textured wafer with the percentage content of silane SiH_4 and dydrogen H_2 at 220℃ under the chamber pressure of 1.5 (1 Torr=133.322 Pa). To get a high quality of a-Si:H passivated wafer, the window of deposition process is rather narrow. The influence of pyramid size on the effective minority charge carrier lifetime τ_{eff} after passivating with a-Si:H layer is summarized in Fig. 3(c). Samples with small size pyramids around 2~4 μm show lower carrier lifetimes of $\tau_{eff} < 2.5$ ms, samples with pyramids around 6~9 μm reach higher values of up to 4.6 ms. For small pyramid wafer, the lifetime is limited by the increased influence of the valleys and edges which are known to be centres of epitaxial growth as well as starting points of local cracks in the (i) a-Si:H layer[16]. τ_{eff} rises with increasing fraction of bigger pyramids due to the lower density of pyramid free areas with (100) orientation, pyramid valleys and edges. It is indicated that 6~9 μm was suitable pyramid size for c-Si wafer passivation. Above a certain threshold, a further increase in pyramid size does not lead to a concomitant increase of the charge carrier lifetime and it is suggested that on textured surfaces with large pyramids the recombination processes at defects on the pyramid facets dominate the overall interface recombination[17].



(a) Reflectivity of original and textured wafers

(b) MCL of wafers with and without CP

(c) MCL influenced by pyramid size

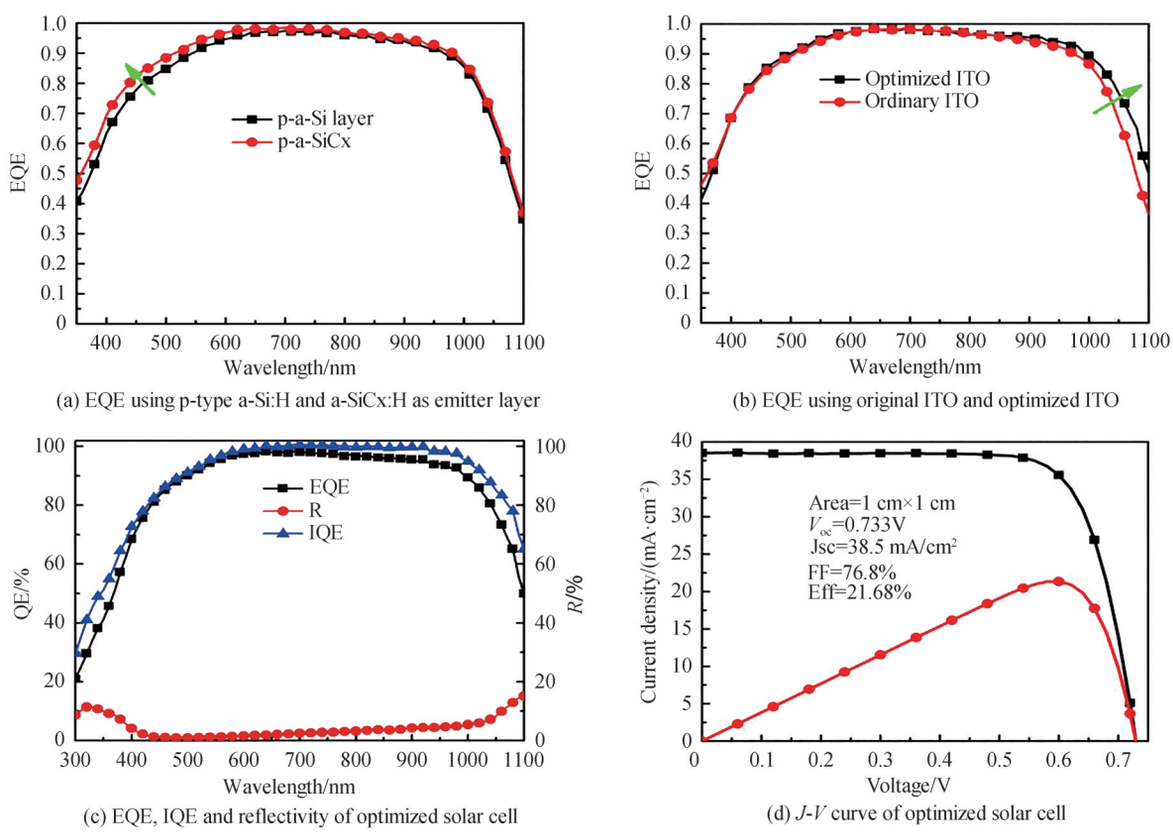
(d) MCL of passivated wafers influenced by deposition temperatures

Fig. 3 Reflectivity of original and textured wafers, MCL of passivated wafers affected by chemical polishing, pyramidsize and a-Si:H deposited at different temperatures

The influence of the deposition temperature on τ_{eff} of textured c-Si wafers is shown in Fig. 3(d). It was found that increasing the temperature up to 220℃ leads to an increase of the charge carrier lifetime to a maximum value of 5.5 ms, which is promoted by the passivation of the (i) a-Si:H/c-Si interface by the highly mobile hydrogen. At 220℃ a trade-off between hydrogen concentration and mobility is reached, as has been confirmed by optical measurements that at lower substrate temperatures the (i) a-Si:H layer contains larger amounts of hydrogen[18]. However, at lower temperatures diffusion is limited and accordingly interface passivation is suppressed, which results in lower charge carrier lifetimes. Beyond 220℃ there is a decrease of τ_{eff}, possibly due to the lower hydrogen concentration or to increased interface recombination caused by local epitaxial growth, which is known as being detrimental for passivation[19]. Consequently, at T_{sub}=220℃ the largest carrier lifetimes are obtained owing to a high-quality (i)a-Si:H layer and a well passivated interface. At deposition temperatures >220℃ no improvement occurs due to partial deterioration of the a-Si:H interface[16].

2.4 Emitter and ITO optimization

In order to improve short wavelength photoresponse, p-type a-SiCx:H emitter was used in the SHJ solar cell absorption alternative to p-type a-Si:H[20]. Due to its broad band gap, the EQE of SHJ solar cell with p-type a-SiCx:H as emitter layer in short wavelength range of 300 to 600 nm is significantly higher than using p-type a-Si:H, as seen in Fig. 4(a).



(a) EQE using p-type a-Si:H and a-SiCx:H as emitter layer

(b) EQE using original ITO and optimized ITO

(c) EQE, IQE and reflectivity of optimized solar cell

(d) *J-V* curve of optimized solar cell

Fig. 4 Performances of SHJ solar cells

Eventually ITO layers were deposited on top Nip and back niN of the layer stack, respectively. ITO parasitic absorption in SHJ solar cell mainly includes the belt edge absorption and free carrier absorption. The former mainly affects the absorption of SHJ in the short wave region, while the latter affects the absorption in the long wave region. By 200℃ annealing after both the rear and front side ITO deposition, the ITO layer doping concentration was optimized to obtain a trade-off between low parasitic free-carrier absorption and low resistivity. The resistivity of 2.5×10^{-4} Ω·cm, highest carrier mobility of 31.8 $cm^2\cdot V^{-1}\cdot s^{-1}$ and carrier concentration of 6.9×10^{20} cm^{-3} were obtained at Ar(O_2) gas flow rate of 20 Sccm with the working pressure of 0.002 Torr. Using the optimized ITO layer with high charge carrier mobility and low resistivity in SHJ solar cell, the long wavelength response was obviously enhanced due to decrease of free carrier absorption, as shown

in Fig. 4(b). In comparison to EQE data obtained for front- and rear-emitter silicon heterojunction solar cells on n- and p-type wafers presented recently by DESCOEUDRES A et al.[21], our cell suffers from losses in the long wavelength range (>1 000 nm) due to parasitic absorption in the doped ITO layer at the back side. By controlling the thickness of ITO at 100 nm, the reflectivity of the solar cell was further decreased, as shown in Fig. 4(c).

After metallic contacts were prepared and the characteristics of the solar cell were determined, the $J-V$ curves of the 1 cm×1 cm cells were measured under standard test conditions with a shadow mask. The results of the best solar cell are given in Fig. 4(d), which shows a rather high efficiency above 21.68% after all the optimized processes. Thanks to excellent surface passivation, the V_{oc} reaches 733 mV. The J_{sc} in $J-V$ curve is well consistant with the J_{sc} integrated according to EQE (Fig. 4(c)). The fill factor is 76.8%, which is limited by thermal deposition of metallic contacts, the use of the silk-screen printing would be beneficial for further improvement of the solar cell.

4 Conclusion

Step-by-step optimization were analysed throughout the processing of SHJ solar cells starting from the pyramid structure etched Si wafer to the complete solar cell. Based on this investigation, recombination losses were successfully minimized and high open-circuit voltages and fill factors were obtained. Power conversion efficiencies above 21.68% were achieved by optimization of the texturing of silicon wafers, interface passivation, broad band gap emitter and ITO adjusting. The use of the silk-screen printing would be beneficial for further improvement of the solar cell.

References

[1] JULIE D, QUENTIN J, JEAN C, et al. 23.5%-efficient silicon heterojunction silicon solar cell using molybdenum oxide as hole-selective contact[J]. Nano Energy, 2020, 70(4): 104495.

[2] DESCOEUDRES A, HORZELl J, PAVIET-SALOMON B, et al. The versatility of passivating carrier-selective silicon thin films for diverse high-efficiency screen-printed heterojunction-based solar cells[J]. Progress in Photovoltaics: Research and Applications, 2020, 28(6): 569-577.

[3] GERENTON F, EYMARD J, HARRISON S, et al. Analysis of edge losses on silicon heterojunction half solar cells[J]. Solar Energy Materials & Solar Cells, 2020, 204: 110213.

[4] YOSHIKAWA K, KAWASAKI H, YOSHIDA W, et al. Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%[J]. Nature Energy, 2017, 2: 817032.

[5] TAGUCHI M, YANO A, TOHODA S, et al. 24.7% record efficiency HIT solar cell on thin silicon wafer[J]. IEEE Journal of Photovoltaics, 2014, 4(1): 96-99.

[6] YANG Zhenhai, YANG Xi, LIN Hao, et al. The role of transition region charges between dopant-free asymmetric heterocontacts in interdigitated back contact silicon heterojunction solar cells[J]. Solar Energy, 2019, 188(8): 1201-1208.

[7] YANG Zhenhai, LIN Hao, SHENG Jiang, et al. Design principles of silicon heterojunction solar cells with dopant-free interdigitated back contacts[J]. Solar RRL, 2019, 3(11): 1900230.

[8] WOLF S D, KONDO M. Abruptness of a-Si: H/c-Si interface revealed by carrier lifetime measurements[J]. Applied Physics Letters, 2007, 90(4): 042111.

[9] KORTE L, CONRAD E, ANGERMANN H R, et al. Advances in a-Si: H/c-Si heterojunction solar cell fabrication and characterization[J]. Solar Energy Materials & Solar Cells, 2009, 93(6-7): 905-910.

[10] WOLF S D, DESCOEUDRES A, HOLMAN Z, et al. High-efficiency silicon heterojunction solar cells: a review[J]. Green, 2012, 2: 7-24.

[11] KOIDA T, FUJIWARA H, KONDO M. Reduction of optical loss in hydrogenated amorphous silicon/crystalline silicon heterojunction solar cells by high-mobility hydrogen-doped In_2O_3 transparent conductive oxide [J]. Applied Physics Express, 2008, 1(4): 04501.

[12] STEGEMANNA B, KEGEL J, MEWS M, et al. Evolution of the charge carrier lifetime characteristics in crystalline silicon wafers during processing of heterojunction solar cells[J]. Energy Procedia, 2014, 55: 219-228.

[13] NISHIMOTO Y, NAMBA K. Investigation of texturization for crystalline silicon solar cells with sodium carbonate solutions[J]. Solar Energy Materials & Solar Cells, 2000, 61(4): 393-402.

[14] DING Yueke, HUANG Shihua. Study on passivation of monocrystalline silicon by tandem hydrogenated amorphous silicon film[J]. Acta Photonica Sinica, 2021, 50(3): 0331001.

[15] LEENDERTZ C, MINGIRULLI N, SCHULZE T, et al. Discerning passivation mechanisms at a-Si: H/c-Si interfaces by means of photoconductance measurements[J]. Applied Physics Letters, 2011, 98(20): 202108.

[16] KEGEL J, ANGERMKANN H, STURZEBECHER U, et al. IPA-free texturization of n-type Si wafers: correlation of

optical, electronic and morphological surface properties[J]. Energy Procedia, 2013, 38(7): 833-842.
[17] OLIBET S, MONACHON C, HESSLER-WYSER A, et al. Textured silicon heterojunction solar cells with over 700 mV open-circuit voltage studied by transmission electron microscopy[C]. 23rd European Photovoltaic Solar Energy Conference, 2008:1140.
[18] STEGEMANN B, KEGEL J, MEWS M, et al. Passivation of textured silicon wafers: influence of pyramid size distribution, a-Si:H deposition temperature, and post-treatment[J]. Energy Procedia, 2013, 38(7): 881-889.
[19] WOLF S D, FUJIWARA H, KONDO M. Impact of annealing on passivation of a-Si:H / c-Si heterostructures[C]. 33rd IEEE Photovoltaic Specialists Conference, 2008.
[20] ZHANG D, DELIGIANNIS D, PAPAKONSTANTINOU G, et al. Optical enhancement of silicon heterojunction solar cells with hydrogenated amorphous silicon carbide emitter[J]. IEEE Journal of Photovoltaics, 2014, 4(6):1326-1330.
[21] DESCOEUDRES A, HOLMAN Z C, BARRAUD L, et al. >21% efficient silicon heterojunction solar cells on n- and p-Type wafers compared[J]. IEEE Journal of Photovoltaics, 2013, 3(1): 83-89.