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集成大面积光电探测器接收芯片的优化设计

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摘 要:通过仿真优化探测器的结构参数和性能,设计了基于 0.25 μm 标准 BCD (Biplor,CMOS and DMOS)工艺的大面积多叉指状 PIN 光电探测器.选择已优化的大面积光电探测器用于和跨阻放大器以及后端放大器单片集成,采用 0.25 μm BCD 工艺实现了一个用于 650 nm 塑料光纤通信的单片集成光接收芯片.结果表明:多叉指状 PIN 光电探测器对 650 nm 入射光的响应度提高至 0.260 A/W,其结电容降低至 4.39 pF.对于 650 nm 的入射光,在速率 250 Mb/s、误码率小于 10^{-9} 的条件下,光接收芯片的灵敏度为 −23.3 dBm,并得到清晰的眼图.该光电探测器可用于宽带接入网中的高速塑料光纤通信系统的光接收芯片中.

关键词:塑料光纤通信;光接收芯片;多叉指 PIN;光电探测器;BCD 工艺
中图分类号:TN49.1;TN303 **文献标识码**:A **文章编号**:1004-4213(2015)04-0423001-6

Realization of a High Sensitivity Fully-integrated Receiver with Optimized Large-area Photodetector

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Abstract: Multi-finger PIN photodetector was designed and optimized in a standard 0.25 μm BCD (Bipolar,CMOS and DMOS) process. The optimized large-area multi-finger structure PIN photodetector was applied in the monolithic optoelectronic receiver with a trans-impedance amplifier and a pre-amplifier. Based on simulation and test results, it is shown that 650nm responsibility of PIN photodetector is improved up to 0.260 A/W and the junction capacitance is decreased down to 4.39pF for the multi-finger structure. The receiver achieves a sensitivity of −23.3 dBm with the bit-error-rate of 10^{-9} at 250 Mb/s at 650 nm. A clear eye diagram of the proposed receiver is demonstrated for 250 Mb/s. Results indicate that the monolithic optical receiver can be applied to 250 Mb/s plastic optical fiber communication.

Key words: Plastic optical fiber communication; Optical receiver; Multi-finger PIN; Photodetector; BCD process
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0 Introduction

With the recent explosive demands for broadband access home communication systems, the standard 1mm core Step-Index Plastic Optical Fiber (SI-POF) is gradually used as a low-cost home networking solution. Compared to Glass Optical Fiber (GOF), POF possesses a greater flexibility and resilience to bending, shock and vibration, more easy to use and relatively low cost. These advantages make POF very popular in short-range optical communication, such as in Media Oriented System Transport (MOST), industrial control and so on [1-4]. As the need for higher data rate home networking grows, more efforts such as monolithic integrated optical receiver and relevant key technology are being put into the development of high-speed POF-based fast ethernet system[5-7].

The physical property of silicon allows the material to be sensitive for wavelengths between 400 nm and 1 100 nm. Since silicon material has a certain response to the wavelength of 650 nm, optical receiver for POF system is feasible to realize the monolithic integration of photodetector (PD) and pre-amplifier in the standard Si-based technology[8-10]. Furthermore, for the large core diameter close to 1 mm of a typical POF cable, a large-area PD integrated in IC standard technology is desired for low-cost high-efficiency light coupling which brings high junction capacitance and large noise[11]. Based on the analysis of PDs proposed in this paper and our former research results[12], an optimized PD with large area, a Tran-Impedance Amplifier (TIA) and a post amplifier have been applied to implement a monolithic integrated in 0.25 μm standard Bipolar, CMOS and DMOS (BCD) technology.

1 Multi-finger P+/N-EPI/BN+ PD

1.1 Structure of PDs

The simple structure of P^+/N-EPI/BN^+ (PIN) PD are depicted in Fig. 1, the insulated medium layers (SiO_2 and Si_3N_4) in BCD technology are not shown. The N-EPI layer with the resistivity of 3.5 Ω·cm forms the I-finger layer, strictly speaking, where I-layer is not a real intrinsic layer but a low doped N epitaxial layer. The N^+ region on the N-well connect with BN^+ buried layer acts as cathode. The P^+ region on the N epitaxial layer acts as anode.

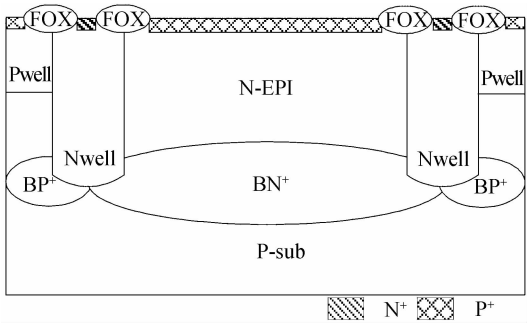


Fig. 1 Simple sectional view of PIN PD

As the area of PIN PD is as large as 200×200 μm², which brings high junction capacitance and large noise, a structure of multi-finger PIN PD has been proposed to boost the speed of the PD at a cost of light loss to reduce the junction capacitance of PD. The simple sketch of multi-finger PIN photodiode under the BCD technology is shown in Fig. 2, P^+ is made into the shape of multi-finger. The P^+ fingers on the N epitaxial layer are combined to a common anode, and N^+ fingers on the N-Well connecting with BN^+ buried layer act as cathode. The multi-finger PIN PDs with different photosensitive area have different number and width of finger.

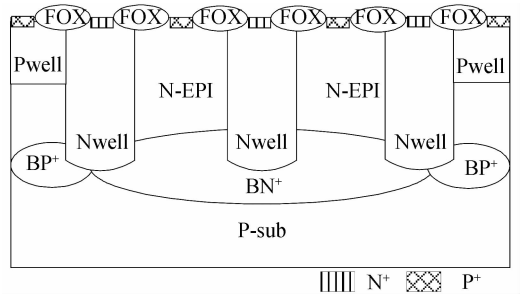


Fig. 2 Simple sectional view of multi-finger PIN PD

1.2 Optimization of multi-finger PIN PD

Fig. 3 is the one-dimension physical structure of single finger for PIN PD. From left to right is the passivation layer and dielectric layer (Si_3N_4 and SiO_2), P^+ (thickness x_s), N-EPI (thickness x_N), BN^+ (thickness x_{BN}), P-Sub in BCD process. The quantum efficiency is improved by antireflection layer. By adding N epitaxial layer, with the width of depletion region increasing, the absorption of light is improved.

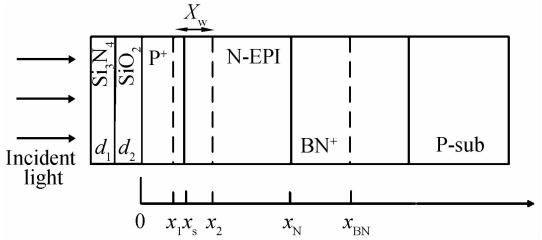


Fig. 3 The physical structure of single finger for PIN PD

As some layers of PD can not be defined by parameters directly, it's simplified to build PD structure using Atlas for simulation. Therefore models constructed by software Athena make the simulation results more reliable. Because of the limitation of simulation software, the area of PD simulated cannot be larger than 50 × 50 μm². It's possible for us to get characteristic of PD whose area is 200 × 200 μm² based on the simulation results.

As the number of P^+ fingers affects the performance of multi-finger PIN detector directly, the structures with different number of P^+ fingers are modeled in software Athena and the number of P^+ fingers varies from 1 to 6. AC characteristic of PDs are simulated in software Atlas based on the models which have been constructed.

Fig. 4 is AC characteristic curves of multi-finger PIN PD with different number of fingers. Obviously, the bandwidth of 3 fingers PIN PD is larger than any other PD, and the bandwidth is as large as 1.2 GHz.

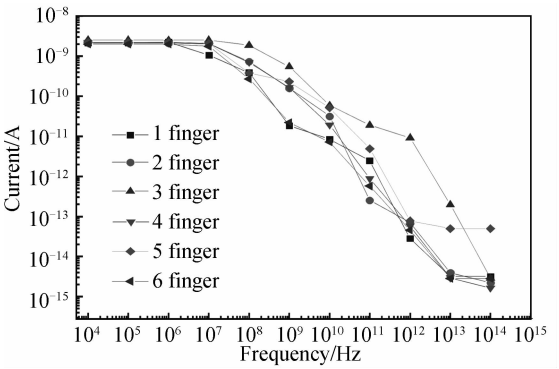


Fig. 4 AC characteristic curves of multi-finger PIN PD with different number of fingers

Bandwidth is affected by the junction capacitance of PD directly, and it decreases with the junction capacitance increasing. Because lateral diffusion junction capacitance can't be ignored, considering the junction capacitance formed by P^+/N-EPI/BN^+, total capacitance C_t can be expressed as Eq. (1)[13].

$$C_t = C_a A_a + C_p A_p \tag{1}$$

A_a is the area of P^+, and A_p is the lateral area;

$$A_a = l \times w_n \times n \tag{2}$$

$$A_p = l \times h \times 2n \tag{3}$$

where n is the number of P^+ finger; l, h and w_n represent the length, the thickness and the width of each P^+ finger, respectively, l and h are both constant, while w_n decreases with n increasing. C_a is unit-area capacitance, C_p is unit-area lateral diffusion capacitance. C_a can be expressed as Eq. (4),

$$C_a = \frac{\varepsilon_s}{x_w} = \sqrt{\frac{\varepsilon_s q N_A N_D}{2(N_A + N_D)(V_{bi} - 2KT/q - V)}} \tag{4}$$

where ε_s is dielectric coefficient of silicon. The depletion region depth x_w determines C_{pd} strongly. N_D and N_A represent donor and acceptor concentration, respectively. V_{bi} is built-in potential. V is bias voltage of capacitor considering the influence of series resistance. A_a increases but A_p decreases with n increasing. The junction capacitance of 3 fingers PIN PD is proved to be minimum by calculating and comparing total capacitance of PDs with different number of fingers. It gives us a reasonable explanation for the maximum bandwidth of 3 fingers PIN PD.

As the width of P^+ finger and the spacing between each P^+ finger affect the performance of multi-finger PIN detector as well, the structures with different sizes are also modeled in Athena. Optical spectrum response and AC characteristic of PDs are simulated on the models. Finally, an optimized 3 fingers PIN PD with preferable width and spacing of P^+ finger is achieved by simulating optical spectrum and AC characteristic.

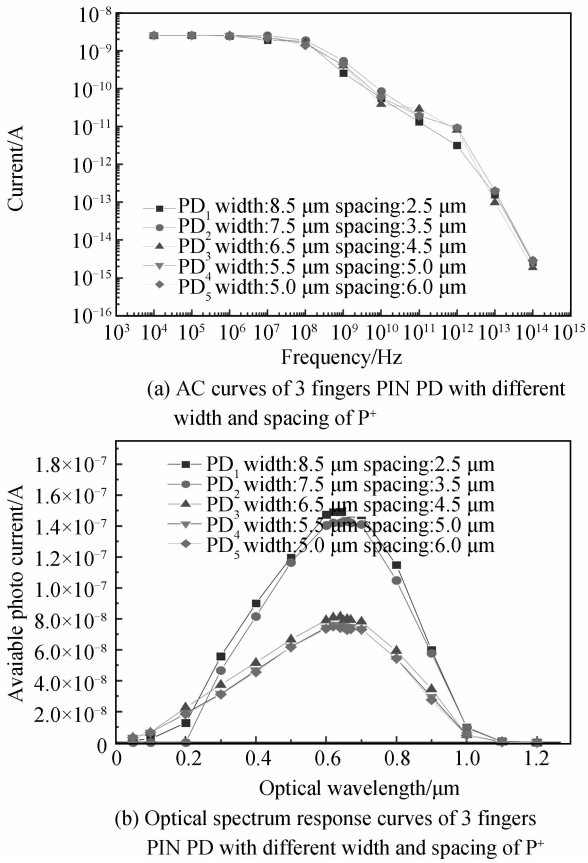
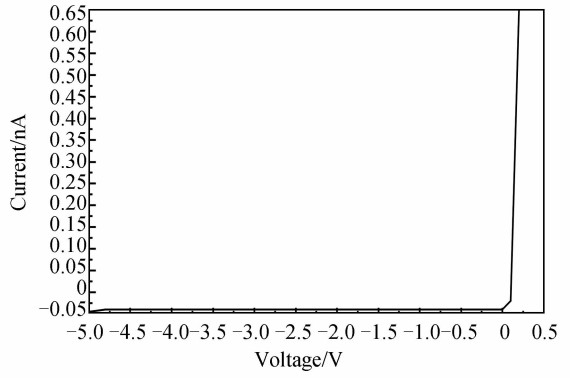


Fig. 5 AC and optical spectrum characteristic of PD

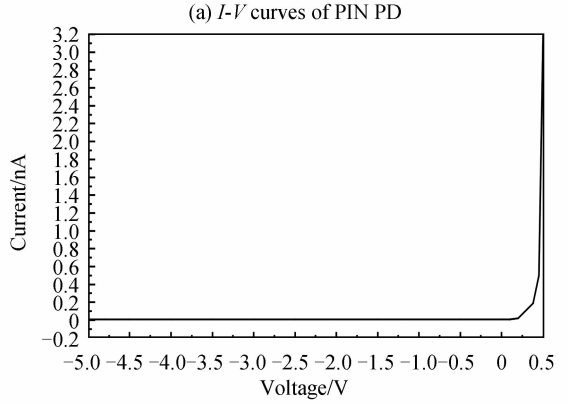
Fig. 5(a) and (b) are AC characteristic curves and optical spectrum response curves of 3 fingers PIN PD with different width and spacing of P^+ finger. Obviously, photo currents of PD_1 and PD_2 are similar, and they are larger than that of other PDs to a large degree, while the bandwidth of PD_1 is not large enough. It can be seen that the bandwidth of PD_2 is larger than that of the other PDs to some degree, for the reason that with the area of P^+ increasing larger photosensitive area contributes to larger photo current. Besides, large photosensitive area also contributes to large junction capacitance, so there's a compromise between the bandwidth and the photo current of PD, which explains why the bandwidth of PD_1 is not as large as that of PD_2. It's easy to get the largest responsibility of PD_2 is 0.355 A/W at the wavelength of 650 nm according to the optical power (1 mW) and the area of PD (50×50 μm^2).

1.3 Experimental results of PD

Different sizes of PDs have been fabricated in 0.25 μm standard BCD technology. The *I-V* curve, optical spectrum responsivity and the junction capacitance of the PDs are measured. Fig. 6(a) and (b) are *I-V* curves of 200×200 μm² PIN PD and multi-finger PIN PD, respectively. The forward threshold voltages of PIN PD and multi-finger PIN PD are almost 0.4 V for Silicon material and their breakdown voltages is 24 V.



(a) *I-V* curves of PIN PD



(b) *I-V* curves of multi-finger PIN PD

Fig.6 *I-V* curves of PIN PD

Fig. 6 *I-V* curves of PD

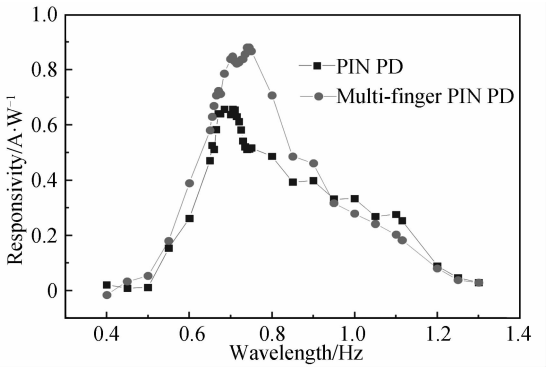


Fig. 7 Tested optical spectral response curves of PIN PD and multi-finger PIN PD

As is shown in Fig. 7, the peak in optical spectral response curve of PIN PD and multi-finger PIN PD are at 700 nm. The absorption in shorter wavelengths range of 600 nm～700 nm become more intense and more photo-generated current are generated consequently. At the wavelength of 650 nm, responsivities of PIN PD and multi-finger PIN PD are 0.251 A/W and 0.260 A/W under 2.5 V reverse bias, respectively. Thus, the PD structures presented in this paper are more suitable for detecting the wavelength range of 600 nm～700 nm.

Table 1 shows the tested capacitances of the two kinds of PDs with different areas under the reverse bias of 2.5 V. It can be seen that the capacitance of multi-finger PIN-PD is smaller than that of PIN-PD with the same size. Furthermore, the junction capacitance of the same structure increases with the area of PD increasing.

Table 1 Tested capacitances of different structures with different area

Area/μm²	50×50	200×200	300×300	500×500
PIN-PD	0.35 pF	8.20 pF	12.7 pF	28.9 pF
Multi-finger PIN-PD	0.15 pF	4.39 pF	6.7 pF	15.21 pF

2 The proposed optical receiver

2.1 Design of optical receiver

Fig. 8 shows the block diagram of the monolithic integrated receiver. It consists of two integrated multi-finger PIN PDs, an illuminated signal PD and a shielded dummy PD, a Trans-Impedance Amplifier (TIA), a limiting amplifier and an output buffer. The area of each PD is 200×200 μm² to meet with the large core plastic optical fiber. A signal PD and a shielded dummy PD are used with a differential pre-amplifier. The incident light is focused only onto the signal PD. The cathode of PDs are the input signal of TIA, and the anode of PDs are connected with the ground of circuit, the reverse bias of PD is approximately the output DC operating points of the receiver chip. A true-differential pre-amplifier usually exhibits a high common-mode Z_{in}, which provides high-frequency Common Mode Rejection Ratio (CMRR). Compared with a single-ended pre-amplifier approach, the adopted approach has the benefits of having a fully balanced structure, good high-frequency CMRR, and better immunities to supply and ground noises at the cost of doubled input-referred noise current power.

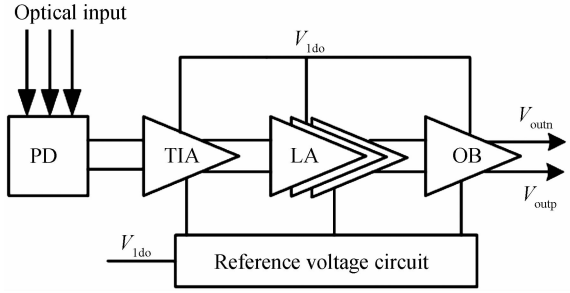


Fig. 8 Structure diagram of optical receiver

The TIA converts the output current of PD into voltage signal. In order to provide a low-enough Z_{in} with reasonable DC current and input-referred noise, a TIA shown in Fig. 9 is proposed to combine the benefits of Regulated Cascade (RGC) buffer and Wilson-sense (MWS) buffer. M_1, M_2 and R_1, R_2 form Common-Source (CS) amplifiers which apply inverted and amplified input signal to the gates of M_3, M_4. Thus, the effective g_m of M_3/M_4 is increased and the Z_{in} is reduced. M_1 and R_1 form a CS stage which drives the gate of M_3 with a non-inverted, amplified copy of the input signal. Thus, M_3 becomes the input transistor that absorbs the signal current. The MWS buffer provides a similar Z_{in} and noise with only half of the bias current. The highest voltage stack in a TIA is the V_{gs3} plus the voltage across R_1. As a result, the MWS buffer can work with low supply voltages.

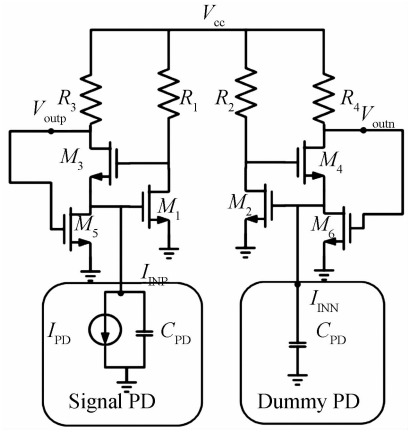


Fig. 9 Schematic of trans-impedance amplifier

The post amplifier amplifies the output of TIA up to the desired swing level, it includes the three cascaded modified Cherry-Hooper amplifiers and an out buffer. Modified Cherry-Hooper amplifiers can increase the gain without a corresponding decrease in bandwidth. In order to reduce the input capacitance of difference without reducing its gain, frequency multiplier is employed as an out buffer, as is shown in Fig. 10. If the parasitic capacitance between node A and node B is ignored, the input capacitance is only $C_{GS}/2$. Therefore, frequency multiplier can be used to provide the same voltage gain with only half of the input capacitance. The load resistor of frequency multiplier is 50 Ω to match the transmission line impedance.

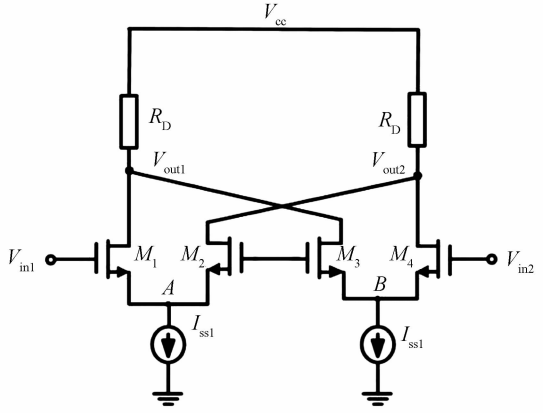


Fig. 10 Schematic of frequency multiplier

2.2 Simulated results

The AC characteristic curves of whole receiver shown in Fig. 11 are simulated in Spectre environment. The input signal has pulse period of 2 ns and magnitude of 5 μA. The DC current of 10 μA and the junction capacitance of 5 pF are applied to the simulation. It can be seen from the AC curves that the −3 dB bandwidth of the whole receiver is 484.23 MHz, and the gain is 66.5 dBΩ.

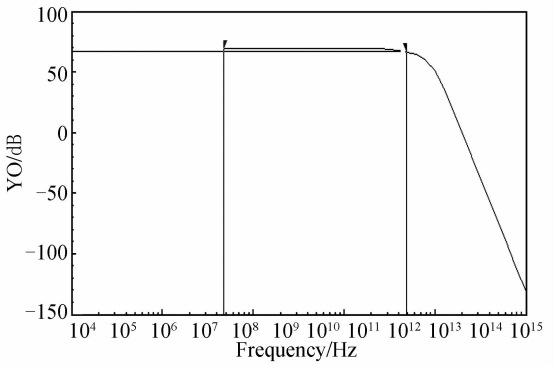


Fig. 11 Simulated AC characteristic curve

2.3 Experimental results

The optical receiver is implemented in low-cost 0.25 μm BCD technology for POF communication. Fig. 12 is the layout of the monolithic integrated optical receiver chip with 200×200 μm^2 optimized multi-finger PIN PD, and Fig. 13 is its micro-photography. The whole receiver chip occupies the area of 0.99 mm^2.

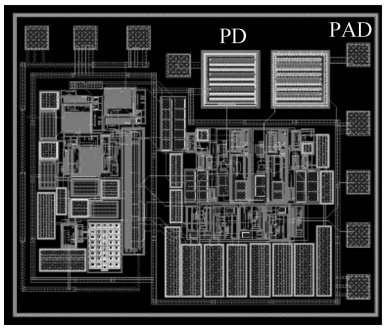


Fig. 12 Layout of optical receiver

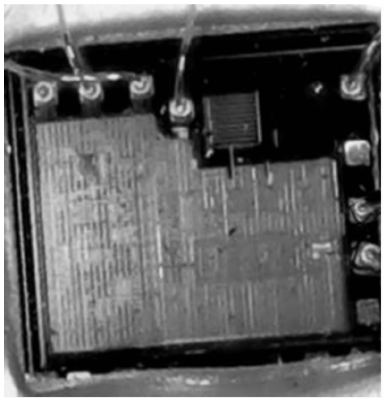
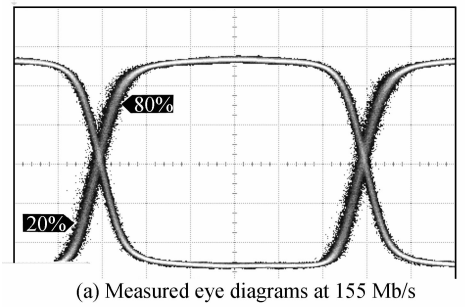
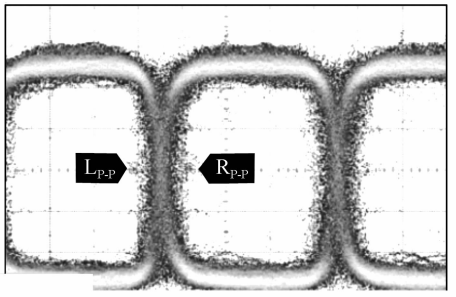


Fig. 13 Microphotography of optical receiver

The output DC operating points of the receiver chip with and without illumination are 3.53 V and 3.61 V, respectively. The gain of the receiver is 2.05 kΩ calculated by the difference of DC voltage of the whole chip and the responsivity at 650 nm. The value is very close to the simulated gain of 66.5 dBΩ. Fig. 14 are eye diagrams of the receiver at the speed of 155 Mb/s and 250 Mb/s, respectively. The rise time is 801 ps, the fall time is 787 ps and the period jitter is 441 ps at 250 Mb/s. It operates with a supply voltage of 5 V and consumes only 100 mW.



(a) Measured eye diagrams at 155 Mb/s



(b) Measured eye diagrams at 250 Mb/s

Fig. 14 Measured eye diagrams of the receiver

Fig. 15 illustrates the conceptual block diagram of sensitivity testing for POF optic link. PRBS signal generated by Agilent 81 250 Bit Error Rate (BER) tester comes into the optical transmitter to convert electrical signal into optical signal whose power is controlled by attenuator, and the optical signal is received by optical receiver and return to BER tester. If the BER of receiver output signal less than given BER (usually BER is at least 10^{-9}), BER tester displays "PASS", attenuating the power of optical signal until "PASS" jumps to "FAIL", this power of optical signal is the sensitivity of optical receiver. The sensitivity measured is −23.3 dBm under the BER of 10^{-9} at 250 Mb/s.

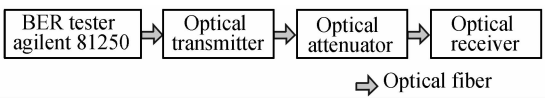


Fig. 15 Conceptual block diagram of sensitivity testing

4 Conclusion

The simulated and measured characteristics of receiver are achieved. Based on the analysis of the optical spectrum and AC characteristic of PD, an multi-finger P^+/N-EPI/BN^+ PD is optimized. The low-cost monolithic integrated receiver with an optimized 200×200 μm^2 multi-finger PIN PD, a TIA, and a post amplifier for 650nm POF communication is fabricated in 0.25 μm BCD Technology. Measured results indicate that the responsivity of optimized 200×200 μm^2 multi-finger PIN PD is 0.260 A/W at 650 nm and the capacitance is 4.39 pF under the reverse bias of 2.5 V. The monolithic integrated receiver operates with a supply voltage of 5 V and consumes 100 mW. At 250 Mb/s and BER of 10^{-9}, the sensitivity is −23.3 dBm and a clear eye diagram of the proposed receiver are demonstrated. These indicate that the receiver chip can be employed in 250 Mb/s POF-based Fast Ethernet system for broadband access network application.

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