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金刚石线锯切割多晶硅片的气相刻蚀制绒研究

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摘 要:采用气相刻蚀制绒法研究金刚石线锯切割多晶硅片制绒.加热体积比 1:3、总体积 400 mL 的 $HF\text{-}HNO_3$ 酸混合溶液到 90 ℃,使酸混合溶液受热产生气相,利用气相对金刚石线锯切割多晶硅片表面进行制绒.结果表明,制绒 15 min 之后,硅片表面的切割纹被完全去除;小腐蚀坑密布硅片表面,尺寸小于 1 μm,而传统湿法酸制绒所形成的腐蚀坑尺寸大于 10 μm.气相刻蚀后的金刚石线锯切割多晶硅片表面的微观粗糙度比传统酸混液制绒后的金刚石线锯切割多晶硅片表面的微观粗糙度高 3 倍多.气相制绒效果明显,并仅有 12.11%的低反射率.

关键词:多晶硅;气相刻蚀;金刚石线锯切割;切割纹;反射率;制绒
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Texture for Diamond Wire Sawn Multicrystalline Silicon Wafers by a Vapor Etching Method

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Abstract: Vapor Etching (VE) was used to etch diamond wire sawn mc-silicon wafers. The vapor was generated from heating the acid mixture solution of $HF\text{-}HNO_3$ in the volume ratio of 1:3 (the total volume of the solution is 400 mL) at 90 ℃. The results showed that etching for 15 minutes, saw marks can be removed and lots of small corrosion pits which appeared in big corrosion pits were densely covered with silicon wafer surface, the average size of the corrosion pits was about 1 μm, while that by wet acid etch was over 10 μm. The wafer surface roughness with VE method is actually 3 times higher than that with traditional wet acid etching method. The effect of VE is obvious and the reflectivity is low to 12.11%.

Key words: Multi-crystalline silicon; Vapor etching; Diamond wire saw; Saw marks; Reflectivity; Texturization
OCIS Codes: 160.0160; 160, 2100; 640.6040

0 Introduction

Diamond Wire Saws (DWS) are widely used in cutting hard brittle materials. The DWS technology has been gradually replacing the conventional Slurry Wire Saw (SWS) in production silicon wafers for solar cells. Diamond wire saw technology has the advantages over the SWS technology including higher productivity, higher precision enabling production of thinner wafers, less pollution and less surface mechanical damages[1-6]. However, the biggest drawback of DWS technology is that there are lots of parallel saw marks on the wafer surface. The DWS silicon wafers thus display a shiny surface, reflectivity of which is over 34 % and found to be 7% ~ 10% relatively higher than that of the conventional SWS wafers.

Surface texture is an important process for fabrication of mc-silicon solar cell. A textured surface

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minimizes the reflected light of the front surface and then increases the optical path length of the incident light of shorter wavelengths by an oblique trajectory within the solar cell and the absorption of light closer to the junction[7-9]. The DWS mono-crystalline silicon wafer can use the conventional alkaline etching to achieve the same low reflectivity as SWS wafers. However, conventional wet acid textured for SWS mc-silicon wafers does not work with DWS mc-silicon wafers[10], and further attempts with a wide range of HF-HNO_3-H_2O ratio in the acid recipes have all failed to reduce the reflectivity to a satisfactorily low level[11-12], and the saw marks generated by the DWS process cannot be removed. It was more difficult to etch DWS mc-silicon wafers, because a thin amorphous silicon layer exists on surfaces of the smooth grooves compared with SWS wafers [13], which can restrain the rate of wet acid textured. As-cut silicon wafer structures have a significant impact on the evolution of the wafer surface morphology during the wet acid textured[12]. The initial damage places decide the sites where the etching preferentially occurs and affects the morphology of the etched surface. The damage areas of DWS silicon wafers displays along the saw marks into a banding distribution, having the anisotropic features and mainly distribute in the valley of the saw marks. While the thin amorphous silicon layer exits in the raised portion of the saw marks[6]. All this result in obtaining bad texture with high reflectivity and with saw marks by using wet acid textured[14].

Sand blasting was proposed to decrease the reflectivity to meet the need of photovoltaic industry and remove the saw marks of DWS mc-silicon wafers, as a pre-treatment before wet acid textured[15]. This treatment can decrease the reflectivity and remove the saw marks. However, its high cost and low productivity hindered its further development into a practical solution for industry.

In our research, vapor etching method has been investigated. Encouragingly, saw mark-free, well textured surfaces of DWS mc-silicon wafers have been obtained. This paper reports the method, characterization and discussion on the mechanisms involved in the VE textured of DWS mc-silicon wafers.

1 Experimental methods

DWS p-type mc-silicon wafers of 190～210 μm thick, and 156 × 156 mm^2 in size, provided by a diamond-wire developer, Bekaert, were sliced into samples of 33×26 mm^2 and used in the present study.

Fig. 1 illustrates the simple and low cost setup of the VE textured experiments. This set-up is composed of a Teflon container, loaded by HF and HNO_3. At the bottom of the container, electric stove wire with temperature control is equipped. The DWS mc-silicon wafer was positioned on the Teflon holder over the acid mixture solution. The acid mixture solution was heated to produce vapor to etch the wafers.

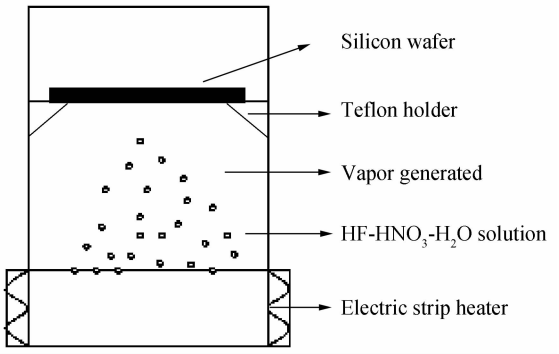


Fig. 1 Schematic representation of the vapor texturing setup

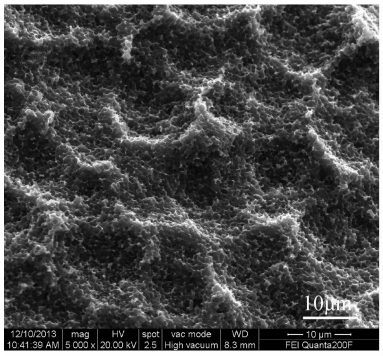
For comparison, the DWS mc-silicon wafers were etched in acid mixture solution of HF-HNO_3-H_2O, in the volume ratio of 1:3.75:2, for 2 min at 8 ℃. The average thickness of one side surface layer removed by the etching was at approximately 5 μm. The wet acid textured solution was prepared from HF (40%, w/w), HNO_3 (65%, w/w) and deionized water (DI).

The surface microstructure of silicon wafer was analyzed by Scanning Electron Microscope (SEM). The surface roughness was measured by laser confocal microscopy (OLS4000, Japan). The reflectivity was measured by the Ocean Optic USB-4000 fiber spectrometer with integrating sphere.

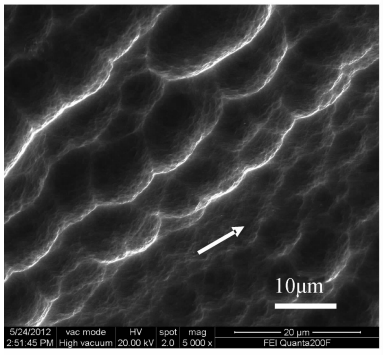
2 Results and discussion

2.1 Morphology, surface roughness and reflectivity of the VE textured mc-silicon wafers

As can be seen from Fig. 2(a), lots of small pits appear in big corrosion pits (as seen as the arrow pointed in Fig. 2(a) and the saw marks were removed completely. In other words, the corrosion small pits formed by VE textured were equal to a second etching on the basis of the corrosion pits formed in wet acid etch solution. From Fig. 2(b), it is found that the saw marks still exist on the wafer surface, and the surface morphology was similar to its before etching, which were found in our previous research[14]. There are still parallel bands of less pitted areas (as seen as the arrow pointed in Fig. 2(a). The average size of the corrosion pits formed by VE textured method was about 1 μm (in Fig. 2(a), while another was over 10 μm (in Fig. 2(b)). The surface texture of the VE textured was better than that of wet acid etch.



(a) Etched with VE textured method



(b) Etched with wet acid textured method

Fig. 2 SEM micrographs of wafers

Table 1 presents the surface roughness of the silicon wafers with two different kinds of etching methods measured with the laser confocal microscope. For each measurement the sampling length is limited to a short length of 120 μm, so that contributions from height variation of large range of surface areas are minimized. The Ra is arithmetic average roughness, which is the average absolute height difference of each point in the sampled length from the average height of the sampled line. The Rz is the largest peak-to-valley distance in the sampling line. As indicated by the data, silicon wafers with VE textured method is actually 3 times higher in both types of roughness than the silicon wafers surface with traditional wet acid textured method.

Table 1 Roughness in 120 μm unit of DWS silicon wafers by wet acidtextured and VE textured

Sampling unit	Wet acid textured		VE textured	
	Ra/μm	Rz/μm	Ra/μm	Rz/μm
1	0.31	1.81	1.23	6.2
2	0.36	1.45	1.56	7.58
3	0.29	1.63	1.48	7.31
4	0.37	1.84	1.49	8.38
5	0.28	1.67	1.39	7.57
Average	0.32	1.68	1.43	7.41

In Fig. 3, as can be seen, in the visible wavelength, the reflectivity of DWS wafers etched by vapor was apparently lower than that of the other two. This is due to the small and deep corrosion pits formed on the wafer surface by VE textured. The results of the reflectivity are consistent well with the micro-topography shown in Fig. 2 and surface roughness appeared in Table 1.

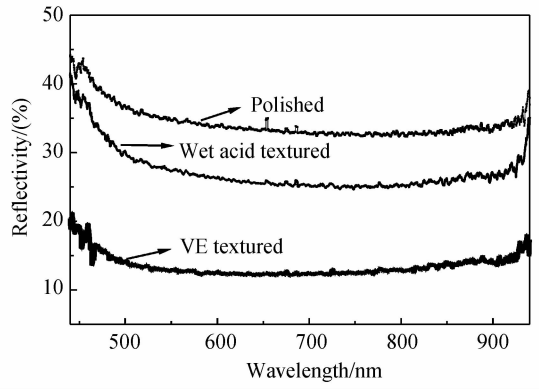


Fig. 3 Reflectivity of polished silicon wafer, silicon wafer with VE textured, and silicon wafer with wet acid textured

2.2 Kinetics and evolution of the VE texturing processes

The weight loss of DWS wafers versus VE textured time is plotted in Fig. 4. As we can see, the weight loss shows a linear dependence with the etching time. From the slope of the weight loss curve, the average rate of the VE textured is found to be ~2 μm · min^{-1}.

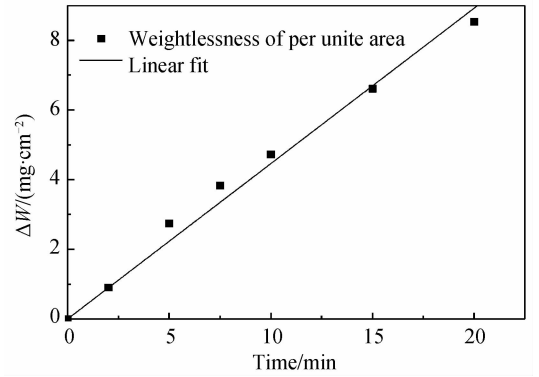


Fig. 4 Weight loss of dissolved silicon wafers versus the etching time

Fig. 5 shows the evolution of DWS mc-silicon wafers surface micro-topography with different etching time in vapor, and the micrographs are taken at the same magnifications. As we can see, the DWS silicon wafer etched in the vapor has shown strong selectivity, the raised portion of the saw marks was preferential etched to become flat and appeared big corrosion pits-named as first corrosion pits (Fig. 5(b)). When the etching time was 5 min, the saw marks was not obvious (Fig. 5(c)). When the etching time was 10 min, lots of small corrosion pits (named as secondary corrosion pits) appeared in the first corrosion pits and the saw marks disappeared completely (Fig. 5(d)). With the extension of etching time to 15 min, the number of corrosion pits increased and the wall of first large corrosion pits were etched by VE textured into a large number of secondary smaller pits compared

with those in Fig. 5(d). However, when the etching time increased to 20 min, the pits merged the nearest pits into relatively larger pits. It is concluded that the etching time of 15 min can acquire proper texture with the saw marks being removed completely and with the smallest corrosion pits.

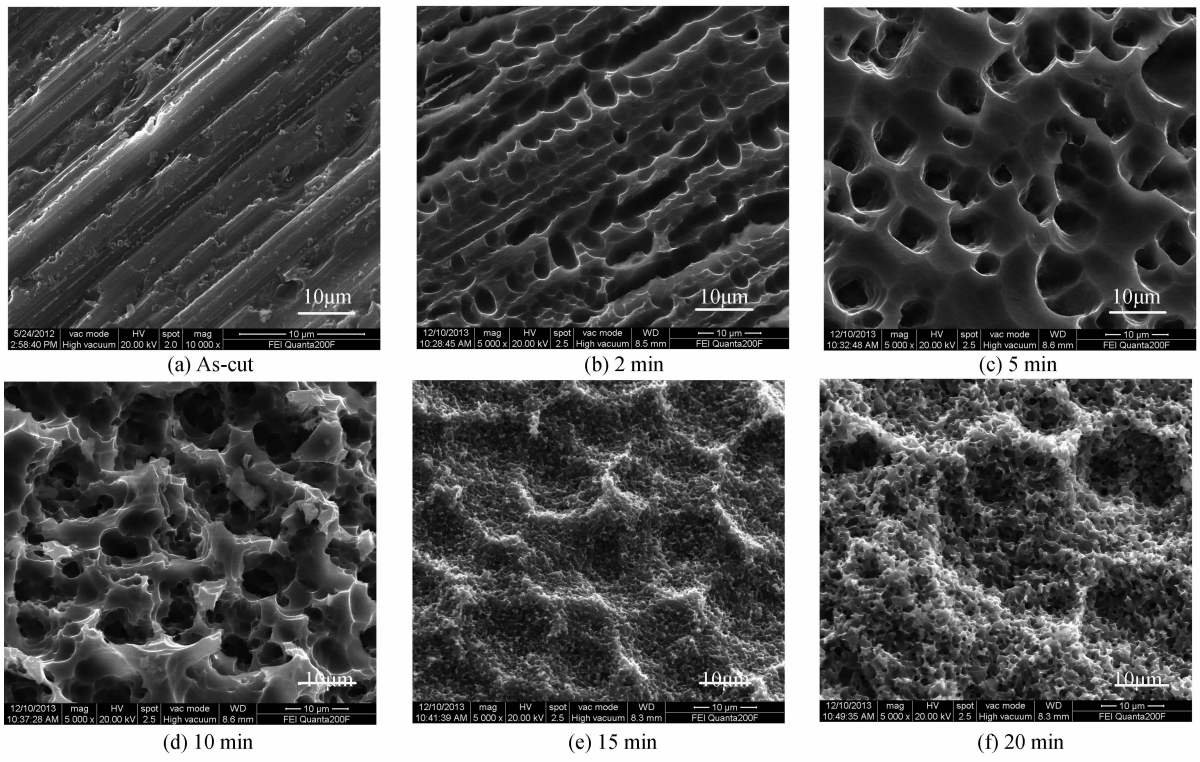


Fig. 5 Evolution of micrographs of DWS mc-silicon wafers etched in vapor (SEM)

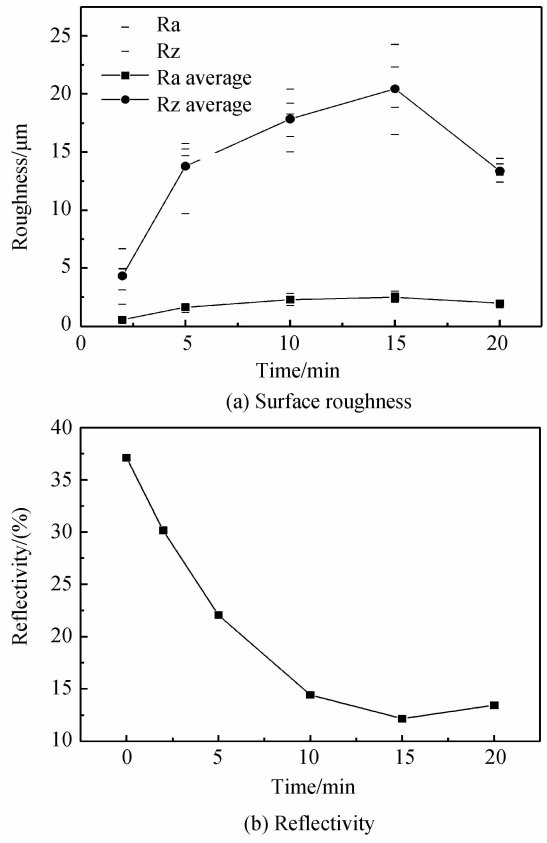


Fig. 6 The surface roughness and reflectivity curves of silicon wafer with different etching time

Fig. 6 presents the surface roughness and reflectivity of silicon wafers with different etching time. As can be seen from Fig. 6(a), the two kinds of roughness present the same change tendency. They increase till the biggest roughness obtained at 15 min and then decrease with the etching time. The variation of surface roughness is fit well with the microstructure evolution in Fig. 5. From Fig. 6(b), it can be seen that the reflectivity (at 600 nm wavelength) reduces first and then increases with the etching time. The lowest reflectivity obtained at etching time of 15 min is just 12.11%. It can be concluded that the biggest surface roughness contributes to the lowest reflectivity. This is due to big surface roughness helpful to increase the path length of light through silicon wafers and absorption of light.

2.3 Discussion

In order to obtain homogeneous texture, we must control the etch kinetics, therefore, all the determined experimental parameters: the volume ratio of HNO_3/HF, the temperature of the acid mixture solution and the exposure time of the silicon wafer to the vapor. In fact, to gain homogeneous texture, these three parameters should vary in a limited range of values. The three appropriate parameters should be found to obtain good texture without saw marks and with low reflectivity.

It is obvious that the acid vapor become richer in HNO_3 as the volume ratio of HNO_3/HF increases. The same effect may be produced by increasing the temperature of the solution. Also, the temperature of the container needs to be controlled to ensure a homogeneous acid vapor flux. The fact is very important regarding the etch kinetics. At room temperature, the etch is low to difficult to detect, the exposure time to increase up to one hour without observing any difference on the silicon surface by high-resolution SEM. For a temperature of 60 ℃, homogeneous texture can be gain with exposure almost 40 min. Beyond 40 min, parts of original small and dense corrosion pits become bigger and a rapid destruction of the surface texture. For the temperatures near 90℃, exposure time should be limited to 15 min, otherwise one favor deep condensation of the acid drops and a rapid destruction of the texture surface. Therefore, the variation of the acid solution temperature should change the vapor density, and hence, may play an important role regarding the etching rate. Furthermore, in order to resolve the problem of inhomogeneous and edge effects, one may enlarge the container and reduce the area of the silicon wafer.

At a given temperature, the volume of the free acid container part is saturated with vapors. As the temperature increases, the amount of the acid vapor may exceed the limit corresponding to saturation, and thus it forms a fog leading to the appearance of small drops on the container walls and particularly on the silicon wafer. The size of the droplets depends on the roughness of the silicon wafer surface and on the saturation degree of the vapors. Refer to our previous study[14], the average roughness of saw marks is 1 μm. This explains the results that the average size of the corrosion pits formed by VE textured method is about 1 μm. Where droplets sticking depends on where is easy to come into contact with. In the case, the vapor may condensate on the peak of the saw marks. That is to say, the raised portion of the saw marks was preferential etched. It is considered that the state of HF, HNO_3 and H_2O in the process of reaction influences the preferred position of etching, in a word, first contact first etch, so raised portion of the saw marks was first smooth and finally disappeared. For the conventional wet acid textured, DWS silicon wafer was surrounded by acid mixture solution, and any location of the silicon wafer had equal opportunity to contact the acid mixture solution. The valley of saw marks with strong mechanical damages is more active and etched preferentially, so the valley was deepen and saw marks cannot be removed. For the VE textured method, the raised portion on the silicon wafer surface was relatively easier wet and etched than the valley of saw marks, so the saw marks can be removed completely. The VE textured reaction equations are as follows:

$$3Si + 4HNO_3 \rightarrow 3SiO_2 + 4NO\uparrow + 2H_2O \quad (1)$$

$$SiO_2 + 6HF \rightarrow 3H_2SiF_6 + 2H_2O \quad (2)$$

$$H_2SiF_6 \rightarrow SiF_4\uparrow + 2HF \quad (3)$$

Silicon reacts with HNO_3, leading to the formation of SiO_2 (reaction1). SiO_2 dissolved easily in HF solution (reaction2) to generate H_2SiF_6. H_2SiF_6 easily decomposes into SiF_4 and HF under the no water condition (reaction3). As can been seen, the products of NO and SiF_4 gases leave and no pollutants are on the surface of wafer.

3 Conclusions

We demonstrated the formation of small and deep corrosive pits with the average size of 1 μm which is much smaller than we gain by wet acid textured, by using a simple and low cost VE textured technique. The VE textured has been developed successfully as a method to texture DWS mc-silicon wafers in a homogeneous way, independently of the grain orientation and saw marks on the surface, that is, all saw marks can be removed completely. We detailed the principle of VE textured and the effect of preparation parameters. We pointed out some differences between VE textured method and the classical wet acid textured method. The wafer surface roughness with VE textured method is actually 3 times higher in both types of roughness than that with conventional wet acid textured method. The reflectivity of DWS mc-silicon wafer by VE textured is low to 12.11%, much lower than its gained by wet acid textured.

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References

[1] BIDIVILLE A, HEIBER J, WASMER K, *et al*. Diamond wire wafering: wafer morphology in comparison to slurry sawn wafers [C]. 25th Eutopean Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photoltaic energy conversion, Semptember 2010, 6-10, Valencia, Spain: 1673-1676.

[2] BIFIBILLR A, WASMER K, KRAFT R, *et al*. Diamond wire-sawn silicon wafers - from the lab to the cell production [C]. Proceedings of the 24th European Photovolatic Solar Energy Conference and Exhibition, 2009 (PV-LAB-CONF-2010-026): 1400-1405.

[3] CLARK W I, SHIH A J, HARDIN C W, *et al*. Fixed abrasive diamond wire machining-part I: Process monitoring and wire tension force[J]. *International Journal of Machine Tools and Manufacture*, 2003, **43**(5): 523-32.

[4] KRAY D, SCHUMANN M, EYER A, *et al*. Solar wafer slicing with loose and fixed grains[C]. Proceedings of the Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference on, IEEE , 2006, 1: 948-951.

[5] WATANABE N, KONDO Y, IDE D, *et al*. Characterization of polycrystalline silicon wafers for solar cells sliced with novel fixed-abrasive wire[J]. *Progress in Photovoltaics: Research and Applications*, 2010, **18**(7): 485-90.

[6] YU X, WANG P, LI X, *et al*. Thin Czochralski silicon solar cells based on diamond wire sawing technology[J]. *Solar Energy Materials and Solar Cells*, 2012, **98**: 337-342.

[7] IENCINELLA D, CENTURIONI E, RIZZOLI R, *et al*. An optimized texturing process for silicon solar cell substrates using TMAH[J]. *Solar Energy Materials and Solar Cells*, 2005, **87**(1-4): 725-32.

[8] STOCKS M J, CARR A J, BLAKERS A W. Texturing of polycrystalline silicon[J]. *Solar Energy Materials and Solar Cells*, 1996, **40**(1): 33-42.

[9] VAZSONYI E, DE CLERCQ K, EINHAUS R, *et al*. Improved anisotropic etching process for industrial texturing of silicon solar cells[J]. *Solar Energy Materials and Solar Cells*, 1999, **57**(2): 179-188.

[10] HOLT A, THOGERSEN A, ROHR C, *et al*. Surface structure of mono-crystalline silicon wafers produced by diamond wire sawing and by standard slurry sawing before and after etching in alkaline solutions[C]. Photovoltaic Specialists Conference, 2010 35th IEEE, 2010, 003501-4.

[11] CHOU Y C, KUO Y C, YANG S W, *et al*. Acid treated surface morphology of fixed abrasive sawn wafers[C]. Proceedings of the Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE. IEEE, 2011: 002136-002138.

[12] MEINEL B, KOSCHWITZ T, ACKER J. Textural development of SiC and diamond wire sawed sc-silicon wafer [J]. *Energy Procedia*, 2012, **27**: 330-336.

[13] CAI E, TANG B, FAHRNER W, *et al*. Characterization of the surfaces generated by diamond cutting of crystalline silicon[C]. 26th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany, 2011, 1884-6.

[14] LIU Xiao-mei, LI Miao , CHEN Wen-hao, *et al*. The surface characteristics of diamond wire sawn multicrystalline silicon wafers and their acidic texturization [J]. *Acta Photonica Sinica*, 2014, **43**(8): 0816001-6

[15] XIE C, EICHMAN D J. Pretreatment process for a surface texturing process[P]. Google Patents, 2001.