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应用于塑料光纤通信接收芯片的集成光电探测器

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摘 要:基于 0.5 μm 标准 Biplor、互补金属氧化物半导体和双扩散金属氧化物工艺设计了两种不同结构不同尺寸的光电探测器,包括传统的 P^+/N-EPI/BN^+ 结构光电探测器和多叉指 P^+/N-EPI/BN^+ 结构的光电探测器.通过仿真优化设计了光电探测器的结构参量和性能,测试结果表明:多叉指状 P^+/N-EPI/BN^+ 光电探测器能够改善 650 nm 的响应度以及降低结电容.选择该结构大面积 P^+/N-EPI/BN^+ 光电探测器用于和跨阻放大器以及后端放大器的单片集成,采用 0.5 μm 标准 Biplor、互补金属氧化物半导体和双扩散金属氧化物工艺实现了一个用于 650 nm 塑料光纤通信的单片集成光接收芯片.该光接收芯片的测试结果表明:对 650 nm 的入射光,在 160 Mb/s 速率的伪随机二进制序列以及小于 10^{-9} 的误码率条件下,光接收芯片的灵敏度为 −15 dBm,并能得到清晰的眼图.因此,本文设计的光电探测器可以很好地应用于宽带接入网中的高速塑料光纤通信系统的光接收芯片中.

关键词:塑料光纤通信;光接收芯片;单片光电集成;光电探测器;硅基;多叉指 P^+/N-EPI/BN^+
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Different Structure Integrated Photodetectors Applied in POF Receivers

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Abstract: Two types of photodetectors including conventional P^+/N-EPI/BN^+ photodetector and multi-finger P^+/N-EPI/BN^+ photodetector were implemented in a standard 0.5 μm Biplor, CMOS and DMOS process with different sizes. The performance and parameter of photodetectors were simulated and optimized. Results of the characteristics of photodetectors simulations and tests were presented, which showed that the multi-finger structure P^+/N-EPI/BN^+ photodetector can improve the responsibility at 650 nm and decrease the junction capacitance. The large-area multi-finger structure P^+/N-EPI/BN^+ photodetector was chosen for the monolithic integration with a trans-impedance amplifier and a preamplifier. A proposed monolithic optoelectronic integrated receiver was fabricated in 0.5 μm Biplor, CMOS and DMOS technology for 650 nm plastic optical fiber communication. The measurements of the proposed receiver were done. The receiver achieved a sensitivity of -15 dBm with the bit-error-rate of 10^{-9} at 160 Mb/s pseudo random binary sequence signal for 650 nm input light. A clear eye diagram was demonstrated for 160 Mb/s pseudo random binary sequence signal. These indicate that the proposed photodetector can be employed in the receiver chip of high-speed plastic-optical-fiber-based fast ethernet

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system for broadband access network application.

Key words: Plastic optical fibers communication; Optical receiver; Monolithic optoelectronics integrated circuit; Photodetector; Silicon-based; Multi-finger P^+/N-EPI/BN^+

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0 Introduction

Large core step-index poly-methyl-meta-acrylate Plastic Optical Fibers (POFs) are well known for their excellentmechanical characteristics compared to Glass Optical Fibers (GOFs), such as stress resilience, low bending radius, low bending losses and ease of connection. In short distance communication systems, POFs are today largely commercially used in Media Oriented System Transport (MOST), industrial control and so on[1-3]. Recently, with the recent explosive demands for broadband access home communication systems, the standard 1mm core Step-index Plastic Optical Fibers (SI-POFs) are gradually applied to the low-cost home networking[4-8]. As the need for higher data rate home networking grows, more efforts such as monolithic integrated optical receiver and relevant key technology are being put into the development of high-speed POF-based fast ethernet system[9].

The physical property of silicon allows the material to be sensitive for wavelengths between 400 nm and 1 100 nm. Since silicon material has a certain response to the wavelength of 650 nm, optical receiver for POF system is feasible to realize the monolithic integration of Photo-Detector (PD) and preamplifier in the standard Si-based process[10-11] (BCD, CMOS, BiCMOS, etc). Furthermore, for the large core diameter close to 1 mm of a typical POF cable, a large-area PDintegrated in IC standard technology is desired for low-cost high-efficiency light coupling, which brings high junction capacitance and large noise [12-13]. The Ref.[14] analyzes the frequency characteristic of the PD for 780 nm and 650 nm. And the cut-off frequency just has 14.4 MHz and 43 MHz, respectively. For improving the characteristic and optimizing the structure of PD, two different structures of PDs consisting of conventional P^+/N-EPI/BN^+ (PIN) PD and multi-finger PIN PD compatible for BCD technology are presentedin this paper. The characteristics of the two types of PDsare also tested and compared. Based on the analysis of PDs proposed in this paper and our former research[15], a preferable PD with large area and novel preamplifier have been applied to implement a monolithic integrated optical receiver of POF proposed in this paper.

This paper is organized as follows. Two types of PD structures are compared in section II. The simulated and tested characteristics are also presented and compared. With the analysis of test results, a preferable PD structure will be applied to the proposed monolithic integrated optical receiver for POF. The architecture and sub-circuit of the proposed optical receiver will be described in section III. Section III will also present simulated results and measured results of receiver chip. Section IV gives a conclusion.

1 Different structure PDs

1.1 Structures of PDs

Two types of PDs including PIN structure PD and multi-finger PIN structure PD in 0.5 μm BCD (Biplor, CMOS and DMOS) process are studied in here. They are labeled as PD_1 and PD_2, and the cross-section of the two PDs are depicted in Fig. 1(a)～(b), respectively. Here, the insulated medium layers (SiO_2 and Si_3N_4) in BCD technology are not shown. In PD_1, the N-EPI layer with resistivity of 3.5Ω·cm forms the I-finger layer, strictly speaking, where I-layer is not a real intrinsic layer but a low doped N epitaxial layer. The N^+ region on the N-well connect with BN^+ buried layer acts as cathode. The P^+ region on the N epitaxial layer acts as anode. The N-well and N epitaxial layer are alternated in structure of PD_2. In PD_2, the P^+ fingers on the N epitaxial layer are combined to a common anode, and N^+ fingers on the N-Well connecting with BN^+ buried layer act as cathode. The multi-finger PIN PDs with different photosensitive area have different number and width of finger.

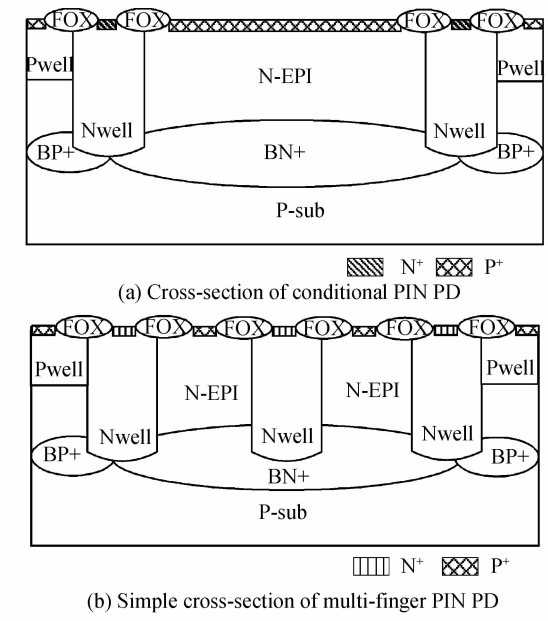

Fig. 1 Cross-section of two types of PDs

1.2 Results and discussion

The characteristics of different PDs, such as responsivity, bandwidth and capacitance, were tested. The same solo PDs as the integrated ones were implemented and packaged with TO for measurements conveniently. The forward threshold voltages of PD_1 and PD_2 are almost the same of 0.7 V for silicon material. But their breakdown voltages are 20 V and 25 V, respectively. The breakdown voltages are dependent on the depletion region thickness of PN junction in different structure PDs. The dark currents of PDs were tested by Agilent Digit Multimeter with the maximum one of 10.9 pA.

The responsivity characteristic of PD is vital for optoelectronic integrated receiver design. The optoelectronic performance of PD can be simulated by constructing PD device in software following the IC process flow. It can be seen from simulated and tested results that the performance of PD can be forecasted. The optimization of PD structure and co-design of receiver can be carried out very well. The simulated and measured spectral response curves of PD_1 and PD_2 at a reverse voltage of 2.5 V are shown in Fig. 2 and Fig. 3, respectively. The light is detected in the range of 400～1 200 nm. The simulated and tested results indicate that the peak of relative spectral response curve of PD_2 is similar to PD_1. Just the absolute responsivities have a little difference. There is a certain oscillation in the tested curve, which is due to the influence of insulated medium and passivation layers on the reflectance coefficient unconsidered during simulation. The PD_2 gets better responsivity characteristic in shorter wavelength. For example, in 650 nm incident light, the tested absolute responsibilities of PD_1 and PD_2 are 0.251 A/W and 0.260 A/W, respectively.

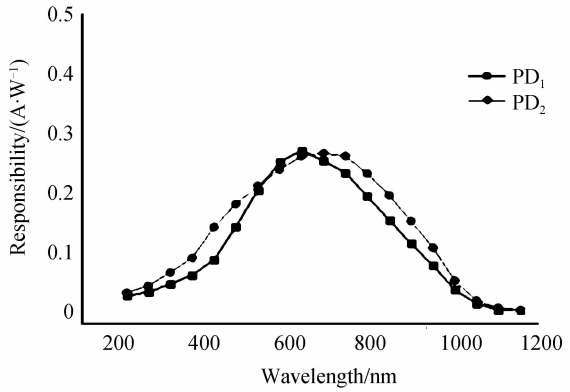

Fig. 2 Simulated optical spectral response curves of two PDs

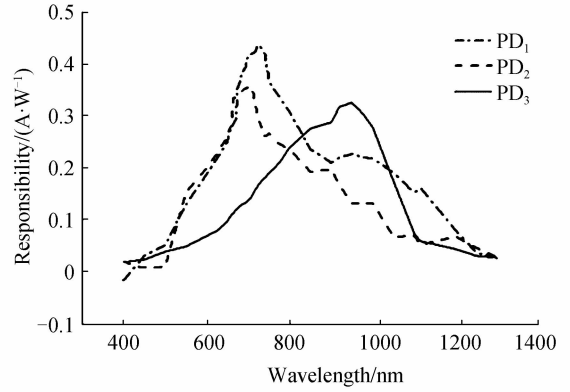

Fig. 3 Tested optical spectral response curves of three PDs

The peak of the optical spectral response curves of PD_1 and PD_2 have shifted to shorter wavelength compared with the photodetector labeled as PD_3 that is implemented in CMOS technology and presented in our former research result[16]. The optical spectral curve of PD_3 shown in Ref. [16] is also put into the Fig. 3 to conveniently compare with the other two. It shows that the peak in optical spectral response curve of PD_3 is about at 950 nm, while the peaks of PD_1 and PD_2 described in this paper are at 700 nm. The reason is that the PDs are implemented in different IC processes. The junction depth of photodetector in CMOS process is shallower than that in BCD process. In the PD_3, most of the energy is absorbed in deeper layers so that the absorption at about 950 nm which is more than 650 nm. With the reason that the epitaxial layer and BN^+ buried layer in BCD process form the I-layer in PD_1 and PD_2, the thicknesses of depletion layers are increased. The absorption in shorter wavelength range of 600～700 nm becomes more intense and more photo-generated current is generated consequently. At the wavelength of 650 nm, the responsivity of PD_3 is 0.100 A/W, while the responsivities of PD_1 and PD_2 are 0.251 A/W and 0.260 A/W, respectively. Thus, the PD structures presented in this paper are more suitable for detecting the wavelength range of 600～700 nm.

Table. 1 shows the tested capacitances of the two kinds of PDs with different areas under the reverse bias of 2.5 V. It can be seen from the results that the capacitance of multi-finger PIN-PD is smaller than that of PIN-PD with the same size. Furthermore, the junction capacitance increases for increasing the area of PD with the same structure. The junction capacitance C_{pd} of photodetector can be described as a plate capacitor, when the influence of the lateral capacitance is neglected. It is expressed as Eq. (1).

$$C_{pd}=\frac{\varepsilon_s A_0}{x_w}=A_0\sqrt{\frac{\varepsilon_s q N_A N_D}{2(N_A+N_D)(V_{bi}-2KT/q-V)}} \tag{1}$$

where ε_s is dielectric coefficient of silicon. A_0 is the optical window area. The depletion region depth x_w determines C_{pd} strongly. N_D and N_A represent donor and acceptor concentration, respectively. V_{bi} is built-in potential. V is bias voltage of capacitor considering the influence of series resistance.

Table 1 Tested capacitances of different structures with different area

Area/μm^2	50×50	200×200	300×300	500×500
PIN-PD/pF	0.35	8.20	12.7	--
Multi-finger PIN-PD/pF	0.15	4.39	--	15.21

The frequency characteristic of photodetector including physical and electrical bandwidth is discussed. The total bandwidth is by approximation the lower of these two. But due to the limit of measure instrument, the bandwidth can't be gotten accurately for the very small photocurrent of discrete photodetector in dynamic-state measurement. The frequency characteristic will be tested in the optical receiver chip with PD and Trans-Impedance Amplifier (TIA) subsequently.

Therefore, the multi-finger PIN structure contributes to lower the photodiode capacitance compared with the same size PIN PD proved by the measurement results. This structure is more appropriate in 600 ~ 700 nm wavelength detection. Because of its low junction capacitance and high responsivity at 650 nm, the multi-finger PIN PD with the responsivity of 0.260 A/W and the capacitance of 4.39 pF is applied to the proposed monolithic integrated optical receiver in next research.

2 The proposed optical receiver

2.1 Design of optical receiver

The optical receiver consisting of a multi-finger structure PD, a TIA, and a post amplifier, is proposed. The used multi-finger PD has 10 fingers of P^+ on the N epitaxial layer combined to a common anode and 11 fingers of N^+ on the N-Well connected with BN^+ buried layer acting as cathode in total. These P^+ fingers have a width of 10.0 μm and are separated by N^+ fingers with a width of 6.3 μm between them. The photo-sensitive surface with the size of 200×200 μm^2 is designed for POF application. The anode and cathode are connected to ground and input of TIA, respectively.

TIA uses the common-source amplifier with feedback and Automatic Gain Control (AGC) as the input stage, shown in Fig. 4. This amplifier has the advantages of low noise, high sensitivity and trans-impedance gain. AGC is also a feedback network. The feedback resistor R_f is parallel with a transistor M_f. The voltage V_{con} is achieved by comparing the output of input stage V_{o1} and reference voltage in a voltage comparator is used to control the switching of M_f. The value of reference voltage is determined by the maximal photocurrent of PD and the gain of input stage. The V_{con} is varied with the V_{o1}. Thus, the feedback resistance can be changed with the variation of V_{con}. When the photocurrent is little, V_{o1} is smaller than reference voltage, AGC do not work and the M_f is closed consequently. While the magnitude of input photocurrent is varied largely, the V_{o1} is larger than reference voltage, AGC gets to work and therefore the M_f opens. The trans-impedance gain is controlled and the swing of output voltage is stable consequently.

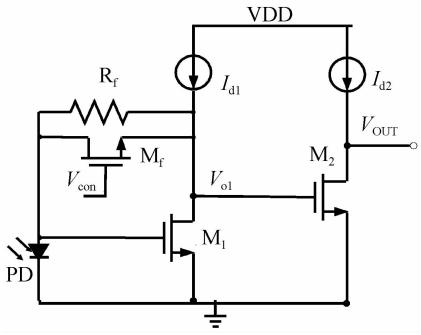

Fig. 4 Schematic of trans-impedance amplifier with feedback and AGC

The post amplifier includes the three cascaded modified Cherry-Hooper amplifiers and an out buffer. The modified Cherry-Hooper amplifier was first introduced in CMOS by Ref. [17]. It can increase the gain without a corresponding decrease in bandwidth. Compared to a traditional Cherry-Hooper stage, the load resistor is split up in two resistors R_1 and R_2, and the transistors M_5-M_6 form the source-follower feedback, shown in Fig. 5. The ratio of R_2 and R_1 is proportional to the gain. To increase the gain, this ratio must be large. The out buffer employs the differential common-source amplifier with the load resistor of 50 Ω to match the transmission line impedance.

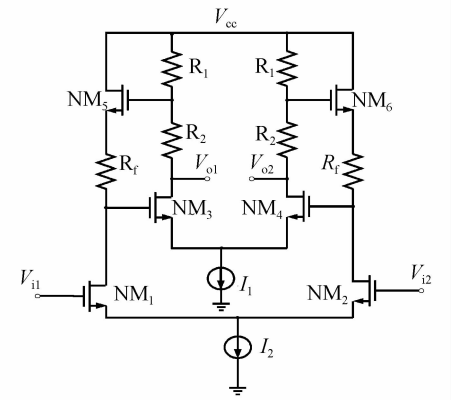

Fig. 5 Schematic of modified Cherry-Hooper amplifier

2.2 Simulated results

The AC characteristic curves of TIA and whole receiver shown in Fig. 6 are simulated in Spectre environment. The input Pseudo Random Binary Sequence (PRBS) signal has pulse period of 2 ns and

magnitude of 5 μA. The DC current of 10 μA and the junction capacitance of 5 pF are applied to the simulation. It can be seen from the AC curves that the −3 dB bandwidth of TIA and whole receiver is 192.7 MHz and 193.9 MHz, respectively, the gain of whole receiver is 86.25 dBΩ.

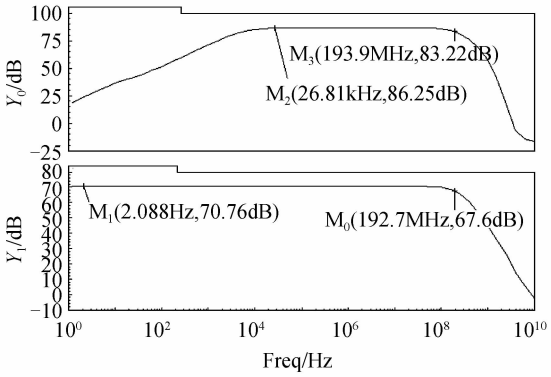

Fig. 6 Simulated AC characteristic curves

2.3 Tested results and discussion

The optical receiver were implemented in low-cost 0.5 μm BCD technology for POF communication. Fig. 7 shows the layout of the monolithic integrated optical receiver chip with a 200 × 200 μm^2 integrated multi-finger PIN PD. The whole receiver chip occupies the area of 1.03 mm^2.

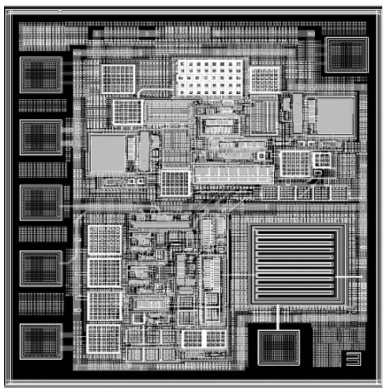

Fig. 7 Layout of optical receiver

The output DC operating point of the receiver chip with and without illumination is 3.92 V and 4.53 V, respectively. The gain of the tested chip is 18.5 kΩ calculated by the difference of DC voltage of the whole chip and the responsivity at 650 nm. The value is very close to the simulated gain of 86.25 dBΩ. The used modulation electrical signal of modulated light source is 2^7-1 NRZ PRBS signal. The light source is Resonant Cavity Light Emitting Diode (RCLED) with the wavelength of 650 nm. The test of eyediagram of the optical receiver chip was carried out. The tested results show that the receiver can operate at the speed of 160 Mb/s with the eyediagram as shown in Fig. 8, respectively. The sensitivity is -15 dBm under the Bit-Error-Rate (BER) of 10^{-9} at 160 Mb/s. Furthermore, this result also can be proof of good frequency characteristic of the proposed PD. In general, the receiver can operate in the100 Mb/s POF-based Fast Ethernet systems.

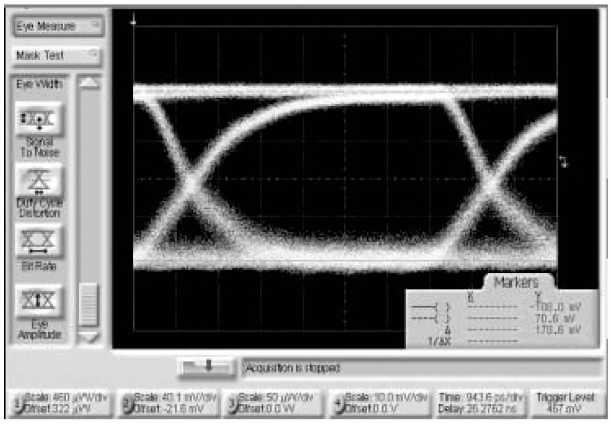

Fig. 8 Tested eye diagrams of the receiver with 160 Mb/s 2^7-1 PRBS

3 Conclusions

The simulated and tested characteristics of two kinds of PDs including conventional PIN PD and multi-finger PIN PD were achieved. Based on the analysis of the characteristics of PDs, the low-cost monolithic integrated receiver with a multi-finger PIN PD, a TIA, an AGC and a post amplifier for 650nm POF communication was fabricated in 0.5 μm BCD process. Measured results show that the responsivity and capacitance of the multi-finger PIN PD are 0.260 A/W at 650 nm and 4.39 pF under the reverse bias of 2.5 V, respectively. At 160 Mb/s and BER of 10^{-9}, the sensitivity of −15 dBm and a clear eye diagram of the proposed receiver were demonstrated. These indicate that the receiver chip can be employed in 100 Mb/s POF-based Fast Ethernet system for broadband access network application. The potentiality of upgrading to a higher transmission data rate (Gb/s) of optoelectronic integrated receiver makes POF communication systems for a more extensive market.

References

[1] POFERL S, BECHT M, DE PAUW P. 150Mbit/s MOST, the next generation automotive infotainment system[C]. 12th International Conference onTransparent Optical Networks, 2010, 1-2.

[2] RICHARDS D, ANTONIADES N, TRUONG T K. Performance modeling and analytical verification of POF transmissive star couplers for avionics system applications[C]. Avionics, Fiber- Optics and Photonics Technology Conference, IEEE, 2011, 77-78.

[3] OKONKWO C M, TANGDIONGGA E, YANG H, et al. Recent results from the EU POF-PLUS project: multi-gigabit transmission over 1 mm core diameter plastic optical fibers[J]. *Journal of Lightwave Technology*, 2011, **29**(2): 186-193.

[4] NESPOLA A, ABRATE S, GAUDINO R, *et al*. High-speed communications over polymer optical fibers for in-building

cabling and home networking[J]. *Journal of Photonics*, 2010, **2**(3): 347-358.

[5] AZNAR F, SANCHEZ-AZQUETA C, CELMA S, *et al*. Gigabit receiver over 1 mm SI-POF for home area networks [J]. *Journal of Lightwave Technology*, 2012, **30**(16): 2668-2674.

[6] NESPOLA A, STRAULLU S, SAVIO P, *et al*. A new physical layer capable of record gigabit transmission over 1mm step index polymer optical fiber[J]. *Journal of Lightwave Technology*, 2010, **28**(20): 2944-2950.

[7] DONG Yun-zhi, MARTIN K W. Gigabit communications over plastic optical fiber[J]. *IEEE Solid-State Circuits Magazine*, 2011, **3**(1): 60-69.

[8] WANG Xue-zhong, RUAN Chi, Gao Ying-jun. Investigation in process of low-loss step index polymer optical fiber[J]. *Journal of Acta Photonica Sinica*, 2002, **31**(7): 870-873.

[9] KARPPINEN M, TANSKANEN A, OLLILA J, *et al*. Fiber-optic transceiver for high-speed intra-satellite links [C]. Avionics, Fiber- Optics and Photonics Technology Conference, IEEE, 2012, 34-35.

[10] YAN Huang-ping, CHENG Xiang, HUANG Yuan-qing. Research of silicon-based monolithic 850nm optical receiver [J]. *Journal of Optoelectronics · Laser*, 2012, **23**(4): 676-680.

[11] KOSTOV P, GABERL W, HOFBAUER M, *et al*. PNP PIN bipolar phototransistors for high-speed applications built in a 180 nm CMOS process [J]. *Journal of Solid-State Electronics*, 2012, **74**(SI): 49-57.

[12] KANG YEOB P, WON SEOK O, JONG CHAN C, *et al*. Design of 250-Mb/s low-power fiber optic transmitter and receiver ICs for POF applications [J]. *Journal of Semiconductor Technology and Science*, 2011, **11**(3): 221-228.

[13] KANG YEOB P, WON SEOK O, WOO YOUNG Chttp://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp? punumber=5331933. Design of CMOS led driver and optical receiver for 650nm POF applications[C]. 9th International Symposium onCommunications and Information Technology, 2009, 1375-1380.

[14] BIAN Jian-tao, CHENG Xiang, CHEN Chao. Frequency response research of photodetecotor by laplace transform[J]. *Journal of Acta Photonica Sinica*, 2007, **36**(10): 1804-1807.

[15] LI Ji-fang, YAN Huang-ping, CHENG Xiang, *et al*. Design of a POF receiver with integrated photodiode in 0.5μm BCD process [C]. IEEE International Conference onAnti-Counterfeiting, Security and Identification, 2011, 194-197.

[16] CHENG Xiang, BIAN Jian-tao, CHEN Chao, *et al*. Research of different structure integrated photodetectors in standard CMOS technology[C]. Procceding of SPIE 6838, Optoelectronic Devices and Integration II, 68381O. 2008.

[17] HOLDENRIED D H, LYNCH M W, HASLETT JW. Modified CMOS cherry-hooper amplifiers with source follower feedback in 0.35 μm technology[C]. 29th EuropeanSolid-State Circuits Conference, 2003, 553-556.