第33卷第4期
2004年4月

光子学报
ACTA PHOTONICA SINICA

Vol. 33 No. 4
April 2004

A Novel Optical Buffer Configuration Optimization Scheme for Slotted Optical Packet Switching*

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Abstract The problem of configuring fiber delay lines (FDLs) for recirculation FDL buffer in a slotted and synchronous optical packet switched network is researched in this paper. By studying the distributions of the lost packet in switch with uniform degenerate buffers configuration, it is found that the lost packets arouse by the taking up of small granularity FDL are much more than the lost packets arouse by the taking up of large granularity FDL. So a good scheme to cut down the Packet Lost Ratio is by increasing the proportion of the small granularity FDL at a cost of decreasing the proportion of the large granularity FDL. Simulation results show this scheme is effective.

Keywords Optical packet switching; Optical buffer; Slotted; FDL

CLCN TN929.1 **Document code** A

0 Introduction

The rapid growth on the Internet traffic has created a great demand for large-capacity networks. The appearance of WDM technology, especially DWDM technology, solves the problem to some extent. However with the more increase in link capacity, the network nodes have to process a large amount of incoming data, which is becoming difficult by electrical processing alone. In order to overcome the bottleneck of the electronic processing technology, it is desired that the optical signals should be routed without being converted to electrical signals, that is, they should be routed directly in the optical layer. So optical packet switching is put forward[1-4], the optical packet consists of a header and a payload, in the header there is the route information. In the switching node, only the header is processed. Through reading the header, the packet is delivered to the port. In general, optical packet switched networks can be divided into two categories: time-slotted networks with fixed-size packets[7] and unslotted networks with fixed-size or variable-size packets[8]. In the packet switched network, there are always contentions in the switching node, which cause the packet loss. In traditional electrical packet switched networks, RAM (random-access memory) is used to resolve these contentions, but in the optical packet switched network, optical fiber delay lines (FDL) is one of these components which can be used as the optical buffer now. By using FDL, packets are stored in different lengths of delay lines, through which the departing times of packets are time-shifted. The other two techniques used for resolving packet contention are wavelength-conversion approach and deflection approach. Our works is focusing on the FDL approach. In fact, many works on FDL approach have been done in the past ten years[3-9]. Here, a novel optical buffer configuration optimization method for slotted- synchronous optical packet switched network was put forward.

1 Principles and simulation

In an all-optical packet switched network, contention occurs at a node whenever two or more packets are trying to go to same output port, on the same wavelength. The contention has a great effect on the network performance, such as packet loss ratio. In packet switched network, FDL is used as the time buffering. But the efficiency of the buffering is very lower, because the FDL is only delayed discrete fixed timeslot delay. Just like the electrical buffing, the common configurations of FDL buffering are: output buffering, shared buffering, recirculation buffering, and input buffering. Here, we focus our attention on the buffer configuration optimization of recirculation buffering. In recirculation buffering (Fig. 1), a number

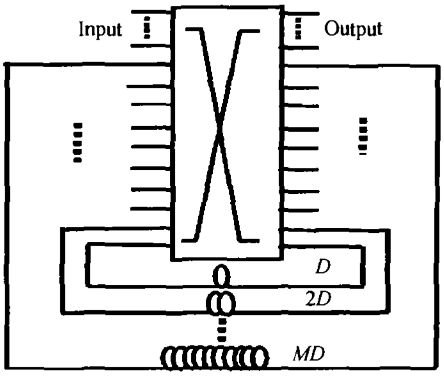

Fig. 1 A general switch model for $N \times N$ with FDL by N consecutive multiples of delay granularity D

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*This work was supported by National Natural Science Foundation of China under the contract 69990540
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Received date: 2003-05-20

of recirculation loops from the output of a space switch feed back into the input. Each loop has a delay of one packet. If more than one packet arrive at the space switch input for a particular packet switch output, all but one is placed into the recirculation loops. Throughout this paper, a packet switch is assumed to have inputs and the same number of outputs.

In recirculation shared buffering, the most common configuration of the FDL is that delays uniformly cover the entire range of buffer depth with increments of one unit: $\{D;2D;\cdots;MD\}$, that means the delay times are M consecutive multiples of delay granularity D. In this paper, we call this configuration as uniform degenerate buffers configuration. Another configuration is that delays are not consecutive multiples of delay granularity D, for an example $\{D; 2D; 4D; \cdots; KD\}$. Someone call it nondegenerate buffers[8].

In a slotted-synchronous optical packet switching node, when there are two packets destining for the same output port synchronously, only one of the packets can pass the given output port, another one has to be discarded. To avoid this, we can use a FDL to postpone the packet for a delay time D. When there are three packets destining for the same output port synchronously, to avoid discarding anyone of the three packets, it needs two FDLs, one FDL is of delay time D and another FDL is of delay time $2D$. When there are k packets destining for the same output port synchronously, it needs $(k-1)$ FDLs, the first FDL is of delay time D, the second one is of delay time $2D$, $\cdots$, the last one is of delay time $(k-1)D$. When there are 4 packets destining for 2 different output port synchronously, among them, one group of two packets destines for the same output port, another group of two packets destines for the other output port, to avoid discarding anyone of the four packets. It needs 2 FDLs, which is of same delay time D. When there are 6 packets destining for 3 different output port synchronously, bi-packets (a group of two packets) destines for different output port respectively, to avoid discarding anyone of the four packets. It needs 3 FDLs, which is of same delay time D. The rests may be deduced by analogy.

Firstly, we study the simplest switching model of N input/output ports without FDL, for clarify reason, we show and compare four kinds of demands for the FDLs: 1-2, 1-3, 2-1, 3-1. Here, 1-2 means one $2D$ FDL, 1-3 means one $3D$ FDL, 2-1 means two $1D$ FDLs, 3-1 means three $1D$ FDLs.

We assume that packets format used here is same as the format in the European ACTS KEOPS Project. The packet is composed of guard time, payload and header, which is shown in Fig. 2. The packets arrival at each port follows the Even distributing process. The routing is also following the Even distributing process. The probability of all kinds of collisions can be calculated by the probability theory, but the process is very complicated. For simplicity, we use the computer simulation. An adhoc event-driven simulator has been built and tested.

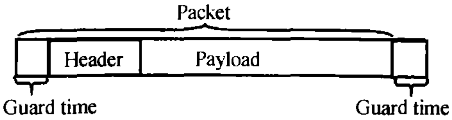


Fig. 2 Packet format

Simulation results show the PLR is independence of the load, which is shown in Fig. 3. However the PLR depends on the number of the port. Fig. 4 shows the relationship between the demands for the FDLs and the number of the port. The number port is from 4 to 80. We can see, when the number of the port is larger than 5, the ratio of demands for the type 3-1 FDLs are higher than the type 1-3, so the demands for three 1D FDLs is higher than demand on one $3D$ FDLs. When the number of the port is larger than 6, the demands for the type 2-1 FDLs are higher than the types 1-2 and 1-3 too, so the demand on two $1D$ FDLs is higher than demand on one $2D$ FDL or one $3D$ FDL.

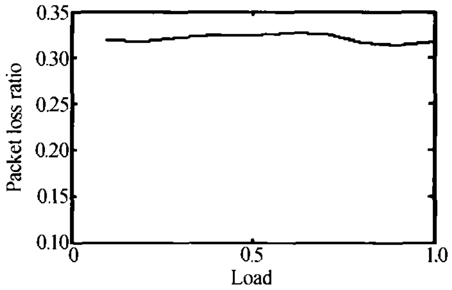


Fig. 3 PLR vs. load

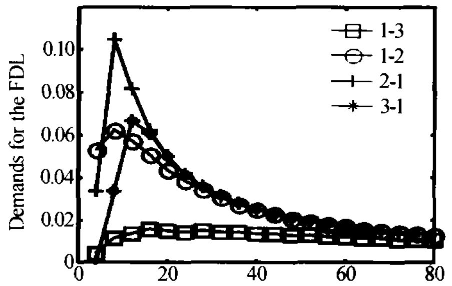
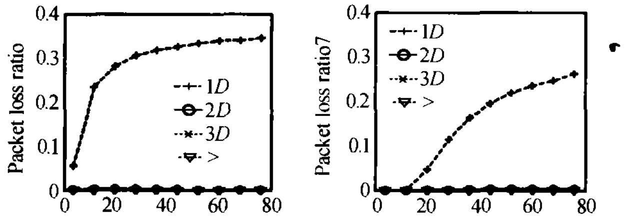


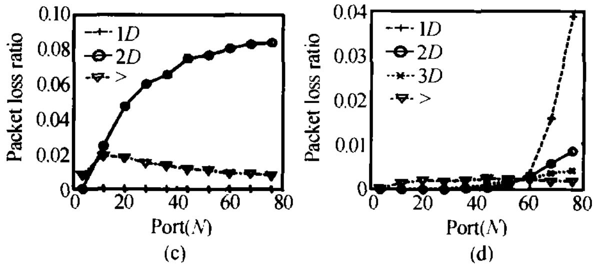
Fig. 4 The demands for the FDLs vs. number of the port

Then, we study the switch with FDLs. In this instance, the policy of choosing the FDLs is: when there is a contention, if there is no favorable FDL, the incoming packet will be dropped, despite possible free FDLs with larger time delay. So, the lost packets are composed of two types. One is produced due to the taking up of appropriate FDL; another is produced that the delay time needed goes beyond the limits of the maxim delay granularity of FDL(MD).

When the switch is configured with uniform and M ($M=30$) consecutive multiples of delay granularity, which is shown in Fig. 1. The simulation results of two kinds of PLR are shown in Fig. 5 (a). The PLR is including the PLR deduced by the exceeding of the maxim delay granularity of FDL, which is marked by "∇" and another one is produced due to the taking up of appropriate FDL, which is marked by other marker. The total PLR is shown in Fig. 6. It's clear that the PLR due to the FDL 1D is lager than the PLR due to the FDL 2D; most of lost packets are produced by the lack of the small granularity FDL. So a good method to cut down the PLR is by increasing the proportion of the small granularity FDL at a cost of decreasing the proportion of the large granularity FDL.



(a){1-1D 1-2D 1-3D...1-29D 1-30D} (b){5-1D 4-2D 3-3D 3-4D 3-5D 2-6D 2-7D 1-8D 1-9D...1-14D 1-15D}



(c){29-1D 1-2D} (d){19-1D 8-2D 3-3D 2-4D}

Fig. 5 The all kinds of PLR vs. the number of the port in different FDL configuration

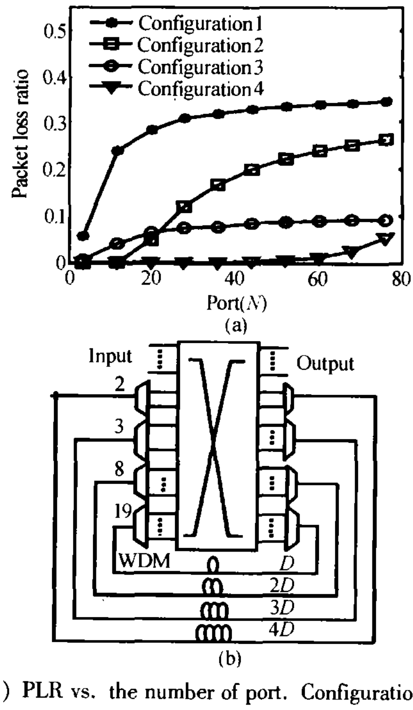


Fig. 6 (a) PLR vs. the number of port. Configuration1: {1-1D 1-2D 1-3D01-29D 1-30D}; Configuration2: {5-1D 4-2D 3-3D 3-4D 3-5D 2-6D 2-7D 1-8D 1-9D 1-10D 1-11D 1-12D 1-13D 1-14D 1-15D}; Configuration3: {29-1D 1-2D}; Configuration4: {19-1D 8-2D 3-3D 2-4D}; (b) the new switching matrix fabric

As a proof of principle and to test the conjecture, we simulate such two architectures of the FDL: {5-1D 4-2D 3-3D 3-4D 3-5D 2-6D 2-7D 1-8D 1-9D 1-10D 1-11D 1-12D 1-13D 1-14D 1-15D} and {19-1D 8-2D 3-3D 2-4D}. The distributions of lost packets are shown in Fig. 5 (b)、(d). Fig. 6(a) is the comparisons of PLR between the uniform degenerate configuration architecture and the novel architecture. Fig. 6 (a) shows that the novel one has much low PLR than the uniform degenerate configuration.

But, it's not true that the more small granularity FDL, the better the performance. We simulate such an architecture of the FDL: {29-1D 1-2D}, which is shown in Fig. 5 (c). The PLR is shown in Fig. 6 (a), curve with mark 'o' represents the architecture, we can see that the PLR is not lower than configuration 4 {19-1D 8-2D 3-3D 2-4D}. This is because the PLR deduced by the exceeding of the maxim delay granularity of FDL, which is represented with mark '∇' in Fig. 5(c), is increasing a little bit when the proportion of the small granularity FDL is increasing in FDL group. Which is shown in Fig. 5 (c) above. So there must be a tradeoff between the two kinds of lost packets: one produced due to the taking up of appropriate FDL; another one produced that the delay time needed goes beyond the limits of the maxim delay granularity of FDL.

From the simulations of multifarious FDLs combination, we can get the most optimal configuration, which has been simulated and shown in Fig. 5(d) above. Fig. 6 is the structure of the switch configured with new optical buffer scheme{19-1D 8-2D 3-3D 2-4D}.

According to these results, we can presume that by using reasonable configuration of the granularity and depth of the FDL, we can depress the PLR effectively. Instead of using one FDL in each granularity, we use different depth (different number FDLs) in each granularity; the depth depends on the higher probability of collisions, from the probability of collisions, using much more FDLs in small granularity FDL (such as 1D) than high granularity FDL.

3 Conclusions

In this paper, we introduce a novel optical FDL configuration. Given the restrictions on FDL number, this method can build more efficient FDL buffers with better performance. Simulation results show that the novel FDL configuration improves the PLR than uniform one.

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时隙光分组交换网络中一种新的光缓存优化配置方案

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收稿日期:2003-05-20

摘　要　研究了时隙光分组交换网中的光缓存配置方案,针对反馈共享式缓存结构,通过对传统的连续分布式光缓存结构中不同延迟粒度的光缓存丢包的分布情况仿真结果研究,发现在传统的连续分布式光缓存结构中,丢包主要发生在小粒度的光缓存上,为此,提出通过适当增加小粒度的光缓存的方法,达到有效地降低丢包率,仿真结果显示,这种光缓存方案可以明显降低节点的丢包率.

关键词　光分组交换;光缓存;光纤延迟线;时隙

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