Optical Phased Array Beam Deflector Drive Study*

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Abstract A drive system for a 16-channel waveguide optical phased array beam deflector is presented, where the control unit for drive voltage regulation is implemented with a field programmable gate array (FPGA) chip. With the drive system, a beam scan rate above 580 kHz can be achieved, which is far higher than that obtained with other implementation methods based on microcontrollers.

Keywords Optical phased array; Beam deflector; Voltage regulation
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0 Introduction

A optical phased array beam deflector (OPABD) is comprised of an array of equi-spaced optical phase shifters made of materials with electro-optic effect. It deflects light beam by phase modulating that is achieved through regulating voltages on the phase shifters. Compared to other scanning mechanisms, OPABD promises to satisfy many of the desired needs of beam steering[1]. Electro-optic response time of most materials (e.g. $LiNbO_3$, PLTZ, AlGaAs) used for the phase shifters is typically in the magnitude of sub-nanosecond, nanosecond and even picosecond, so that the beam deflection speed virtually depends on performance of control circuit of voltage regulation for OPABD.

As early as 1989, Hobbs et al.[2] reported a 5-channal AlGaAs electro-optic phased array device that reached a 500 kHz beam scan rate. Several years later, McManamon et al.[1] developed a OPABD device based on a nematic liquid crystal. Drive and control of the device was realized via custom built electronics resident within an 80486-based EISA bus computer. In this device, update time of the beam steering direction for a 256-channel independent module could be short to 88 μs, corresponding to a 11.3 kHz refresh rate. Recently a 4-channel OPABD for low-voltage drive with AlGaAs material was demonstrated[3], where control of drive was provided by a microcontroller chip 89C51. Under serial software control, beam scan rate with the 4-channel OPABD was below 10 kHz.

Here a FPGA-based voltage regulation drive system for a 16-channel AlGaAs waveguide OPABD is described and shown to be much superior in realizing high scan rate to an implementation of the drive system based on a microcontroller.

1 Voltage regulation for OPABD

As shown in Fig. 1, a AlGaAs waveguide OPABD has a multilayer structure and is based on the electro-optic effect in epitaxially grown semiconductor AlGaAs layers sandwiched by conducting electrode layers.

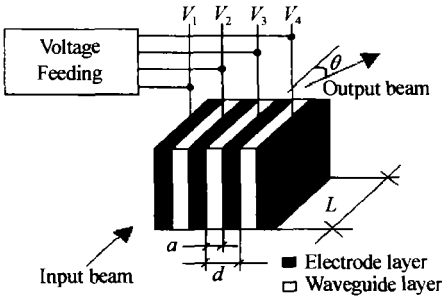

Fig. 1 Beam deflecting of a waveguide OPABD

With an analysis of Fourier optics and crystal optics[4,5] it is known for a N-channel AlGaAs OPABD that the voltage ΔV_{mi} applied on the m^{th} shifter is required to generate a corresponding resolvable deflection angle $\theta = i\Delta\theta\,(i = 0, \pm 1, \pm 2, \cdots, \pm (N/2)_{int})$, which is given as follows

$$\Delta V_{mi} = \left[i\frac{2\lambda a}{Nn_0^3 r_{41} L}(m-1) \right] \bmod \left[\frac{2\lambda a}{n_0^3 r_{41} L} \right]$$

$$m = 1, 2, \cdots, N$$

where λ is the wavelength of the input beam, n_0 is the index of refraction of the material in the absence of the electric field, r_{41} is the electro-optic coefficient of the material, L and a are the dimensions of the layer as shown in Fig. 1. The equation is as basic drive formula for beam deflectors based on AlGaAs waveguide optical phased array.

2 Design of the drive system

It is increasing difficult to implement voltage regulation with analogue circuits for a waveguide OPABD when the number of waveguide layers is increased. An approach for the voltage regulation is to

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use D/A conversions based on a microcontroller that takes data from a ROM into D/A converters to generate the required voltages. This method is flexible in control, but time-consuming due to the control program running, and thus results in low scan rate of light beam.

Here is a new drive system accomplishing voltage regulation for a 16-channel waveguide OPABD as shown in Fig. 2, in which a control unit for voltage regulation is developed and implemented in a FPGA chip. According to the previous section, there are 256 voltages ΔV_{mi} on 16 waveguide layers for 16 resolvable deflection angles. With these waveguide voltages we can get voltages V_m applied to the electrode layers, and data relating to the electrode voltages, which are prestored in a 256 × 8-bit ROM configurated in the control unit. For this design, 8-bit and current-output type D/A converters TLC7524 from Texas Instruments are selected. The converter with 100 ns setting time is innerly single-stage buffered, and therefore an extra buffer stage between the control unit and the D/A converters is needed.

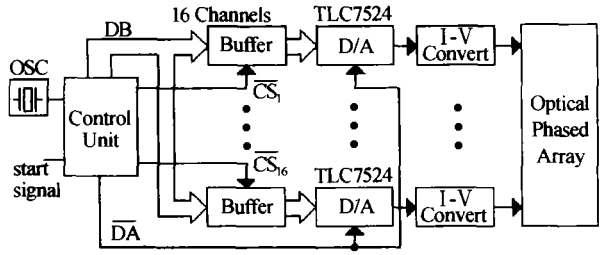

Fig. 2 Block diagram of the OPABD

The control unit comprises three functional blocks shown in Fig. 3, where address of the 256 × 8 ROM are provided by the address generator realized with a 8-bit binary counter. An external frequency oscillator (OSC) affords a system clock of 160 MHz, from which all control signals are derived. The start signal in the figure is used as a trigger signal for scan of light beam. In sequence, the timing logic in the control unit generates the strobing signals /CS_i, respectively for 16 external buffers, and the strobing signal/DA for internal buffers of all TLC7524. In addition, the timing logic offers a counting enable (CE) signal for the address generator . Fig . 4 shows the simplified

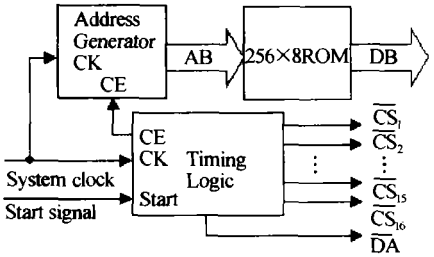

Fig. 3 Structure of the control unit

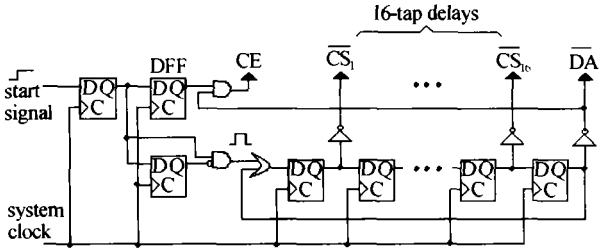

Fig. 4 Schematic of the timing logic

schematic of the timing logic. In the figure, D-type flip-flops (DFFs) are used to form the strobing signals that are cyclically presented through a feedback of Q output of the last DFF.

Operation of the drive system is described as follows: when the address generator in the control unit is enabled, 16 strobing signal /CS_i lead 16 ROM-element data generated electrode voltages for a resolvable deflection angle to enter 16 external buffers respectively, and then the /DA signal makes the buffered data simultaneously into the internal buffers of all TLC7524s, which starts the D/A conversions of TLC7524s. During validity period of the /DA signal the address generator is disabled. The above-mentioned process is circulated for next resolvable deflection angles, so that scaning of light beam is performed.

In the Fig. 5 timing sequence of signals in the control unit is shown. It is known from this that 17 × 16 cycles of the system clock CK are required for a complete scaning, which is 1700 ns corresponding to a scaning rate of 588 kHz.

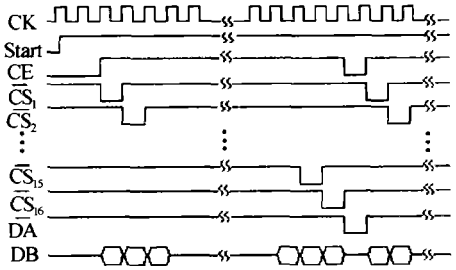

Fig. 5 Timing sequence of the control signals

3 Implementation of the control unit

A prototype of the control unit is implemented in a Xilinx Spartan II FPGA chip. The FPGA is selected as a hardware platform, because it has system frequency as high as 200 MHz, and provides plentiful and reconfigurable logic and memory resources. A look-up table based configurable logic block (CLB) in Spartan II can be used as four 16 × 1-bit ROMs or as two 32 × 1-bit ROMs, with which a 256 × 8-bit ROM can be constructed. The design and verification of the control unit are performed with an EDA tool (integrated software environment ISE and ModelSim from Xilinx

Co.). From the output report of the EDA tool it is shown that the control unit has utilized 46 CLBs, in which 184 independent 4-input logic function generators have been used.

4 Conclusion

In summary, the design and implementation of the drive system for the waveguide OPABD are based on a FPGA, with which a high scaning rate of light beam is gotten. In addition, goals of low cost and short time for research & development of the drive system are reached.

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光学相控阵光偏转器的驱动研究

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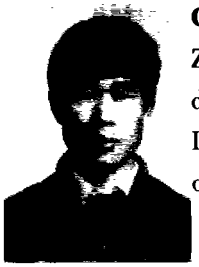
摘 要 提出了一个用于16通道波导光学相控阵光偏转器的驱动系统, 其中电压调节控制单元用一个现场可编程门阵列(FPGA)芯片实现. 这个系统可使该OPABD的光束扫描速率达到580 kHz以上, 远远高于基于微控制器的驱动系统所能达到的水平.

关键词 光学相控阵; 光偏转器; 电压调节



Gong Xiangdong was born in 1956. He received a B. S. degree and a M. S. degree from Zhejiang University in 1982 and in 1984, respectively. As visiting scholar he worked in Germany during 1989-1990 and 1994-1996. He is presently a professor at the Department of Photonic Information Engineering of Shenzhen University. His research interests include transient optoelectronic technology, hardware and software design for optical instruments.