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紧凑型宽带低损耗3 dB功率分配器设计与制备

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摘要 光功率分配器作为光子集成电路中分束并束的关键器件，要求结构紧凑、宽带、低损耗。基于亚波长光栅(SWG)结构，提出一种分束区域长5 μm、分光比为50∶50的超大带宽低损耗3 dB光功率分配器。仿真结果表明，该光功率分配器在±15 nm的大工艺容差下，TE模式在1.26～2.02 μm波段内(即760 nm带宽)损耗低于0.54 dB。通过电子束曝光、干法刻蚀等工艺在绝缘体上硅(SOI)晶圆上加工制备该光功率分配器，在扫描电子显微镜(SEM)下观察SWG结构的加工误差不超过±10 nm。此外，搭建垂直耦合测试平台，利用可调谐激光器在1496.8～1600 nm波段，对TE模式的损耗与分光比进行测试。结果表明，该波段损耗约为0.3 dB，与仿真结果吻合，分光比误差在5%以内。该功率分配器适用于高速、大容量通信、波分复用(WDM)系统等互联应用场合。

关键词 紧凑；宽带；低损耗；光功率分配器

中图分类号 TN256 **文献标志码** A **DOI**：10.3788/AOS230935

1 引 言

在光通信领域，2 μm有望成为继850 nm、1310 nm、1550 nm之后的近红外第4个窗口[1-3]。随着大容量通信的发展，设计与制备具有紧凑型体积、低损耗覆盖O、E、S、C、L、U波段(1.26～1.675 μm)和2 μm波段全通信带宽的光子集成电路，成为该领域的研究热点[4-10]。光功率分配器作为光子集成电路的重要组成部分，广泛应用于大容量通信和互联领域。作为基础器件，其支持波分复用(WDM)系统、调制器[11]、光开关[12]等器件的设计与开发。具有突破性带宽的功率分配器在片上超宽带系统中发挥基石作用，其研发具有重要意义。

经典的片上光功率分配器有3种类型：定向耦合(DC)型、多模干涉(MMI)型和Y分支型。其中，DC型光功率分配器由于倏逝场耦合强烈依赖于波长，往往带宽有限[13]；MMI型光功率分配器由于绝缘体上硅(SOI)波导的强模式色散，同样面临带宽受限的问题[14-15]。当传统的Y分支角足够小(约1°)时，Y分支型光功率分束器过渡损耗较低，对波长的依赖性不明显[16]，可以扩大应用带宽。然而，这种传统的设计对尖角处的制造误差很敏感，尖角缝隙中的光刻胶或蚀刻残渣会导致明显的辐射损耗并引起分光不均[17]。目前，能实现包括2 μm波长的超大带宽光功率分配器少有报道[4-5,18]。哈尔滨工业大学徐科教授课题组[5]提出一种在1500～2020 nm波长范围内，附加损耗(L_{EL})小于0.2 dB的3 dB光功率分配器，极大地扩展了光功率分配器的带宽范围。然而，能够覆盖O、E、S、C、L、U波段(1.26～1.675 μm)和2 μm波段全通信带宽的光功率分配器仍然鲜有报道。

根据等效介质理论(EMT)[19]，通过设计亚波长结构可以获得自然界不存在的折射率，这为光子集成电路的器件设计带来了极大的灵活性。随着微纳制造技术的发展，亚波长结构设计得到了更好的应用。许多器件通过引入亚波长结构实现了宽带应用[20]，包括偏振分束器[21]、偏振旋转器[22]、移相器[23]、光纤芯片边缘耦合器[24]、滤波器[25]等。受此启发，基于SOI平台，结合亚波长结构，提出一个超大带宽3 dB光功率分配器。

为了实现宽带应用，本文在设计中引入折射率可调的亚波长光栅(SWG)结构。以一种新型结构取代传统Y分支型光功率分配器的尖角设计，从根本上解决实际加工中在尖角处遇到的难题。将绝热锥形结构、亚波长光栅结构和分支波导相结合来实现光波的均匀、平滑分离，在考虑加工容差的基础上，仿真结果表明，所设计器件具有超大带宽(1.26～2.02 μm)和超

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小尺寸(分光区域仅 5 μm),且附加损耗小于 0.54 dB。在实测性能上,实现了超过 100 nm 的带宽和 5% 以内的分光误差。该器件支持片上超宽带系统的设计,如宽带调制器、宽带光开关和其他多波段光子集成系统。

2　器件原理与设计

该器件在SOI平台上设计,具有 220 nm 厚的顶部硅层(在 1550 nm 处 $n_{Si}\approx3.47$)和 3 μm 厚的二氧化硅绝缘层(在 1550 nm 处 $n_{SiO_2}\approx1.44$),上包层为空气($n_{air}\approx1$),如图 1 所示。图 1 中 L_c 表示耦合区域长度,g 表示耦合间隙,Λ 表示亚波长光栅的周期,f_M 表示亚波长光栅的最大占空比,f_m 表示亚波长光栅的最小占空比,f_i 表示第 i 个亚波长光栅条的占空比。依次连接直波导、绝热锥形波导结构、两个平行直波导和两个分支波导组成 3 dB 光功率分配器,并使用亚波长光栅填充两个平行的直波导。当基本 TE 模通过时,光波在分支波导上均匀分离。

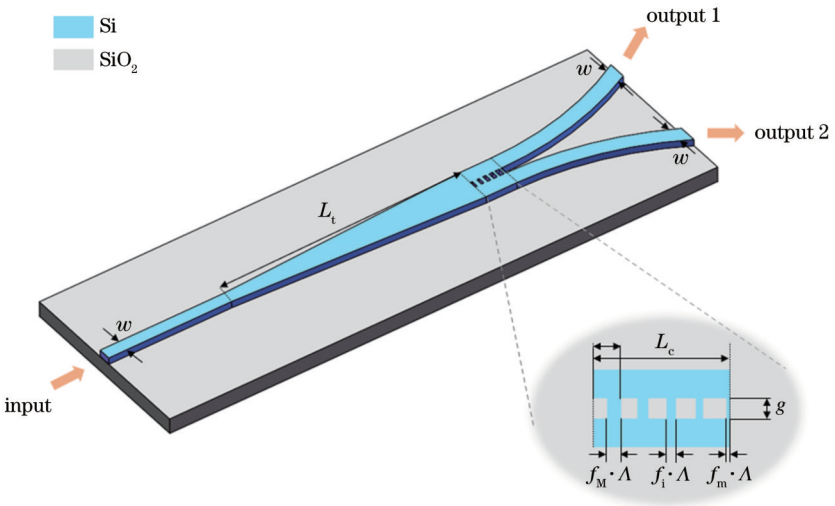

图 1　所提 3 dB 光功率分配器

Fig. 1　Proposed 3 dB optical power splitter

使用 L_{EL} 来评价 3 dB 光功率分配器的性能:

$$L_{EL}=-10\cdot\log_{10}(T_{Output1}+T_{Output2}),\tag{1}$$

$$\begin{cases}T_{Output1}=\dfrac{P_{Out1}}{P_{In}}\\ T_{Output2}=\dfrac{P_{Out2}}{P_{In}}\end{cases},\tag{2}$$

式中:$T_{Output1}$ 和 $T_{Output2}$ 是基本 TE 模在两个分支末端的透射率;P_{Out1}、P_{Out2} 分别为图 1 中两个输出端的光功率;P_{In} 为图 1 中输入端的光功率。

由于 TE 偏振和 TM 偏振电场的主要分量都垂直于光束的传播方向,因此可将亚波长光栅视为具有等效折射率的均匀介质。其等效折射率[26]可近似表示为

$$n_{SWG}^2=f\cdot n_{Si}^2+(1-f)\cdot n_{air}^2,\tag{3}$$

式中:f 为亚波长光栅中的占空比;n_{SWG} 为亚波长光栅的等效折射率。根据式(3)可知,亚波长光栅的等效折射率可以通过占空比进行调节和控制,亚波长光栅能够提高两个平行直波导中间狭缝内的等效折射率,减小狭缝区域与分支波导间的折射率差。因而,在引入亚波长光栅时,将在较大的带宽范围内有效降低 L_{EL}。设计沿分光方向亚波长光栅的占空比逐渐减小,构建出折射率下降均匀台阶,使得 L_{EL} 在更大的带宽范围下保持低水平。使用式(4)计算沿分光方向第 i 个光栅条的占空比,使占空比均匀减小:

$$f_i=(f_M-f_m)\cdot\frac{n-i}{n-1}+f_m,\tag{4}$$

式中:f_M 为最大占空比;f_m 为最小占空比;n 为亚波长光栅的层数。通过仿真优化,取亚波长光栅的周期 Λ 为 200 nm、n 为 5、f_m 为 0.3、f_M 为 0.5、波导宽度 w 为 400 nm、耦合区域长度 L_c 为 1 μm、耦合间隙 g 为 160 nm。利用三维时域有限差分法(3D FDTD)在光纤通信的全波段:O、E、S、C、L 和 U 波段(1.26~1.675 μm)及 2 μm 波段上仿真,得到该器件在 3 个常用波长 1260 nm、1550 nm 和 2000 nm 下的场分布、全通信带宽下的 L_{EL} 以及考虑 30 nm 加工容差后的性能,具体如图 2 所示。结果表明,考虑±15 nm 的工艺误差情况下,本设计可覆盖 O、E、S、C、L 和 U 波段(1.26~1.675 μm)及 2 μm 波段,在 760 nm 的超大带宽内保持低于 0.54 dB 的低损耗工作。

3　工艺制备与测试

为验证所提光功率分配器的性能,在顶层硅为 220 nm 厚的标准 SOI 晶圆上完成其制备,并在光功率分配器的输入输出端制备具有 70 nm 浅刻蚀的光栅耦合器,用于光纤与待测光学芯片的垂直耦合。工艺流程如图 3 所示。

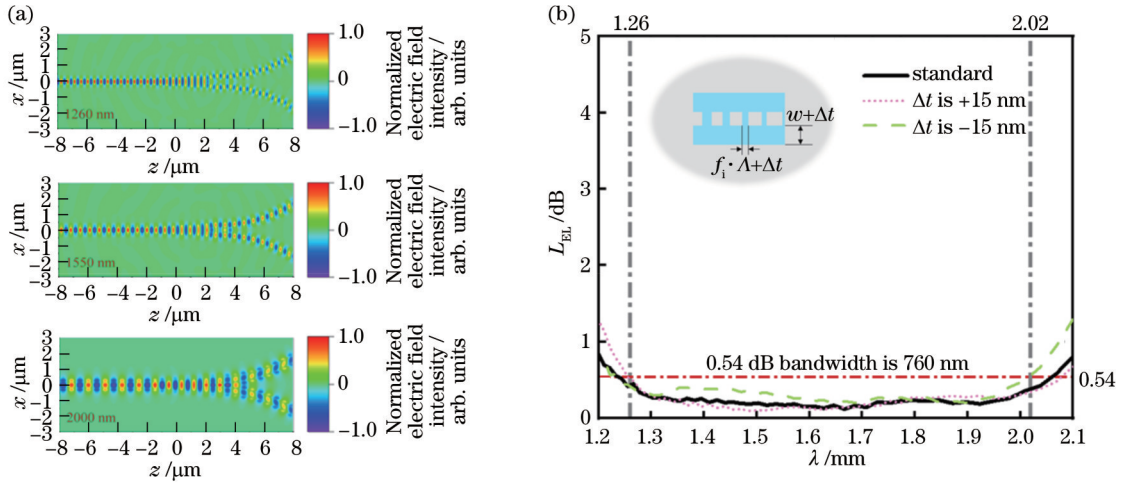

图 2　所提 3 dB 光功率分配器的场分布与性能分析。(a)基本 TE 模(E_x)在 3 种波长下的场分布;(b)该 3 dB 光功率分配器的理想性能与±15 nm 加工误差影响下的性能

Fig. 2　Field distribution and performance analysis of the proposed 3 dB optical power splitter . (a) Field distribution of the fundamental TE mode (E_x) at three wavelengths; (b) the ideal performance of the 3 dB optical power splitter and its performance under the influence of ±15 nm processing error

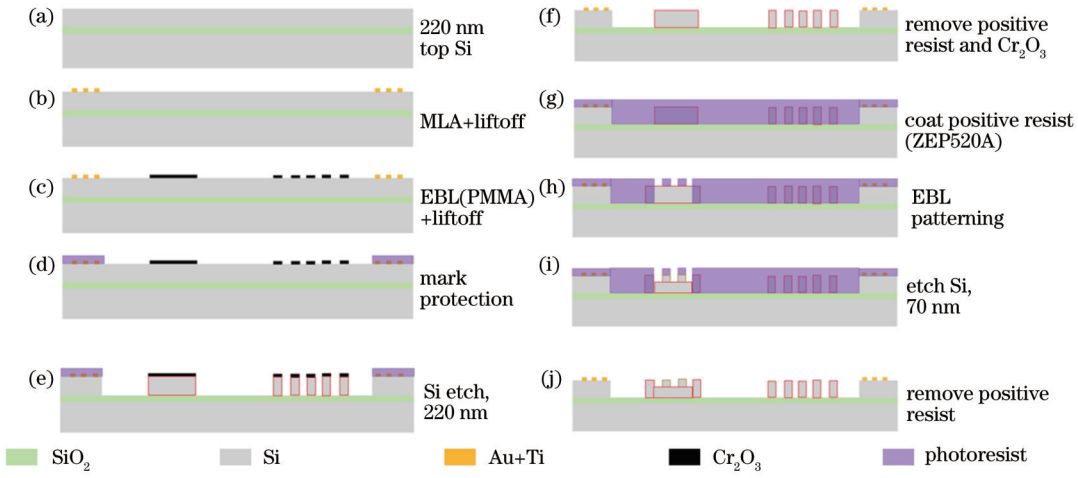

图 3　制备光功率分配器与光栅耦合器的工艺流程

Fig. 3　Process of preparing optical power splitter and grating coupler

图 3(a)～(f)是光功率分配器的制备工艺流程,图 3(g)～(j)是光栅耦合器的制备工艺流程。首先,对 8 inch SOI 晶圆进行划片(1 inch=2.54 cm),切割出 4 cm×4 cm 单元,然后进行划片后的清洗。由于光栅耦合器上存在 70 nm 浅刻蚀,故需要采用 liftoff 工艺制作套刻对准用的金属标记,同时使用激光直写(MLA)实现曝光。其中,通过电子束蒸发(EBE)实现金属的沉积。通过第 1 次电子束曝光(EBL)与 EBE 完成光功率分配器与光栅耦合器在刻蚀深度 220 nm 上的 Cr_2O_3 硬掩膜的制作。接下来,对套刻标记进行保护处理[由于 Au 材料不能进入感应耦合等离子体刻蚀机(ICP-RIE)中,会造成机器污染,所以在金属标记处用光刻胶做保护层]并使用 ICP-RIE 完成第 1 次硅刻蚀(刻蚀深度 220 nm,包括形成光功率分配器形貌与光栅耦合器除 70 nm 浅刻蚀光栅凹槽外的其他部分形貌)。最后,通过第 2 次 EBL 与第 2 次 ICP-RIE 刻蚀(刻蚀深度 70 nm)完成套刻,即光栅耦合器部分 70 nm 浅刻蚀凹槽的制作。

制备好的光功率分配器在扫描电子显微镜(SEM)下的照片如图 4 所示。图 4(a)中的 3 个结构分别为级联多个光功率分配器、单个光功率分配器、一对背靠背的光栅耦合器;图 4(b)为单个光功率分配器;图 4(c)为单个光功率分配器在分光区域的细节放大;图 4(d)为 SWG 区域的实际加工尺寸,分别是 89.46 nm、91.45 nm、105.4 nm、111.3 nm、125.2 nm,与设计值相差不超过±10 nm。

基于使用光栅耦合器的垂直耦合平台对所提光功率分配器进行性能测试,通过依次连接是德光波测量系统(LMS)8164B 的内置可调谐激光源模块 81600B、起偏器(polarizer)、偏振控制器(PC)、待测器件(DUT)、

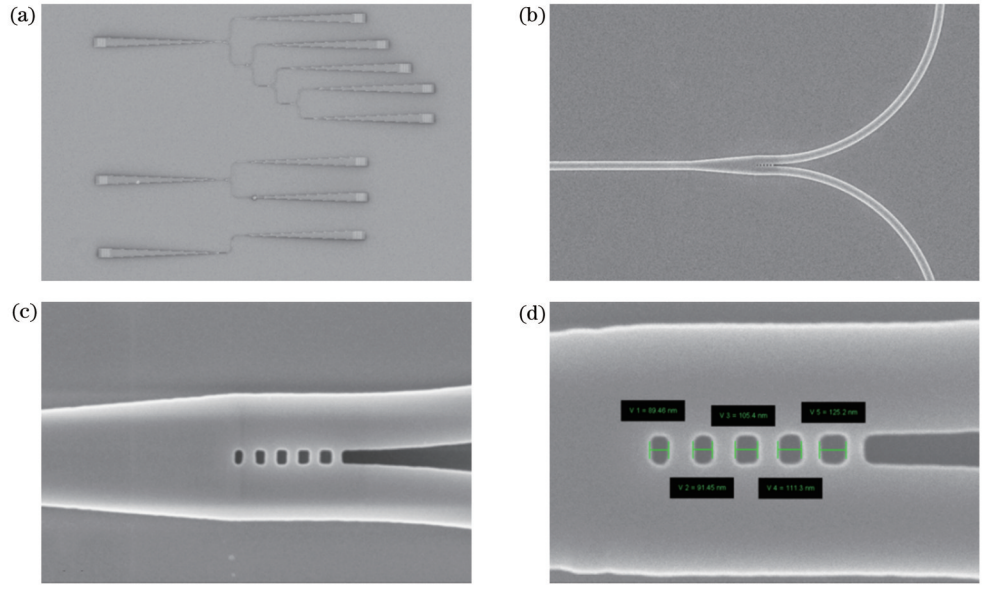

图 4　光功率分配器的 SEM 图。(a)光功率分配器芯片整体;(b)单个光功率分配器;(c)单个光功率分配器在分光区域的细节放大;(d) SWG 区域的实际加工尺寸

Fig. 4　SEM images of the optical power splitter. (a) Optical power splitter chip as a whole; (b) individual optical power splitter; (c) detail enlargement of individual optical power splitter in the beam splitting area; (d) actual processing dimensions of SWG region

是德光功率探头(OH)81623B 与是德光波测量系统 8164B 完成测试系统搭建,在是德光波测量系统 8164B 背部以串口 GPIB-USB-HS 连接电脑主机,进行测试系统的数据采集与存储,如图 5 所示。在测试过程中,先通过 DUT 输出端连接光功率计,移动光纤找到最大输出功率后,再换接是德光功率探头 81623B。

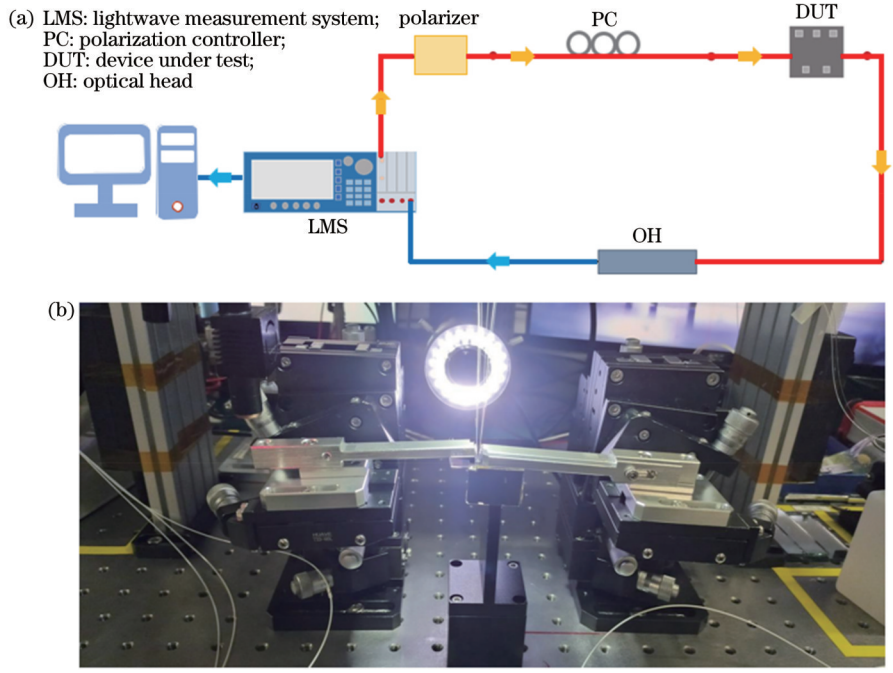

图 5　测试时使用到的设备。(a)垂直耦合测试系统示意图;(b) 垂直耦合测试平台

Fig. 5　Equipment used in the test. (a) Diagram of vertical coupling test system; (b) vertical coupling test rig

由背对背光栅耦合器可以测得光栅耦合器损耗,通过对照实验,在终端测试结果中去除光栅耦合器的损耗即可得到光功率分配器的损耗。由于单个光功率分配器的损耗较小(<0.5 dB),测试设备存在噪声可能导致测量不准,故选取级联 4 个光功率分配器的待测芯片进行测试,并通过取平均的方式得到单个光功分器的附加损耗。受实验系统光源带宽限制,仅在 1496.8~1600 nm 波段下进行测试,实测结果与仿真结果对比如图 6 与图 7 所示。制备的光功率分配器在 1496.8~1600 nm 波段下的实测损耗与仿真结果近乎一致,损耗

大概在 0.3 dB 左右；实测分光比在 45%～55% 之间。与其他科研单位的光功率分配器性能对比如表 1 所示：Yi 等[4]首次展示了在 1.55 μm 和 2 μm 波段工作的基于双波段 MMI 的 3 dB 功率分配器；Wang 等[5]展示了可应用于 1.55 μm 和 2 μm 波段工作的基于均匀亚波长结构的 Y 分支型 3 dB 功率分配器；Fernández de Cabo 等[27]展示了可应用于 1300～1700 nm 波段的基于均匀亚波长结构的宽带 Y 分支型 3 dB 功率分配器；Han[28]展示了可应用于 1260～1680 nm 波段的基于亚波长结构各向异性的 Y 分支型 3 dB 功率分配器。所提渐变亚波长结构光功率分配器在仿真中实现了低损耗覆盖 O、E、S、C、L、U 波段（1.26～1.675 μm）和 2 μm 波段的全通信带宽，在考虑 ±15 nm 工艺容差下，仿真带宽达到 760 nm。在 1496.8～1600 nm、103.2 nm 带宽范围内的测试结果表明，附加损耗为 0.3 dB，与仿真数据吻合，证明了仿真的有效性与器件加工的可行性。此外所提分配器的有效分光区域长度仅为 5 μm，极大地减小了器件的有效尺寸。

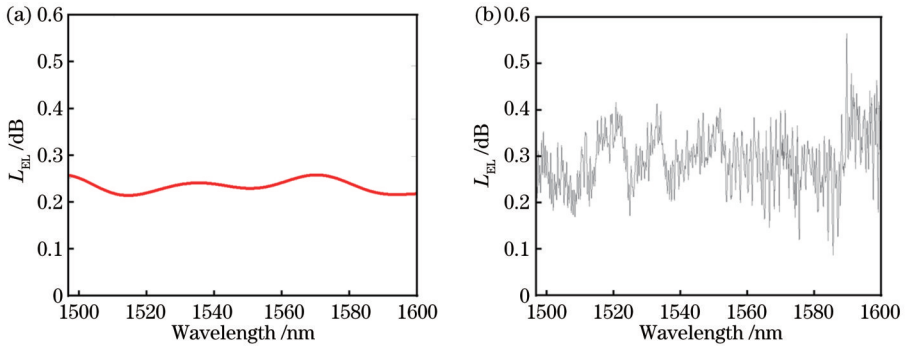

图 6 仿真与测试结果的对比。(a)仿真下光功率分配器的附加损耗；(b)实测下光功率分配器的附加损耗

Fig. 6 Comparison of simulation and test results. (a) Excess loss of optical power splitter under simulation; (b) actual measurement of the excess loss of the optical power splitter

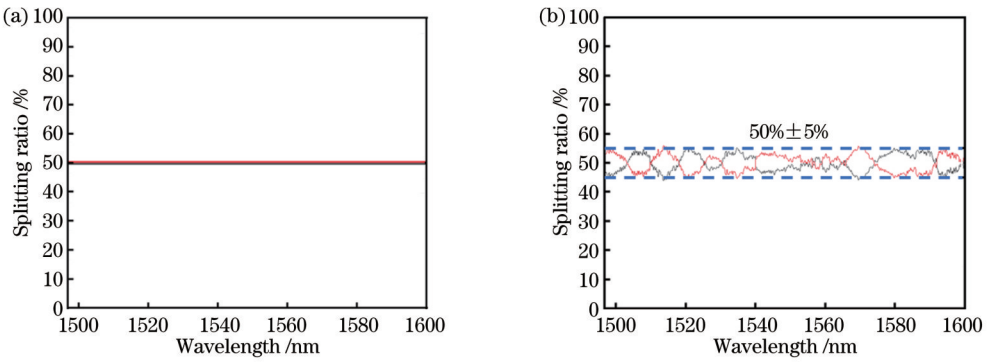

图 7 仿真与测试结果的对比。(a) 仿真下光功率分配器的分光比；(b) 实测下光功率分配器的分光比

Fig. 7 Comparison of simulation and test results. (a) Splitting ratio of optical power splitter under simulation; (b) actual measurement of the splitting ratio of the optical power splitter

表 1 基于 SOI 平台的光功率分配器性能参数对比表

Table 1 The performance comparison table of optical power splitter based on SOI platform

Reference	L_{EL} /dB		Splitting ratio			Wave band /nm	
	Simulation	Actual test	Simulation	Actual test	Size /μm	Simulation	Actual test
[4]	<0.8	<1	50∶50	<53.16∶46.84	72.7	1500-1600	1500-1600
[5]	<0.2	<0.4	50∶50	<50.91∶49.09	3	1500-2020	1500-1620
[27]	<0.5	<0.6	50∶50		41.3	1300-1700	1410-1680
[28]	<0.4	<1	50∶50	<58∶42	18.4	1260-1680	1260-1680
This work	<0.54	~0.3	50∶50	<55∶45	5	1260-2020	1496.8-1600

4 结 论

应用等效介质理论完成紧凑、宽带、低损耗的硅基光功率分配器设计，使用 3D FDTD 方法对器件的性能进行模拟优化及仿真容差处理。在设计中引入折射率可调的亚波长光栅结构，以一种新颖的结构取代传统 Y 分支的尖角设计，从根本上解决尖角在实际加工中遇到的问题。所提硅基光功分器在 ±15 nm 的大工

艺容差的条件下，TE模式在1.26～2.02 μm波段内（即760 nm带宽下）损耗低于0.54 dB。首次在仿真中实现了低损耗覆盖O、E、S、C、L、U波段（1.26～1.675 μm）和2 μm波段的全通信带宽。其有效分光区域长度仅为5 μm，极大地减小了器件的有效尺寸，实现了紧凑型器件设计。该器件证明了小尺寸、大工艺容差下，单个光功率分配器实现全通信带宽低损耗覆盖的可行性。对于片上大容量，超宽带通信系统的设计具有重要的意义。此外，经历旋涂光刻胶、电子束曝光、激光直写、显影、定影、干法刻蚀等操作完成光功率分配器的加工制作，加工尺寸误差不超过10 nm，证明了该结构加工的可行性。搭建垂直耦合测试系统完成对光功分器的性能测试，1496.8～1600 nm波段下的实测损耗为0.3 dB左右，分光比在45%～55%之间，在该波段内实测指标与设计指标接近，实现了设计目标。

参 考 文 献

[1] Soref R. Enabling 2 μm communications[J]. Nature Photonics, 2015, 9(6): 358-359.

[2] Xu K, Sun L, Xie Y Q, et al. Transmission of IM/DD signals at 2 μm wavelength using PAM and CAP[J]. IEEE Photonics Journal, 2016, 8(5): 7906407.

[3] 王震, 谢文青, 豆奥举, 等. 掺铥钬离子碲锗酸盐玻璃2 μm发光性能研究[J]. 中国激光, 2020, 47(10): 1003004.
Wang Z, Xie W Q, Dou A J, et al. 2 μm fluorescence properties of Tm^{3+} and Ho^{3+} ions doped tellurite-germanate glass[J]. Chinese Journal of Lasers, 2020, 47(10): 1003004.

[4] Yi Q Y, Cheng G L, Yan Z W, et al. Silicon MMI-based power splitter for multi-band operation at the 1.55 and 2 μm wave bands [J]. Optics Letters, 2023, 48(5): 1335-1338.

[5] Wang Z L, Liu Y J, Wang Z, et al. Ultra-broadband 3 dB power splitter from 1.55 to 2 μm wave band[J]. Optics Letters, 2021, 46(17): 4232-4235.

[6] Xu K, Wu Q, Xie Y Q, et al. High speed single-wavelength modulation and transmission at 2 μm under bandwidth-constrained condition[J]. Optics Express, 2017, 25(4): 4528-4534.

[7] Li N, Jia H, Guo M, et al. Nano-Cs_xWO_3: Ultra-broadband nonlinear optical modulator for near-infrared and mid-infrared ultrafast fiber lasers generation[J]. Nano Research, 2022, 15(5): 4403-4410.

[8] Wang X, Shen W H, Li W X, et al. High-speed silicon photonic Mach - Zehnder modulator at 2 μm[J]. Photonics Research, 2021, 9(4): 535-540.

[9] Cao W, Hagan D, Thomson D J, et al. High-speed silicon modulators for the 2 μm wavelength band[J]. Optica, 2018, 5(9): 1055-1062.

[10] Zheng S A, Huang M, Cao X P, et al. Silicon-based four-mode division multiplexing for chip-scale optical data transmission in the 2 μm waveband[J]. Photonics Research, 2019, 7(9): 1030-1035.

[11] Yamaguchi Y, Kanno A, Kawanishi T, et al. Precise optical modulation using extinction-ratio and chirp tunable single-drive Mach - Zehnder modulator[J]. Journal of Lightwave Technology, 2017, 35(21): 4781-4788.

[12] Zhong C Y, Zhang Z B, Ma H, et al. Silicon thermo-optic switches with graphene heaters operating at mid-infrared waveband[J]. Nanomaterials, 2022, 12(7): 1083.

[13] Yamada H, Chu T, Ishida S, et al. Optical directional coupler based on Si-wire waveguides[J]. IEEE Photonics Technology Letters, 2005, 17(3): 585-587.

[14] Sheng Z, Wang Z Q, Qiu C, et al. A compact and low-loss MMI coupler fabricated with CMOS technology[J]. IEEE Photonics Journal, 2012, 4(6): 2272-2277.

[15] 汪静丽, 皇甫利国, 陈鹤鸣. 偏振无关多模干涉型1×3光功分器的设计[J]. 光学学报, 2021, 41(7): 0713001.
Wang J L, Huangfu L G, Chen H M. Design of polarization-insensitive multimode interference 1 × 3 optical power splitter [J]. Acta Optica Sinica, 2021, 41(7): 0713001.

[16] Love J D, Riesen N. Single-, few-, and multimode Y-junctions [J]. Journal of Lightwave Technology, 2012, 30(3): 304-309.

[17] Tao S H, Fang Q, Song J F, et al. Cascade wide-angle Y-junction 1 × 16 optical power splitter based on silicon wire waveguides on silicon-on-insulator[J]. Optics Express, 2008, 16(26): 21456-21461.

[18] Zhang Y G, Hu X A, Chen D G, et al. Ultra-broadband 3dB power splitter based on silicon slot waveguide[C]//Conference on Lasers and Electro-Optics, May 13-18, 2018, San Jose, California. Washington, D.C.: Optica Publishing Group, 2018: JW2A.8.

[19] Rytov S M. Electromagnetic properties of a finely stratified medium[J]. Sovphysjept Engltransl, 1956, 2(3): 202624512.

[20] 赵然, 孙崇磊, 徐晓, 等. 基于亚波长光栅的高集成度垂直光耦合器[J]. 光学学报, 2020, 40(14): 1405002.
Zhao R, Sun C L, Xu X, et al. Ultra-compact vertical optical coupler based on subwavelength grating[J]. Acta Optica Sinica, 2020, 40(14): 1405002.

[21] Xu H N, Dai D X, Shi Y C. Ultra-broadband and ultra-compact on-chip silicon polarization beam splitter by using hetero-anisotropic metamaterials[J]. Laser & Photonics Reviews, 2019, 13(4): 1800349.

[22] Xu H N, Shi Y C. Subwavelength-grating-assisted silicon polarization rotator covering all optical communication bands[J]. Optics Express, 2019, 27(4): 5588-5597.

[23] González-Andrade D, Luque-González J M, Gonzalo Wangüemert-Pérez J, et al. Ultra-broadband nanophotonic phase shifter based on subwavelength metamaterial waveguides[J]. Photonics Research, 2020, 8(3): 359-367.

[24] He A, Guo X H, Wang K N, et al. Low loss, large bandwidth fiber-chip edge couplers based on silicon-on-insulator platform [J]. Journal of Lightwave Technology, 2020, 38(17): 4780-4786.

[25] 廖莎莎, 包航, 冯玉婷, 等. 基于级联啁啾亚波长光栅辅助反向耦合器的超宽带可调滤波器[J]. 光学学报, 2022, 42(14): 1405003.
Liao S S, Bao H, Feng Y T, et al. Ultra-wideband tunable filter based on cascaded chirped subwavelength grating assisted reverse coupler[J]. Acta Optica Sinica, 2022, 42(14): 1405003.

[26] Mao S M, Cheng L R, Zhao C Y, et al. Ultra-broadband and ultra-compact polarization beam splitter based on a tapered subwavelength-grating waveguide and slot waveguide[J]. Optics Express, 2021, 29(18): 28066-28077.

[27] Fernández de Cabo R, González-Andrade D, Cheben P, et al. High-performance on-chip silicon beamsplitter based on subwavelength metamaterials for enhanced fabrication tolerance [J]. Nanomaterials, 2021, 11(5): 1304.

[28] Han S T, Liu W X, Shi Y C. Ultra-broadband dual-polarization power splitter based on silicon subwavelength gratings[J]. IEEE Photonics Technology Letters, 2021, 33(15): 765-768.

Design and Preparation of Broadband 3 dB Power Splitter with Compact Size and Low Loss

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Abstract

Objective Recently, in optical communications, 2 μm is expected to be the fourth window in the near-infrared after 850 nm, 1310 nm, and 1550 nm. The research on the devices, which could be applied to 1.26-1.675 μm and 2 μm bands with large broadband and low loss, follows the high-capacity communication development in the future. As part of the photonic integrated circuits (PICs), the optical power splitter is widely employed in high-capacity communication and interconnection scenes. It supports the design of wavelength division multiplexing (WDM) system, modulator, optical switch, and other devices. As a key device for beam splitting and beam merging, the optical power splitter requires compact structure, broadband, and low loss. The power splitter with breakthrough bandwidth will play a cornerstone role in the ultra-broadband systems on chip, which can cover the full communication bandwidth of O-, E-, S-, C-, L-, U-bands (1.26-1.675 μm) and 2 μm band with low loss.

Methods According to the equivalent medium theory (EMT), the refractive index of the dielectric that does not exist in nature can be obtained by designing the subwavelength structure, which brings high flexibility to the PIC design. With the progress in micro-nano fabrication, subwavelength structures are adopted to yield better performance. Many kinds of devices have achieved large bandwidths by introducing subwavelength structures, including polarization beam splitter, polarization rotator, phase shifter, and fiber-chip edge coupler. Inspired by this, we propose a 3 dB power splitter on the silicon-on-insulator (SOI) platform. Subwavelength grating (SWG) structures with adjustable refractive index are introduced to realize large bandwidths. Then the optical power splitter is fabricated on an SOI wafer using electron beam lithography and dry etching processes. Additionally, a vertical coupling test rig is set up to test the loss of the TE mode and the beam splitting ratio in the bands from 1496.8 nm to 1600 nm.

Results and Discussions As shown in Fig. 1, a novel structure is utilized to replace the traditional sharp-corner design in the traditional Y-branch, which radically solves the problems of actual processing in sharp corner. The light wave can be separated evenly and smoothly by the combination of adiabatic taper structure, SWG structure, and branch waveguides. The ultra-large bandwidth (1.26 μm-2.02 μm) and ultra-compact size can be obtained, which is shown in Fig. 2. Considering a large process tolerance of ±15 nm, the bandwidth of 760 nm is realized, with the excess loss (EL) less than 0.54 dB and the size of the beam splitting area 5 μm. The fabrication process and results are shown in Figs. 3 and 4 respectively. After preparation on an SOI wafer by electron beam lithography and dry etching processes, the processing error of the SWG structure is no more than ±10 nm when observed under the scanning electron microscope (SEM). As shown in Fig. 5, a vertical coupling test rig is set up to test the loss of the TE mode and the beam splitting ratio. In Figs. 6 and 7, the results show that the loss is about 0.3 dB in the bands from 1496.8 nm to 1600 nm, which is consistent with the simulation results, and the splitting ratio error is within 5% in the same waveband.

Conclusions A compact, broadband, and low-loss silicon optical power splitter is designed through the equivalent medium theory. The 3D FDTD method is leveraged to optimize the device performance and analyze the fabrication tolerance. The subwavelength grating structure with an adjustable refractive index is introduced to the design. Sharp corner design in the traditional Y branch is replaced by a novel SWG structure, which solves the problems in the actual machining of sharp corner. Under the large process tolerance of ±15 nm, the TE mode loss is less than 0.54 dB in the band of 1.26 μm to 2.02 μm (760 nm bandwidth). For the first time, the full communication bandwidth covering O-, E-, S-, C-, L-, U-bands (1.26 μm-1.675 μm) and 2 μm band with low loss is realized in the simulation. The effective length of the beam splitting region is only 5 μm, which greatly reduces the effective device size and realizes a compact device design. A single optical power splitter is proven to achieve low loss coverage of full communication bandwidth under

small size and large process tolerance. It is of significance to design communication systems with large capacity on the chip. Meanwhile, the optical power splitter processing has been completed through the operations of spin coating photoresist, electron beam exposure, laser direct writing, development, fixing, and dry etching. The processing size error is less than 10 nm, which proves the structure processing feasibility. The vertical coupling test system is established to complete the performance test of the optical power splitter. The excess loss is about 0.3 dB at 1496.8-1600 nm bands, and the spectral ratio is between 45% and 55%. The measured results in this band are close to the simulation to realize the design goal.

Key words compact; broadband; low loss; optical power splitter