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Lithography-friendly spot-size converter for thin-film lithium niobate photonics

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Conventional spot-size converters for thin-film lithium niobate require sub-100-nm features incompatible with standard dry etching. A 300-nm-lithography-compatible edge-coupled spot-size converter achieves a 3.5-μm mode field diameter at 1550 nm. With a matched single-mode fiber, it exhibits a single-facet coupling loss as low as 0.90 dB, average 1.0 dB, and alignment tolerances of ±1.1 μm vertically and ±1.45 μm horizontally. Monolithic integration with a 64-GHz modulator enables error-free 200-Gbps PAM-4 transmission with a transmitter dispersion eye closure for quaternary modulation of 2.39 dB, satisfying IEEE 802.3dj. This provides a practical, process-friendly fiber–chip interface for platforms lacking advanced nanofabrication.

Keywords: spot-size converter; thin-film lithium niobate; quartz substrate; PAM-4 transmission.

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1. Introduction

Thin-film lithium niobate (TFLN) has become a core platform for high-speed electro-optic (EO) modulators[1-5] due to its excellent EO coefficient, low optical propagation loss, and compatibility with integrated photonics[6–9]. However, the strong optical confinement in sub-micron TFLN waveguides yields a mode field diameter (MFD)[10-12] of merely 1 to 2 μm, far below the typical 3.5 μm of commercial single-mode fibers (SMFs), resulting in substantial mode mismatch upon direct coupling. Therefore, on-chip spot-size converters (SSCs)[13-17] remain essential for achieving efficient fiber–chip interfaces.

Two primary coupling strategies are employed in TFLN photonics: edge couplers and grating couplers[18-22]. While grating couplers enable wafer-scale testing, edge couplers remain indispensable for high-speed datacom due to their broader bandwidth and lower intrinsic loss. Grating couplers, especially those enhanced with metal mirrors and cavity structures, have recently achieved low fiber-to-fiber losses of 6.5 dB and perfectly vertical coupling, enabling wafer-scale testing and packaging, a significant advance demonstrated by Wang *et al.*[23] using ultraviolet (UV)-adhesive-bonded quartz substrates. Nevertheless, for high-speed datacom applications requiring minimal insertion loss (IL), broad bandwidth, and robust signal integrity, edge couplers remain the preferred solution due to their polarization insensitivity and lower intrinsic loss.

Beyond its excellent EO properties, TFLN also serves as an ideal host for rare-earth ion doping (e.g., Er^{3+}, Yb^{3+}), enabling on-chip lasers[24-27], optical amplifiers[28,29], and quantum memories, thereby supporting fully integrated active–passive photonic circuits.

To bridge this gap between theoretical performance and practical manufacturability, we present a 300-nm-lithography-compatible edge-coupled SSC monolithically integrated on a quartz-substrate TFLN platform. By leveraging the naturally formed 75° sidewall profile of standard reactive ion etching and optimizing a bilayer inverse taper structure, the device achieves a 3.5-μm output MFD at 1550 nm, enabling efficient matching to a commercial single-mode fiber (SMF) with a 3.5-μm MFD. The SSC exhibits a single-facet coupling loss (CL) as low as 0.90 dB (average 1.0 dB) and large alignment tolerances of ±1.1 μm vertically and ±1.45 μm horizontally. When integrated with a 64-GHz EO modulator, the system demonstrates error-free 200-Gbps PAM-4 transmission with a transmitter dispersion eye closure for quaternary modulation (TDECQ) of 2.39 dB, satisfying the IEEE 802.3dj standard. This work provides a practical, reproducible, and process-friendly fiber–chip interface for TFLN platforms lacking access to advanced nanofabrication infrastructure.

2. Device Design and Fabrication

The SSC [region A in Fig. 1(a)] and the TFLN EO modulator are monolithically integrated on an *X*-cut TFLN-on-insulator wafer [Fig. 1(a)], consisting of a 600-nm-thick TFLN device layer, a 2-μm-thick SiO_2 cladding layer, and a 500-μm-thick quartz substrate. This *X*-cut quartz-substrate TFLN wafer was fabricated by NanoLN. The choice of a quartz substrate is driven by the co-design requirement of the high-speed modulator and the fiber–chip interface. Quartz possesses a low relative permittivity ($\varepsilon_r \approx 3.8$), which minimizes microwave leakage and enables better velocity matching between the optical and electrical signals, critical for achieving the demonstrated 64-GHz EO bandwidth and error-free 200-Gbps PAM-4 transmission. In contrast, a high-permittivity silicon substrate ($\varepsilon_r \approx 11.7$) would severely confine the microwave field, increasing RF loss and limiting the modulator's high-frequency response. The quartz substrate thus provides an optimal platform for low-loss optical coupling (via the SSC) and high-bandwidth EO modulation in a monolithic architecture.

The proposed SSC employs a dual-layer inverse taper structure, as illustrated in Figs. 1(b) and 1(c), consisting of a lower TFLN tapered waveguide and an overlying SiO_2 wide-mode waveguide. The coupling process from a lensed fiber to the chip can be described as follows: first, light from a lensed fiber with an MFD of 3.5 μm is efficiently coupled into the SiO_2 waveguide; subsequently, the optical field evanescently couples into the TFLN dual-layer inverse taper and is adiabatically transferred to the final TFLN ridge waveguide.

Figure 1(d) presents the results of a sequential one-dimensional parameter sweep: first, the height of the SiO_2 cladding layer was swept to identify its favorable range; subsequently, this height was fixed, and the mode overlap integral was calculated across varying waveguide widths, thereby revealing the influence of each parameter on coupling performance. Although this approach simplifies the simulation workflow, the results still clearly indicate a strong coupling effect between width and height. The overlap integral exceeds 98% only when both parameters fall within specific ranges. For the TE_0 mode coupled to a fiber with an MFD of 3.5 μm, a peak overlap exceeding 98% is achieved when the SiO_2 waveguide width is 4.7 μm and the height is 3 μm, with a broad high-overlap plateau surrounding this optimum point. However, during downstream dicing and polishing processes, SiO_2 thicknesses exceeding 2 μm are prone to film delamination due to accumulated thermo-mechanical stress[30]. Moreover, increasing the thickness from 2 to 3 μm yields less than a 2% improvement in the overlap integral. Therefore, to significantly enhance process reliability while maintaining high mode-matching efficiency, the upper cladding thickness was conservatively set to 2 μm, slightly below the simulated optimum, while the waveguide width was retained at 4.7 μm.

The dual-layer inverse taper in TFLN is fabricated via a two-step dry etching process. In the first step, inductively coupled plasma reactive ion etching (ICP-RIE) using a $Cl_2/Ar/O_2$ gas mixture etches the TFLN layer uniformly to a depth of

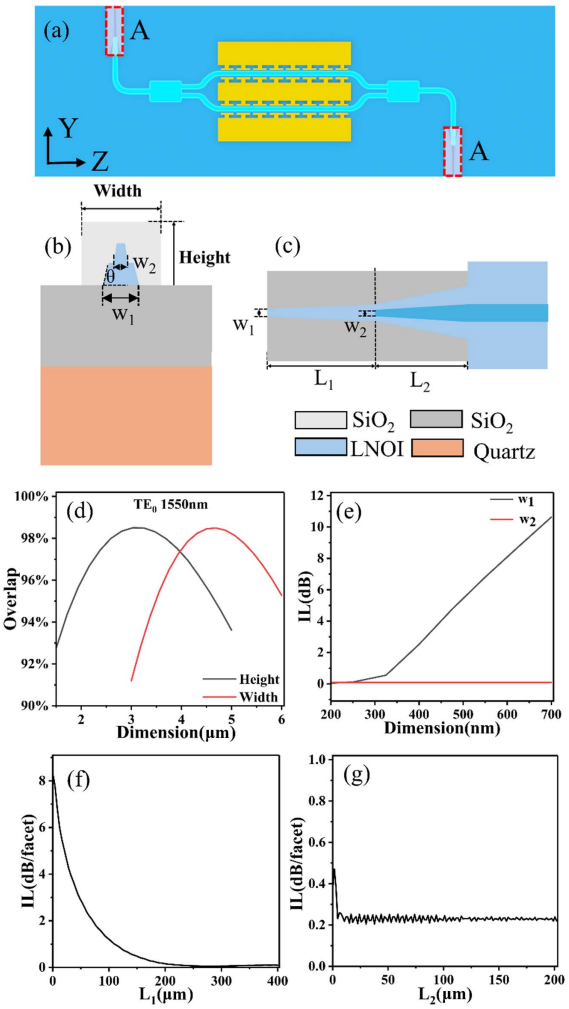

Fig. 1. (a) Schematic layout of the monolithically integrated device. (b) Cross-sectional view of the bilayer SSC structure. (c) Magnified view of the dual-layer inverse taper. (d) Effect of cladding width and thickness on the mode overlap integral with a single-mode fiber having a 3.5-μm MFD. (e) Coupling IL versus w_1 and w_2. (f) Coupling IL versus L_1. (g) Coupling IL versus L_2.

600 nm, forming a 500-μm-long lower taper. This taper comprises a 350-μm front section (L_1) that linearly expands from 400 nm to 1 μm in width, followed by a 150-μm rear section (L_2) that further widens to 3 μm. A second lithography step then defines an upper taper solely within the L_2 region, with its width increasing linearly from 400 nm to 1.2 μm. A subsequent ICP-RIE step etches an additional 300 nm into the TFLN, yielding a dual-layer waveguide in which both the upper and lower segments are 300 nm tall. This geometry supports adiabatic vertical mode evolution and effectively mitigates interfacial scattering, enabling low-loss mode conversion.

All geometric parameters were optimized in Lumerical MODE, with the experimentally measured 75° sidewall angle incorporated as a hard process constraint. The optimization followed a sequential one-variable-at-a-time strategy: with all other parameters fixed, w_1, w_2, L_1, L_2, and the SiO_2 cladding dimensions were independently scanned to identify local optima. The

final parameter set was then combined for a full three-dimensional simulation to validate overall performance.

As shown in Fig. 1(e), reducing the tip width w_1 of the lower taper improves coupling efficiency, as a narrower tip reduces the effective mode area and enhances modal confinement. However, further reduction of w_1 approaches the minimum feature size reliably achievable with our fabrication platform, namely, 248-nm deep ultraviolet (DUV) lithography combined with commercial TFLN dry etching, risking pattern collapse or linewidth control failure. Considering both simulated performance and process robustness, w_1 was ultimately set to 300 nm, a value that has been repeatedly achieved in our experiments without observable structural degradation.

For the upper taper width w_2, simulations indicate that the coupling efficiency varies by less than 0.1 dB over the range of 200–700 nm, demonstrating that this parameter has negligible impact on device performance. Consequently, w_2 of 400 nm was selected based primarily on process reliability and fabrication tolerance: this dimension is significantly larger than the minimum resolvable feature size of our platform, effectively mitigating structural degradation or collapse caused by lithographic misalignment, etch loading effects, or linewidth variations. Thus, 400 nm represents a rational compromise that ensures high device yield and structural integrity while maintaining performance robustness.

The taper lengths were set to L_1 of 350 μm and L_2 of 150 μm, corresponding to the points where coupling efficiency saturates in Figs. 1(f) and 1(g), respectively. This choice maximizes performance while avoiding unnecessary chip area consumption.

A full three-dimensional simulation, based on the final geometric parameters and the measured 75° sidewall profile, predicts a single-facet IL of only 0.37 dB at 1550 nm. Figure 2 shows cross-sectional electric field distributions of the TE_0 mode at three critical locations: Fig. 2(b) the SiO_2 waveguide region, Fig. 2(c) the TFLN dual-layer taper region, and Fig. 2(d) the final TFLN ridge waveguide. These field profiles clearly illustrate the gradual mode compression from a wide mode [Fig. 2(d)] to a narrow mode [Fig. 2(b)], confirming the effective modal control provided by the dual-layer taper. The smooth vertical transition demonstrates that the optical field undergoes adiabatic evolution, enabling efficient coupling to a 3.5-μm-MFD fiber without requiring sub-100-nm fabrication processes.

As shown in Fig. 3, the complete device was fabricated on a 1 cm × 1 cm TFLN chip, with the process flow divided into three key modules: 1) patterning of the TFLN dual-layer taper [Figs. 3(a)–3(t)], 2) definition of the SiO_2 wide-mode waveguide [Figs. 3(u)–3(w)], and 3) fabrication of the modulator electrodes [Figs. 3(x)–3(ac)].

First, a Ni/Au hard mask was deposited on the chip surface, followed by spin-coating of DUV photoresist (AR-P 672.0) and 248-nm DUV lithography to define the inverse taper waveguide pattern. The pattern was then transferred into the TFLN layer via reactive ion etching (RIE) using a $Cl_2/Ar/O_2$ gas mixture. A two-step etching process was employed to form a stepped dual-layer inverse taper: the first etch defined the lower taper to a depth of 600 nm, and the second etch added an upper taper

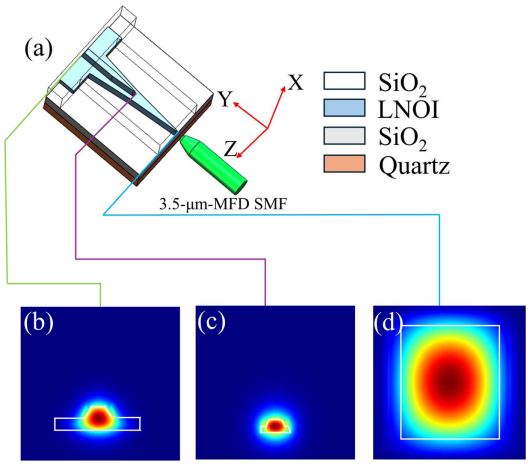

Fig. 2. (a) Schematic 3D view of the mode field converter. (b)–(d) Cross-sectional electric field distributions of the TE_0 mode in different regions of the dual-layer inverted-taper mode field converter.

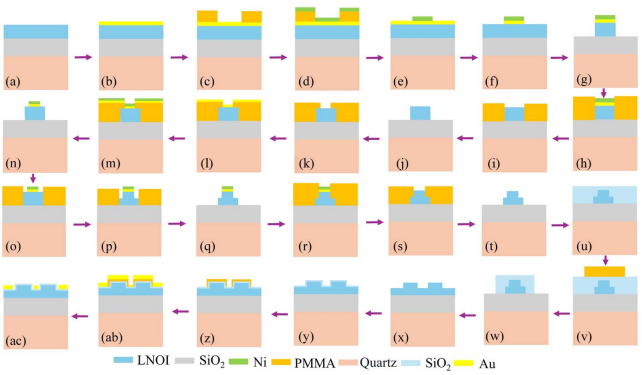

Fig. 3. Fabrication process flow of the monolithically integrated TFLN device. (a)–(ac) Schematics illustrating the 26-step fabrication sequence. Gold-colored regions represent Au: a Ni/Au bilayer is used as the hard mask, while pure Au is employed for the RF electrodes.

by removing an additional 300 nm, resulting in a symmetric transitional structure with a total height of 600 nm comprising two 300-nm-high segments.

Next, a 2-μm-thick SiO_2 upper cladding was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300°C over the SSC region to mitigate thermal stress[30]. DUV lithography and CF_4/O_2 RIE were then used to define the 4.7-μm-wide SiO_2 waveguide. The chip was subsequently annealed at 350°C to relieve residual stress.

Finally, a 350-nm-thick SiO_2 passivation layer was deposited over the modulator region. DUV lithography defined the capacitively loaded traveling-wave electrode (CLTWE) pattern, followed by gold evaporation and lift-off in acetone to form steep, well-defined electrode arrays. The input and output facets were then precision-polished to enable fiber coupling measurements.

The use of a Ni/Au hard mask and dual-step TFLN etching is a pragmatic adaptation to our 248-nm DUV lithography and

Cl_2-based ICP-RIE platform, enabling reliable patterning and a controlled sidewall profile of approximately 75°, which is essential for smooth vertical mode evolution without sub-100-nm features. The resulting waveguides exhibit a propagation loss of 0.28 dB/cm and slight sidewall asymmetry (74.7° versus 73.9°), which are fully consistent with standard DUV-processed TFLN platforms and comparable to advanced electron-beam lithography (EBL)-based results[31]. Crucially, this process supports error-free 200-Gbps PAM-4 transmission, confirming that such minor morphological variations do not impair system-level performance. While Ni/Au provides robust etch resistance in this work, future efforts will explore lower-cost alternatives such as Cr, Ti, or SiO_2 to enhance cost-effectiveness without compromising optical quality.

3. Experimental Results and Discussion

The fiber–chip coupling performance was characterized using a commercial SMF customized by CXFIBER, which has an MFD of 3.5 μm at 1550 nm [Fig. 4(a)]. Coupling tests were performed using a tunable C-band laser (Conquer KG-TLS), a polarization controller, and a self-developed high-precision alignment platform (positioning accuracy ±20 nm) to inject the TE_0 mode into the device. All devices were characterized under identical conditions.

The micro-ring resonator was probed through a grating coupler to enable rapid, non-destructive extraction of its intrinsic propagation loss, without requiring facet polishing, following the method described in Ref. [32]. In contrast, all performance metrics of the main device, including CL, alignment tolerance, and high-speed transmission, are exclusively based on edge coupling through the lithography-friendly SSC reported herein.

To accurately extract the facet CL of the SSC, two types of reference structures were fabricated on the same 1 cm × 1 cm chip as the main modulator: micro-ring resonators for measuring intrinsic propagation loss, and straight waveguides with identical SSCs at both ends [Fig. 4(e)]. The micro-ring resonator yielded a propagation loss of 0.28 dB/cm at 1550 nm [Fig. 5(d)]. The total on-chip IL of the straight waveguide ranged from 1.18 to 1.51 dB across the C-band. After subtracting the propagation loss of 0.42 dB over the corresponding length of 1.5 cm, the single-facet CL was obtained. As shown in Fig. 4(b), the single-facet CL of three independently fabricated devices ranged from 0.90 to 1.09 dB, with an average of approximately 1.0 dB, demonstrating good device uniformity and process repeatability. This result confirms effective mode matching between the SSC output and the 3.5-μm-MFD commercial SMF. Under a 1-dB excess IL allowance, the lateral alignment tolerances reached ±1.1 μm in the X direction and ±1.45 μm in the Y direction [gray curves in Figs. 4(c) and 4(d)], in excellent agreement with simulations based on the actual etched morphology (red curves).

The measured single-facet CL (0.90–1.09 dB) is higher than the simulated value of 0.37 dB, primarily due to several practical factors. First, residual roughness from mechanical facet polishing, with a typical RMS of approximately 2 to 5 nm, introduces additional scattering loss at the chip edge. Second, the actual MFD of the commercial SMF, nominally 3.5 μm, deviates slightly from the ideal Gaussian profile used in simulation, reducing mode overlap. Notably, the variation in loss across three independently fabricated chips is only ±0.1 dB, indicating good process control and confirming that the measured loss level is representative of standard photolithography-compatible TFLN platforms.

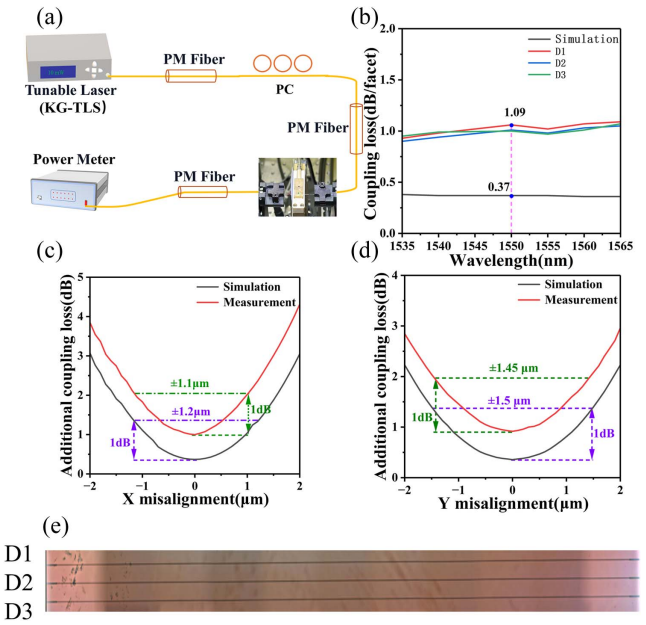

Fig. 4. Fiber–chip coupling characterization. (a) Test setup schematic. (b) Measured single-facet CL versus wavelength for three independently fabricated devices, showing an average loss of 1.0 dB at 1550 nm. (c), (d) Lateral alignment tolerance in X and Y directions (±1.1 μm and ±1.45 μm at 1-dB excess loss). (e) Reference straight waveguide with identical SSCs at both ends.

Notably, the design with w_1 of 300 nm and θ of 75° [Fig. 5(b)] exhibits smooth and gradual mode expansion, highly similar to that of the conventional sub-100-nm structure with θ of 85° [Fig. 5(a)]. This indicates that, despite significantly relaxing the minimum feature size requirement, coupling performance comparable to sub-100-nm designs is still achievable. More importantly, this design is fully compatible with the naturally formed 75° sidewall profile of standard dry etching, enabling low-loss, large-tolerance fiber–chip coupling without high-precision lithography. Cross-sectional SEM images confirm θ of 74.7° and 73.9°, in close agreement with the 75° model used in simulations [Fig. 5(c)], further validating the alignment between design and fabrication.

Table 1 summarizes a performance comparison between this work and representative coupling schemes reported in recent literature. Although sub-100-nm electron-beam lithography (EBL)-based SSCs achieve lower IL (0.5–0.54 dB/facet), they rely on high-resolution direct-write techniques and typically require lensed fibers or suspended waveguide structures, making them incompatible with wafer-scale batch fabrication. In contrast,

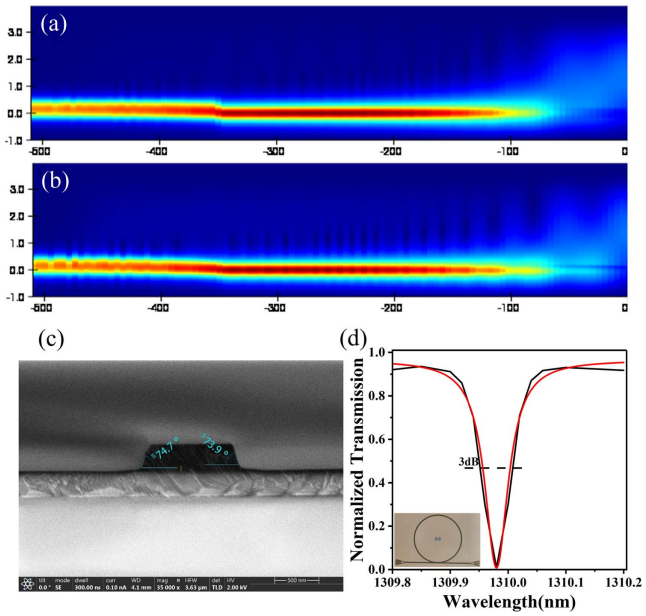

Fig. 5. (a) Optical mode evolution process in conventional sub-100-nm structures with 85° sidewalls. (b) Optical mode evolution in sub-300-nm structures with 75° sidewalls. (c) SEM image characterizing the θ of the TFLN waveguide. (d) Transmission spectrum of a micro-ring resonator.

our approach leverages 248-nm DUV lithography and standard dry etching processes, enabling direct coupling to commercial single-mode fibers with a 3.5-μm MFD without any additional post-processing or special structures. It also offers alignment tolerances of ±1.1 μm (vertical) and ±1.45 μm (lateral). Although the single-facet loss is approximately 1 dB, about 0.4–0.5 dB higher than EBL-based schemes, the present design exhibits clear advantages in process compatibility, fabrication yield, and packaging simplicity, making it more suitable for practical applications such as data-center interconnects and quantum photonic systems.

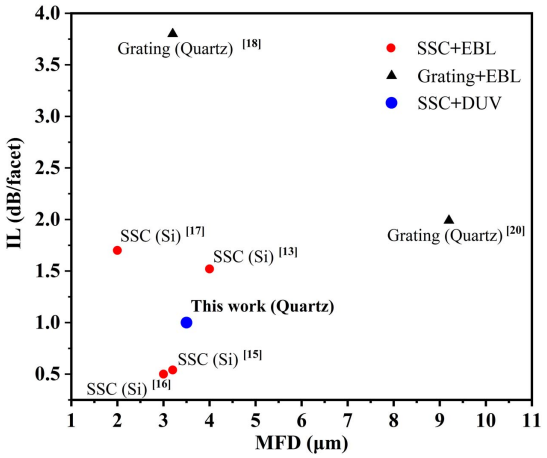

Fig. 6. Comprehensive performance comparison of IL versus mode field diameter: revealing the superior trade-off of this work with simplified fabrication.

To visually illustrate the trade-off between performance and fabrication complexity, Fig. 6 plots the IL versus MFD for representative coupling schemes, with marker size indicating the minimum required feature size. Smaller markers correspond to greater reliance on EBL and higher manufacturing difficulty. The proposed approach (blue circle) resides in the quadrant characterized by high MFD, low loss, and large feature size, highlighting an excellent balance between optical performance and compatibility with standard DUV lithography. This result underscores a key insight for practical TFLN photonic integration: minimizing IL alone is insufficient; instead, coupling efficiency, alignment tolerance, and compatibility with manufacturable DUV processes must be co-optimized. This co-design philosophy constitutes the core contribution of the work.

To verify the SSC's compatibility in high-speed systems, it was monolithically integrated with a mature 64-GHz Mach–Zehnder

Table 1. Comparison of Coupling Schemes.

Coupling scheme	Substrate	SMF MFD (μm)	Loss (dB/facet)	w_1/w_2 (nm)	Tolerance (μm)	Lithography type
SSC[16]	Si	3	0.5	120 150	/	EBL
SSC[15]	Si	3.2	0.54	260 150	*X*: ±1.2 *Y*: ±1.1	EBL
SSC[17]	Si	2	1.7	340 30	*X*&*Y*: 1	EBL
SSC[13]	Si	4	1.52	100 100	*X*&*Y*: 1	EBL
Grating[18]	Quartz	3.2	3.8	/	/	EBL
Grating[20]	Quartz	9.2	1.99	/	/	EBL
This work	**Quartz**	**3.5**	**1.0**	**300** **400**	*X*: **±1.1** *Y*: **±1.45**	**DUV**

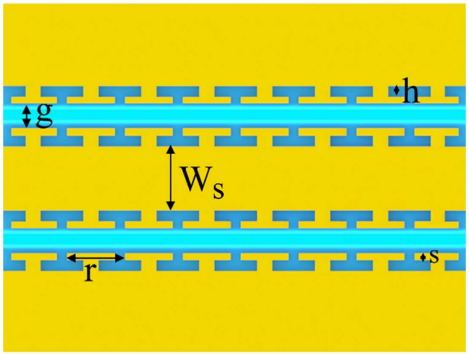

Fig. 7. Schematic of the 64-GHz Mach–Zehnder modulator with CLTWEs.

EO modulator fabricated using standard TFLN processes. The modulator employs a mature CLTWE structure (Fig. 7), with W_s of 80 μm, h of 2 μm, s of 1 μm, g of 3 μm, and r of 50 μm. Its 3-dB EO bandwidth was measured as 64 GHz [Fig. 8(b)] using a vector network analyzer (Keysight N5227B) and a high-speed photodetector (XPDV3120) [Fig. 8(a)], which is sufficient for 200-Gbps PAM-4 transmission according to the IEEE 802.3df standard.

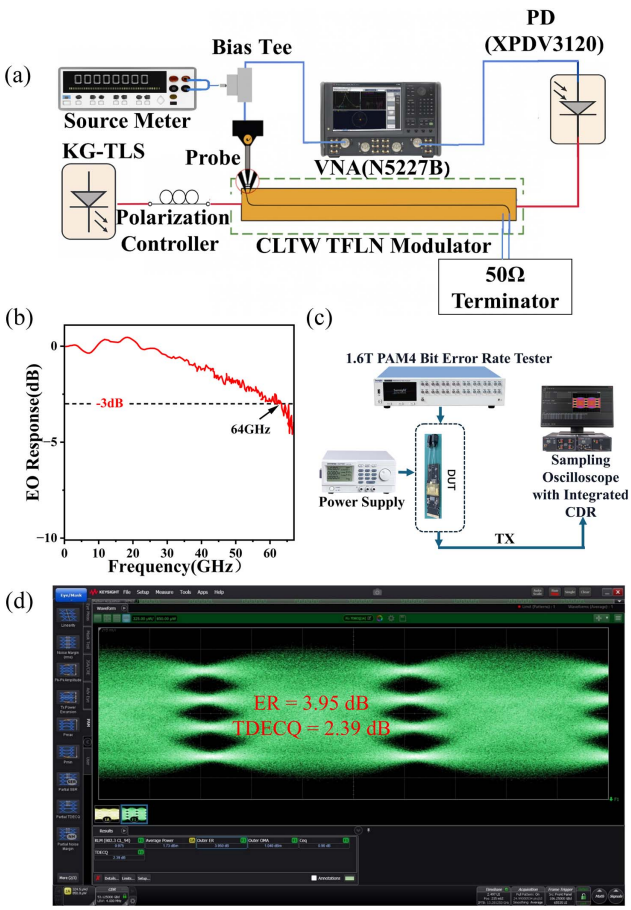

Fig. 8. (a) Schematic of the EO bandwidth measurement setup. (b) Measured EO response with 3-dB bandwidth of 64 GHz. (c) Schematic of the 200-Gbps PAM-4 system-level test setup. (d) Measured eye diagram of the transmitted signal (TDECQ = 2.39 dB).

A 200-Gbps PAM-4 transmission experiment was conducted as shown in Fig. 8(c). The transmitter employed feed-forward equalization and decision-feedback equalization (FFE/DFE), while the receiver included clock and data recovery, continuous-time linear equalization (CDR/CTLE), and FFE. The measured transmitted eye diagram [Fig. 8(d)] shows a TDECQ of 2.39 dB and an extinction ratio (ER) of 3.95 dB. This TDECQ value is below the 2.5-dB limit specified in IEEE P802.3dj for 200-Gbps PAM-4 links, indicating that the pre-forward error correction (FEC) bit error ratio is below the KP4-FEC threshold of 3.8×10^{-3} and no error floor is observed. Thus, the result satisfies the IEEE 802.3 series standard requirement for 200-Gbps optical links and confirms that the SSC introduces no significant signal integrity degradation.

4. Conclusion

In conclusion, a low-loss edge-coupled SSC for TFLN photonics has been developed with a 300-nm lithographic feature size, fully compatible with standard dry etching processes. The device achieves a 3.5-μm MFD, exhibiting a fiber-to-chip single-facet CL as low as 0.90 dB (average 1.0 dB) and lateral alignment tolerances of ±1.1 μm and ±1.45 μm in the X and Y directions, respectively. Monolithic integration with a mature in-house 64-GHz EO modulator enables 200-Gbps PAM-4 transmission, confirming its practicality in high-speed optical interconnects. The proposed SSC is fully compatible with standard photolithography and can be readily integrated with other TFLN components (e.g., modulators, filters) on quartz or silicon platforms, enabling scalable photonic circuits for datacom and quantum applications. This work provides a practical, reproducible, and process-friendly fiber-to-chip coupling solution for TFLN platforms lacking advanced nanofabrication capabilities. The large alignment tolerance (±1.1/± 1.45 μm) and low CL of the demonstrated SSC also make it well suited for future fiber array (FA) packaging, where input and output fibers could be co-located on a single chip facet to simplify assembly. Such system-level integration is beyond the scope of this work, which focuses on the lithography-compatible SSC as a foundational building block.

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