

Fabrication-constrained inverse design and demonstration of high-performance grating couplers

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A high-performance grating coupler (GC) operating at a wavelength of 1550 nm is proposed by utilizing the adjoint-based inverse design algorithm on a 220 nm silicon-on-insulator (SOI) substrate. The grating scheme offers several advantages, including simple structure, large minimum feature size (MFS), manufacturing friendliness, support for large-scale production and multi-project wafer (MPW) runs, etc., while simultaneously maintaining exceptional coupling performance and fabrication tolerance. The design process incorporates various fabrication constraints to satisfy the specifications of different foundry processes. The optimized GC demonstrates excellent coupling performance and 3 dB bandwidth within the MFS range of 60 to 180 nm. The simulated coupling efficiency (CE) of the GC with 130 nm MFS is -1.69 dB, whereas the experimentally measured CE of the fabricated GC using electron beam lithography (EBL) is -2.83 dB. Notably, the experimental CE of the GC with 180 nm MFS fabricated using 248 nm deep ultraviolet (DUV) lithography is -2.77 dB, representing the highest experimental CE ever reported for a single-layer etching C-Band GC supported by MPW runs fabricated on 220 nm SOI without utilizing any back reflector, multi-etch layer, or overlay. The manufacturing outcomes of the same GC structure employing different manufacturing processes are discussed and analyzed, providing valuable insights for the fabrication of silicon photonics devices.

Keywords: grating coupler; inverse design; minimum feature size; fabrication process.

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1. Introduction

Silicon photonics has emerged as a promising solution for various application fields due to its high-density integration, low fabrication costs, and power consumption, as well as its compatibility with the standard complementary metal-oxide semiconductor (CMOS) platform. However, one of the major challenges faced by silicon photonic chips is effectively connecting light emitted by single-mode fibers (SMFs) to these photonic circuits. To tackle this issue, two commonly used solutions are in-plane edge coupling and off-plane grating coupling methods^[1]. Grating couplers (GCs) offer a compelling alternative to edge couplers due to their avoidance of intricate post-fabrication procedures^[2] and their ability to be flexibly positioned on the chip for seamless wafer-level automated testing. However, uniform grating couplers (UGCs) exhibit a narrow bandwidth and relatively low coupling efficiency (CE), which can be attributed to

limited grating directionality and a mode mismatch between the SMF mode profile and the radiated mode profile.

In order to enhance the directionality of the guided mode and minimize power leakage to the substrate, various proposals have been put forward in the literature. These include incorporating poly-silicon overlayers^[3-5], utilizing multilayer etching structures^[6-10], increasing the thickness of the Si waveguide layer^[6,11,12], employing binary blazed grating couplers (BBGCs)^[13,14], and embedding distributed Bragg reflectors (DBRs)^[15] or metallic mirrors^[16-19] within the substrate. However, the majority of these methods necessitate the introduction of supplementary manufacturing steps or materials, leading to heightened manufacturing intricacy and tape-out costs while diminishing tape-out yields.

Another important factor limiting the CE of the GC is the mode mismatch between the diffraction light field distribution and the mode distribution of the fiber. By employing apodized

GC structures^[11,12,19-25], it is possible to effectively enhance the mode profile overlap with the Gaussian-like mode distribution in the fiber by carefully engineering each scattering unit's coupling strength. Additionally, this approach helps reduce back reflection at the waveguide grating interface, thereby improving overall CE, whereas the minimum feature size (MFS) of most apodization schemes often falls below 100 nm, which typically exceeds the manufacturing constraints imposed by common deep ultraviolet (DUV) lithography employed in commercial silicon photonic foundries. Consequently, most apodization schemes typically rely on electron beam lithography (EBL) for defining the grating pattern and are incompatible with high-volume industrial drive applications.

To address the challenges posed by intricate manufacturing processes and small MFSs in existing GC schemes documented in the literature, a high-performance single-layer etching GC operating at C band on 220 nm silicon-on-insulator (SOI) was meticulously designed utilizing an inverse design methodology. Subsequently, comprehensive experimental and characterizations were conducted. The proposed structure comprehensively explores the parameter space of the GC, optimizing the groove width and spacing of each scattering unit through a gradient descent algorithm to maximize mode overlap area and minimize back reflection. This design exhibits a straightforward manufacturing process with large MFS while maintaining exceptional coupling performance suitable for multi-project wafer (MPW) runs. To ensure compatibility with mainstream foundry processes, including Advanced Micro Foundry (AMF) 100 nm technology, Interuniversity Microelectronics Centre (IMEC) 130 nm technology, and Institute of Microelectronics of Chinese Academy of Sciences (IMECAS) 180 nm technology, we have incorporated MFSs ranging from 60 to 180 nm into the GC optimization process, aligning with the manufacturing constraints of EBL, 193 nm DUV, and 248 nm DUV lithography. Within the MFS range of 60 to 180 nm, for EBL-fabricated optimized GCs operating at approximately 1550 nm, simulation results demonstrate an insertion loss ranging from -1.55 to -2.29 dB, while experimental results exhibit a range of -2.70 to 3.72 dB, with a 3 dB bandwidth spanning from 70 to 67 nm. Notably, the experimental insertion loss for the GC with 130 nm MFS is measured at -2.83 dB, showcasing the unparalleled coupling performance of the single-layer etched GC on 220 nm SOI substrate thus far without any additional processes. Furthermore, within the ± 20 nm range of grating groove width variable, the insertion loss fluctuates by less than 0.5 dB, indicating excellent manufacturing tolerance and robustness. Additionally, the proposed GC with 180 nm MFS, fabricated using 248 nm DUV lithography, demonstrates exceptional coupling insertion loss of -2.77 dB and a 72 nm 3 dB bandwidth.

2. Design and Simulation

The majority of GCs proposed in the literature are generally designed by population-based metaheuristic intuition-based optimization methodologies, such as genetic algorithms and

particle swarm optimization algorithms, which rely on several limited parameter sweeps (etching depth of grooves, grating period, duty factor, cladding thickness, and buried oxide thickness) and random perturbations. The limited design freedom presents a constraint on the exploration of an extensive design space, thereby necessitating an increase in the number of optimized parameters to enable the comprehensive exploration of design space and ultimately enhance the GC's CE. Considering that the adjoint-based inverse design algorithm^[25] can effectively tackle the limitations of optimization methods based on physical intuition and requires only one forward simulation to calculate fields and one backward simulation to calculate gradients, irrespective of their number, significant reductions in computational resource consumption and simulation time can be achieved.

Therefore, we employ the adjoint-based inverse design method to optimize GC. The optimization process is divided into two stages: continuous and discrete states. During the continuous stage, the geometry structure of GC is parameterized to facilitate a seamless variation in permittivity distribution between the cladding and the grating. Subsequently, we use the second-order limited-memory Broyden–Fletcher–Goldfarb–Shanno algorithm (L-BFGS)^[26] for iterative until convergence. The discrete stage then transforms the optimized structure from the continuous stage into an initial structure for further discretization.

As illustrated in non-proportional Fig. 1, when parameterizing the geometric boundary of the GC, we define the optimization parameters as the widths of each groove (g_n) and each tooth (t_n), with the objective of increasing the degrees of freedom. The optimization parameter vector $x = (t_0, g_1, t_1, g_2, t_2, \dots, g_n, t_n)$ is specifically set, with the first spacing t_0 defined relative to a prescribed fixed point along the horizontal axis. The CE corresponding to the center wavelength of 1550 nm was subsequently defined as the figure of merit. The optimization problem can be formulated as^[25]

$$\begin{aligned} & \text{minimize}_{x, E_1, E_2, \dots, E_m} \sum_{i=1}^m [1 - \eta_i(E_i)]^2, \\ & \text{subject to } \nabla \times \mu_0^{-1} \nabla \times E_i - w_i^2 \epsilon(x) E_i = -i w_i J_i, \\ & i = 1, 2, \dots, m, \end{aligned} \quad (1)$$

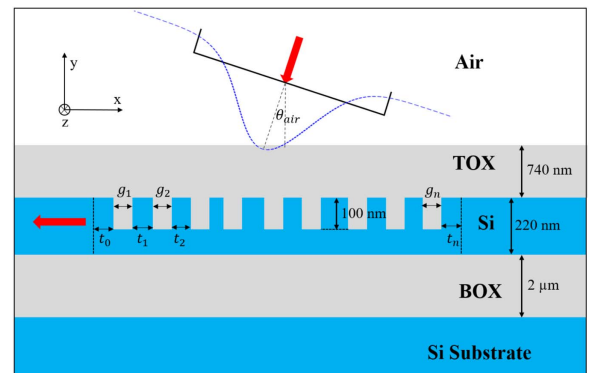


Fig. 1. Schematic diagram of optimized GC. TOX, top oxide; BOX, bottom oxide.

where m represents the number of input modes, E_i denotes the electric field that satisfies Maxwell's equations in the frequency domain at frequencies ω_i , J_i refers to the equivalent current density distribution, x is a vector parameterizing the structure, μ_0 stands for the magnetic permeability of free space, $\epsilon(x)$ represents the electric permittivity, and η_i corresponds to the objective function, which can be defined as either equal to the CE from a Gaussian beam into the fundamental waveguide mode.

The 2D finite-difference time-domain (FDTD) solver is adopted to analyze the Maxwell equation during the simulation process. The optimized GC structure is depicted in Fig. 1, where the Gaussian beam source represents the transverse electric (TE) mode of SMF-28 with a mode field diameter (MFD) of 10.4 μm . It is positioned 1 μm above the top oxide (TOX) layer and inclined at an angle of 14.5° relative to the normal direction ($\theta_{\text{air}} = 14.5^\circ$). As previously mentioned, the optimization parameters encompass all groove widths and spacings within the grating structure. Assuming a 25-period GC, there are 50 corresponding optimization parameters that need to be solved using the L-BFGS algorithm until either the change in figure of merit is less than 10^{-5} or 300 iterations have been completed.

Due to the inherent highly non-convex and difficult-to-navigate nature of the discretization parameter space, it is often challenging for gradient descent to converge toward the globally optimal position of GC's spatial parameters. To mitigate the risk of being trapped in local optima, selecting an appropriate initial condition before commencing the optimization process becomes crucial. Therefore, we adopt an apodized GC configuration as an initial condition for iteratively optimizing CE. This approach not only retains the advantages associated with the simple structure of an apodized GC but also overcomes fabrication limitations imposed by its small MFS. Subsequently, numerical simulations were performed to investigate the etching depth and thickness of the initial apodized GC with the MFS of 30 nm. It was determined that the optimal etching depth for the initial condition was 100 nm, while the optimal thickness of the TOX layer was found to be 740 nm, as illustrated in Fig. 2. At this point, the GC structure reached maximum directionality by realizing constructive interference for upward diffracted light and destructive interference for downward diffracted light.

The manufacturing constraint condition is incorporated as a penalty function in the GC optimization process to increase the MFS, resulting in the following formulation of the figure of merit:

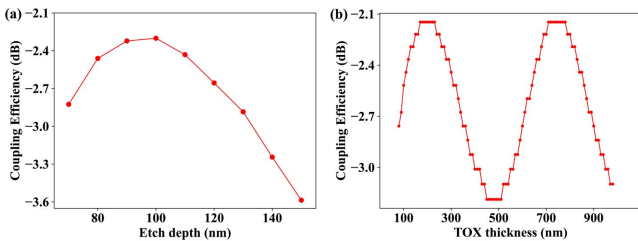


Fig. 2. The simulated CE as a function of (a) etch depth; (b) TOX thickness.

$$\eta_i = \max_x [\eta_i(E_i) - p(x)], \quad (2)$$

where x is a vector parameterizing the GC structure and $p(x)$ is a function representing the design parameters of the penalty applied when the MFS exceeds the specified value. After imposing boundary constraints on the optimization parameters, the optimization parameters are updated iteratively by a certain step in the opposite direction of the gradient until convergence is achieved at the global optimal value of the objective function. At this point, we obtain a solution for GC geometric structure parameters that exhibit maximum CE and satisfy specific feature size constraints. Considering the compatibility with various foundry processes, we have designed five sets of GCs featuring sizes ranging from 60 to 180 nm. The transmission spectrum is illustrated in Fig. 3. The MFS of the initial GC structure prior to optimization measured 30 nm, while the CE was recorded as -2.15 dB. The CEs of the optimized GCs, with MFSs of 60, 100, 130, 160, and 180 nm at a wavelength of 1550 nm, are -1.55, -1.63, -1.69, -2.02, and -2.29 dB, respectively, while the 3 dB bandwidth ranges from 68 to 60 nm. To the best of our knowledge, the CE achieved by the proposed GC with the MFS of 130 nm is currently unparalleled among reported MPW-compatible GCs on 220 nm SOI, without requiring any additional processes such as back reflectors, multi-etch layers, and overlay layers.

Furthermore, it is evident that the CE of GC gradually diminishes with increasing MFS; however, the minimum value remains higher than that of a UGC with a CE of -2.6 dB. This phenomenon arises due to the enforced expansion of the minimum groove width, which disrupts the coupling strength distribution profile conforming to the Gaussian beam. Consequently, there is a reduction in the overlap area between the radiated mode profile and the SMF Gaussian-like mode profile, leading to a decrease in CE. The electric field distribution of the GC with 130 nm MFS is illustrated in Fig. 4. A majority of the optical power is efficiently coupled into the waveguide from the optical fiber at a tilt angle of 14.5° relative to the normal direction. Additionally, only a minority of light leaks into the high refractive index silicon substrate, thereby confirming the high directionality achieved through optimization. The adjoint-based

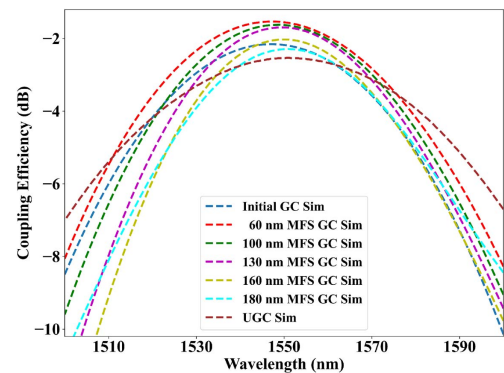


Fig. 3. Simulated transmission spectra of UGC and optimized GCs with various fabrication constraints.

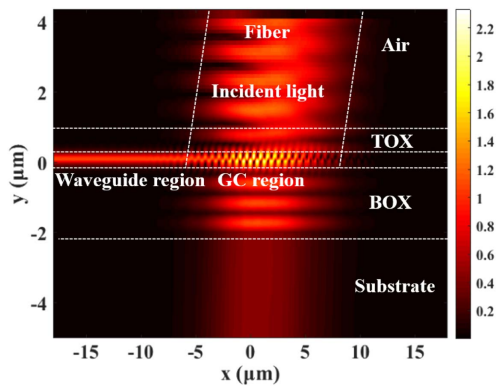


Fig. 4. Electric field distribution of the optimized GC.

optimization process for each target GC typically necessitates approximately 150 iterations of L-BFGS-B, with a total computation time of around 80 core minutes on a 3.7 GHz AMD Ryzen 5 5600X 6-Core Processor.

3. Fabrication and Measurement

Based on the simulation structure, we utilized the EBL system (Vistec EBPG 5200) available at the Center for Advanced Electronic Materials and Devices (AEMD) of Shanghai Jiao Tong University to fabricate optimized GCs with MFSs of 60, 100, 130, 160, and 180 nm as well as UGCs. Additionally, for comparison with the EBL processing results, we employed the MPW service offered by the IMECAS 180 nm CMOS process platform to manufacture the same GC structure with 180 nm MFS on a 220 nm SOI substrate. The test structure comprises an input GC and an output GC. By employing a 350 μm long taper, the 12 μm by 15 μm GC is seamlessly connected to a 450 nm by 100 μm waveguide. To assess the impact of fabrication errors on GC performance optimization, we employed the process design kit (PDK) tool developed by AEMD to design and fabricate GCs with varying MFSs. The widths of the grating grooves were adjusted within a range of ± 20 nm at 10 nm intervals.

In the process of fabricating GCs utilizing EBL, the SOI wafer was initially cleaned using a wet process and oxygen plasma treatment (PVA TePla Plasms System). A 200-nm-thick electron-beam resist of AR-P 6200.09 used as the etching mask was spin-coated on the surface of the top silicon layer, followed by 2 min of curing on a 150°C hot-plate. Subsequently, the resist was exposed by the EBL (Vistec EBPG 5200) system with an acceleration voltage of 100 kV. When the exposed photoresist was developed, a dry etching in inductively coupled plasma reactive ion etching (PE-100) system was employed to transfer the grating pattern with 100 nm etch depth to the device layer of the SOI sample (SPTS DRIE-I) and the resist was wet-stripped, followed by the oxygen plasma cleaning. This entire process was repeated for a second time to achieve full etching for transferring waveguide and taper patterns. Finally, a protective TOX layer with a thickness of 740 nm was deposited using

plasma-enhanced chemical vapor deposition (Oxford PECVD) technology.

The fabrication inaccuracies were characterized by performing scanning electron microscope (SEM) system (Zeiss Ultra Plus) measurements on GCs fabricated by EBL with different MFSs, as depicted in Fig. 5 (130 nm MFS). The pale white mottled spots in the figure represent the remnants resulting from HF solution corrosion of the silica cladding. The actual processing width of the GC groove deviates from the design width by a few nanometers, potentially attributed to the excessive exposure or proximity effect^[27] of EBL. Additionally, the figure reveals the presence of certain irregularities and roughness on both the surface and side wall of the GC teeth, which will result in variations in the diffraction angle of the light beam passing through the GC, thereby impacting its coupling performance. Furthermore, considering the micro-loading effect^[28], it is observed that exposed areas with smaller line widths experience slower etching speeds, leading to a failure in achieving the expected etching depth for narrow grooves in the proposed GC.

The actual groove depth of several sets of GCs fabricated by EBL with different MFSs was measured using an atomic force microscope (AFM) system (Bruker ICON). The 3D morphology and the etching depth of the GC with 100 nm MFS are presented in Figs. 6(a)–6(d), respectively. The etching depth of the GC structure is approximately 104 nm, which agrees well with design values. The 3D topography reveals that the surface and

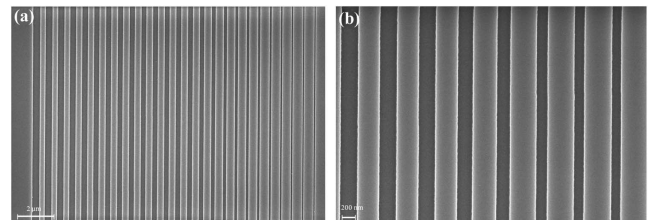


Fig. 5. (a) Top view and (b) partial enlarged drawing of an SEM micrograph of an optimized GC fabricated by EBL.

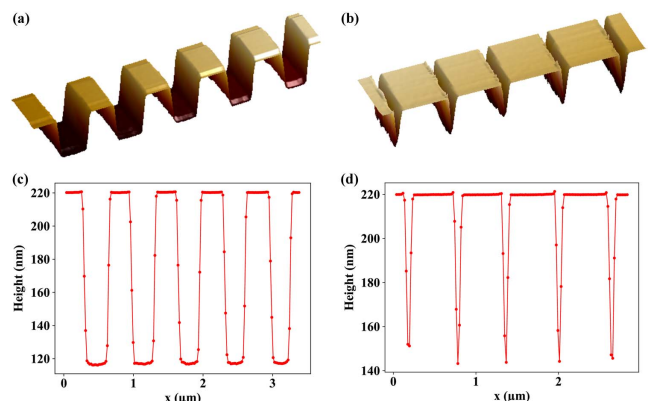


Fig. 6. 3D morphologies and etch depths at the (a), (c) widest and (b), (d) narrowest grooves of the EBL-fabricated GC.

side wall of the grating teeth exhibit deviations from perfect flatness, thereby compromising the constructive interference of upward diffracted light between adjacent scattering units and diminishing CE. This phenomenon arises due to inherent characteristics of the dry etching process, which further corroborates the findings from SEM characterization. Moreover, the narrowest groove width in the grating surpasses the measurement capabilities of the AFM probe to accurately determine its actual depth at that specific location, thereby resulting in the sharp corner pattern depicted in Fig. 6(d).

The experimental measurement was conducted on an optical probe station. The optical source utilized in the experiment was a tunable continuous-wave (CW) source, with tunability ranging from 1510 to 1600 nm at 5 pm intervals. A power meter (Keysight 81989 A) was employed to measure the output optical power collected from the test structures. The polarization controller was used for selecting the TE polarization light mode. Input and output fibers were prepared by stripping and cleaving SMF-28 patch fibers, positioned at an incidence angle of 14.5° on both input and output couplers. As shown in Fig. 7, we present experimentally measured transmission spectra of the optimized GCs with MFSs of 60, 100, 130, 160, and 180 nm.

Comparing the measured spectrum with the simulated results, we observe a good agreement between the measured CEs and their simulated counterparts, while maintaining a central wavelength close to 1550 nm. The measured CEs of optimized GCs fabricated by EBL with MFSs of 60, 100, 130, 160, and 180 nm are -2.70, -2.89, -2.83, -3.31, and -3.72 dB, respectively. The 3 dB bandwidth of the corresponding GC changes from 70 to 67 nm. Notably, the experimental CE of the optimized GC with a 130 nm MFS achieves the highest reported value in the literature for single-layer etching GCs supporting MPW tape-out on 220 nm SOI substrate, without requiring any additional complex processes such as multilayer etching, multilayer deposition, or embedded reflectors. The simulation and experimental results of the optimized GC clearly demonstrate a consistent trend: as the MFS increases, there is a gradual decrease in the CE of GC. However, despite an increase in the MFS to 160 and 180 nm, the optimized GC still demonstrates reduced CEs of -3.31 and -3.72 dB, respectively.

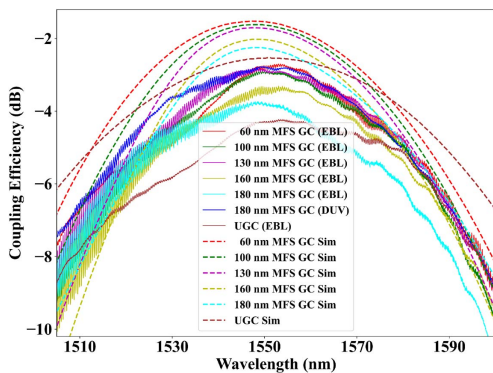


Fig. 7. Simulation and experimental transmission spectra of optimized GCs with various MFSs.

Nevertheless, these values remain significantly superior to those achieved by the UGC (-4.43 dB), highlighting the exceptional coupling performance of our proposed GC while maintaining a commendable 3 dB bandwidth. The discrepancy between the experimental and simulation values of insertion loss primarily arises from manufacturing imprecisions, encompassing the roughness of the grating surface and groove sidewall, slight deviations in etching depth from the design specifications, and inadequate etching depth in narrow grooves, as well as non-uniform deposition of the TOX layer.

In addition, we fabricated the optimized a GC with a 180 nm MFS using 248 nm DUV lithography via the IMECAS MPW service. After measuring 25 chips, we obtained a maximum CE of -2.77 dB, an average CE of -3.2 dB, and an average 3 dB bandwidth of 72 nm. It is evident that the DUV fabrication results outperform those obtained through EBL fabrication, showcasing a reduction in insertion loss by 0.95 dB. The results convincingly demonstrate the superior processing capabilities of DUV lithography over EBL. In the EBL system, the electron beam light source is utilized, leading to forward scattering^[27] of electrons in photoresist and consequent broadening of the beam. Additionally, strong backward scattering^[27] of electrons in both photoresist and Si layers results in inadequate exposure of certain adjacent areas and excessive exposure of others, ultimately causing significant distortion in the exposure pattern. Consequently, DUV lithography exhibits reduced line edge roughness, enhanced linewidth uniformity, and higher manufacturing accuracy when compared to EBL.

To investigate the impact of fabrication inaccuracies on device performance, we employed EBL to fabricate the optimized GC with a constant MFS while systematically varying the groove width within a range of ±20 nm. As illustrated in Fig. 8, when the groove width variable Δ varies from -20 to 20 nm, the GC's CE with a fixed MFS varies within the range of 0.5 dB, and the central wavelength is blue-shifted, showing exceptional fabrication tolerance and robustness. The optimal coupling

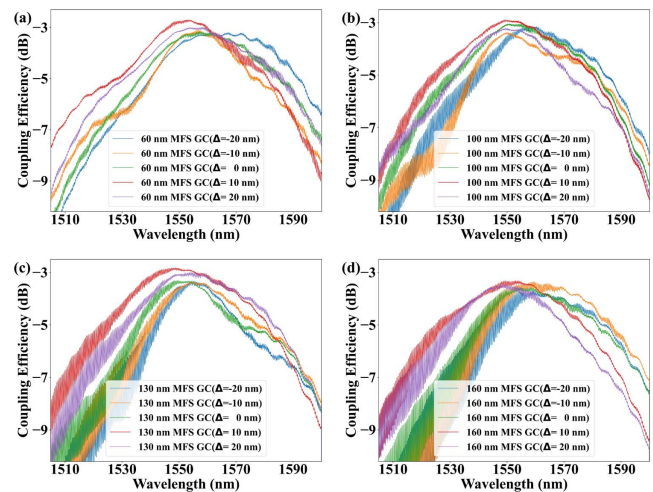


Fig. 8. Measured transmission spectra of optimized GCs with [a] 60, [b] 100, [c] 130, [d] 160 nm MFSs at various groove width variables.

performance is attained when the GC grooves deviate from the design value by +10 nm, potentially attributed to manufacturing errors and process instability. Simultaneously, we observe a gradual increase in the amplitude of the proposed GC's parasitic oscillation ripple with an increase in MFS, attributed to the existence of the Fabry–Pérot cavity and back reflection phenomena. Expanding the width of the narrowest slot in GC leads to a deflection of the coupling strength profile distribution from its optimal value, resulting in a reduction in the overlap area between the radiated mode and fiber mode, as well as an increase in back reflection. The influence of this effect is further amplified by variations in grating slot width due to manufacturing errors, causing an amplification in oscillation ripple amplitude induced by the Fabry–Pérot cavity with an increasing MFS of optimized GC. However, upon comparing the DUV and EBL manufacturing results of GCs with 180 nm MFSs in Fig. 7, it is evident that the GC with identical structure produced by DUV exhibits a smaller amplitude of Fabry–Pérot ripple. As previously mentioned, the superior linewidth uniformity and roughness of DUV in comparison to EBL contribute to a reduction in exposure distortion area, thereby minimizing manufacturing errors associated with DUV. This reduction also significantly decreases back reflection, resulting in a substantial decrease in oscillation Fabry–Pérot amplitude and enhancing the device's robustness and fabrication tolerance.

The comparison of figures of merit between previous literatures and our work is summarized in Table 1. It is evident that

most GC optimization strategies mentioned in the literature either employ multi-layer intricate structures or single-layer etching schemes such as BBGCs and apodized GCs. However, the adoption of a multi-layer complex structure leads to increased manufacturing difficulty, higher tape-out cost, reduced chip yield, and decreased robustness despite improving CE. On the other hand, the sub-wavelength structure of BBGC and the meticulously engineered coupling strength distribution profile of apodized GC typically necessitate MFSs smaller than 100 nm, which fail to meet the resolution requirements of DUV lithography and hinder industrial-scale mass production. Contrarily, from a practical manufacturing perspective, our designed single-layer etching GC overcomes the limitations of the aforementioned approaches. It not only achieves superior coupling performance and manufacturing tolerance but also exhibits a larger MFS and enhanced manufacturing flexibility to meet the resolution requirements of 193 nm DUV and 248 nm DUV while supporting MPW tape-out, thereby significantly reducing production costs. Most importantly, our optimized GC's manufacturing process is exceptionally straightforward and fully compatible with CMOS technology without necessitating additional overlay, deposition, or metal layer processes; solely requiring a single-layer etching in the grating area. This significantly streamlines the manufacturing process, reduces complexity and costs, and enhances the robustness and yield. In summary, the comparative literature results in Table 1 demonstrate that our proposed optimized GC not only

Table 1. Summary of the Simulated (Sim) and Experimental (Exp) CEs for Different GCs Reported in the Literatures.

Ref.	SOI (nm)	Structure	Band	MFS (nm)	Sim CE (dB)	Exp CE (dB)	Process
[10]	220	Multilayer etching	C	200	-2.4	-4.2	248 nm DUV
[13]	220	BBGC	C	74	-2.2	-4.1	EBL
[14]	220	BBGC	C	57	-1.78	-3.69	EBL
[20]	220	Apodization	C	30	-2.15	—	—
[11]	220	Apodization	C	100	-1.9	—	—
[23]	220	Apodization	C	180	-2.6	-3.1	248 nm DUV
[12]	220	Apodization	C	60	-1.6	—	—
[25]	220	Apodization	C	100	-1.94	—	—
[29]	220	Apodization	C	50	-2.13	—	—
This work	220	Improved apodization	C	60	-1.55	-2.70	EBL
				100	-1.63	-2.89	
				130	-1.69	-2.83	
				160	-2.02	-3.31	
				180	-2.29	-3.72	
				180	-2.29	-2.77	248 nm DUV

offers a simplified fabrication process and supports MPW runs but also exhibits excellent coupling performance of -2.77 dB. This represents the best experimental outcome for a single-layer etching grating manufactured on 220 nm SOI using DUV lithography without any intricate procedures.

Furthermore, the majority of single-layer etching schemes for the apodized GC proposed in existing literature have not been experimentally validated due to limitations in the MFS. In addition to employing EBL for the optimized GC experiment, we also utilized EBL and 248 nm DUV lithography techniques to fabricate the proposed GC with a 180 nm MFS, followed by subsequent testing and analysis of experimental results. The disparity in microstructure morphology and fabrication precision between EBL and DUV processes, as previously discussed, contribute significantly to the substantial variations observed between the experimental and simulation performance of GCs processed by EBL, in addition to the inherent manufacturing error associated with EBL. By fully embracing DUV lithography for fabricating optimized GCs with MFSs exceeding 100 nm, a notable enhancement in CE and fabrication tolerance can be achieved compared to the current outcomes.

4. Conclusion

A high-performance, large MFS, and structurally simple single-layer etching GC is presented in this paper. The GC employs an inverse design method, incorporating MFSs ranging from 60 to 180 nm into the optimization process to meet the manufacturing requirements of various foundry processes. The design and fabrication of the GC is carried out on 220 nm SOI substrate. The proposed GC demonstrates exceptional coupling performance and robustness within the MFS range of 60 to 180 nm. The simulation and experimental results indicate CEs of -1.69 and -2.83 dB, respectively, for the 130 nm MFS optimized GC fabricated by EBL. The CE value of the optimized GC with a 180 nm MFS, fabricated using 248 nm DUV lithography, is measured to be -2.77 dB. To the best of our knowledge, this represents the highest reported experimental coupling achieved for a single-layer etched GC fabricated on 220 nm SOI that supports MPW runs without any additional process steps to date. If the GC is fabricated using a DUV lithography process, it will exhibit even superior coupling performance. In summary, our proposed GC scheme demonstrates exceptional characteristics, encompassing superior coupling performance, high fabrication tolerance and robustness, straightforward structure and manufacturing process, and compatibility with mainstream foundry processes, as well as support for MPW runs and industrial-driven mass production. The analysis and discussion of the experimental results for the same GC structure fabricated using EBL and DUV, respectively, also reveal the performance and differences of these distinct manufacturing processes. This holds immense significance in comprehending the intricate characteristics associated with diverse manufacturing techniques while offering invaluable guidance to silicon photonic device designers when selecting the appropriate manufacturing process.

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