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Fabrication and photo-response of monolithic 90° hybrid-photodetector array chip for QPSK detection

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A quadrature phase-shift keying (QPSK) coherent photodetector chip consisting of a 4×4 multimode interference 90° optical hybrid and a four-channel evanescent photodetector array is designed and fabricated with its photo-response in the L-band characterized. The metal organic chemical vapor deposition regrowth method is adopted to realize active–passive monolithic integration. The chip exhibits a low dark current below 100 nA for each photodetector in the array, a low excess loss of 0.85 dB, a common mode ratio rejection better than 13.6 dB, and a phase deviation within ±10° over the 40 nm wavelength span.

Keywords: hybrid; photodetectors; monolithic integration; photo-response.

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1. Introduction

Encouraged by the high-speed data transmission demand of the developing 5G and the upcoming 6G optical communication systems, a big surge in the aggregate data transfer rate in optical networks will be expected in the near future. The coherent optical transmission technology, nowadays standard in the long-haul fiber-optic networks, will be further ameliorated into shorter distance applications such as metropolitan areas, access networks, or even data centers[1,2]. Enabled by the high-order (de)modulation formats scheme targeting both amplitude and phase of the optical carrier, it could conveniently expand data bitrate by-fold without remarkable increase in optic module speed[3]. One of the most popular and widely used formats is quadrature phase-shift keying (QPSK). It utilizes four quadrature phase states to encode 2 bit information into one symbol and doubles the transmission rate accordingly with a higher receiver sensitivity as well. Early researches on transmission link performance and signal processing methods have proven the effectiveness and feasibility of the format[4–6].

On the other hand, higher port density and pluggable optical modules in such networks require miniaturization of optical components for less power consumption and optical coupling loss, where integrated devices and modules are obviously a better choice than assembled ones. Many monolithic coherent transceivers have been reported for C-band applications, with low excess loss of 1 dB[7], high responsivity of 70 mA/W[8], and high channel speed[9]. Other novel types of hybrids have also been proposed for compact size and wide operation wavelength ranges[10,11]. We have also recently designed and fabricated an InP-based 90° hybrid for QPSK at the C-band[12] with comparable phase and common mode rejection ratio (CMRR) characteristics.

In this Letter, a four-channel evanescent photodetector (PD) array is further monolithically integrated to the 90° hybrid with its operation wavelength range adjusted to the wider L-band. The chip is fabricated by the metal organic chemical vapor deposition (MOCVD) regrowth technology, and its photo-response is characterized. The monolithic chip shows a CMRR better than 13.6 dB, a phase deviation within ±10°, and a small excess loss of 0.85 dB over a 40 nm range in the L-band. The PD array also exhibits a low dark current level below 100 nA at −3 V.

2. Device Design

The monolithic chip consists of a 90° hybrid based on the 4×4 general multimode interference (MMI) structure, an array of four evanescent PDs, and a Mach–Zehnder (MZ) 1×2 MMI power splitter. A typical sandwich deep-ridge waveguide structure is adopted for both the hybrid and the power splitter, with an InP bottom cladding layer of 2.5 μm, an InGaAsP (Q1.065)

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Table 1. Parameters of the 90° Hybrid.

Input/Output waveguide width	2.0 μm
Waveguide separation	5.0 μm
Taper end width	3.6 μm
Taper length	50 μm
MMI region length	810 μm
MMI region width	20 μm

core layer of 0.5 μm, and an InP top cladding layer of 1.5 μm. The hybrid parameters are summarized in Table 1.

A taper of linearly varied width is inserted between each input/output waveguide and the MMI region for less phase deviation sensitivity on the MMI region width. The MMI region length is estimated by the self-imaging principle for the four-fold general imaging situation[13]:

$$L_{\mathrm{MMI}} = \frac{n_{\mathrm{eff}} W_{\mathrm{eff}}^2}{\lambda_0}, \tag{1}$$

where n_{eff} denotes the effective refractive index of the MMI region; W_{eff} denotes the effective waveguide width, which could be approximated by the actual deep-ridge MMI region width W_{MMI}; λ_0 denotes the vacuum center wavelength of the input light. For the L-band center wavelength of 1595 nm, n_{eff} is calculated to be 3.194 for an MMI width of 20 μm. Considering a possible fabrication error, W_{MMI} may vary in the range of 20 μm to 20.3 μm, and the estimated MMI region length then ranges from 800.93 μm to 825.21 μm.

The PD structure layers are designed to be regrown on the MMI core layer to collect optical power by evanescent field coupling to the absorption layer. Details are listed in Table 2. The active area of each PD is 90 μm^2.

An MZ 1 × 2 MMI power splitter is also integrated on chip for phase measurement using only one necessary input source. It first splits the input optical beam into two arms with ideally equal intensity using a 1 × 2 MMI of symmetrical interference

Table 2. Parameters of the Evanescent Photodetector.

Material Composition	Doping Type and Density [cm^{-3}]	Thickness [nm]
$In_{0.53}Ga_{0.47}As$	P, 1×10^{18}	50
InP	P, 2×10^{17}	300
InGaAsP (graded)	P, 1×10^{16}	40
$In_{0.53}Ga_{0.47}As$ (absorption layer)	N, 1×10^{16}	560
InGaAsP (graded)	N, 2×10^{17}	40
InGaAsP (Q1.065)	N, 3×10^{18}	500

Table 3. Parameters of the 1 × 2 Splitter.

MMI region length	95 μm
MMI region width	10 μm
Delay line radius	550 μm
Delay line length difference	172.24 μm

type[14] and then provokes an additional phase difference in one arm by an additional bending delay line relative to a straight one. The two outputs are directly connected to the second and fourth input channels of the hybrid. Parameters of the splitter are listed in Table 3, with the input/output waveguide and taper sizes identical to the hybrid (Table 1).

3. Chip Fabrication

Fabrication of the monolithic chip starts with waveguide layers growth by MOCVD. Then, the top cladding layer in the PD region is removed by chemical etching using hydrochloric and phosphoric acid solutions. The patterned substrate then undergoes a second MOCVD for whole area PD layers growth. Figure 1 illustrates the epitaxial layer structure after regrowth. The PD layers cover the whole hybrid and splitter regions over the top cladding layer, the coupling region with gradually thinning cladding layer, and the core layer at the PD region. Two inductively coupled plasma (ICP) etching steps are conducted successively to define first the p-i-n junction mesa and then the N-contact mesa. The N-contact mesa front edge has extended 8 μm before the junction mesa into the coupling region to prevent high optical coupling loss as previously demonstrated[15]. PD layers elsewhere are redundant and etched out completely in the process. Metallization of contacts are realized by lifting off the Au/Ge/Ni alloy film for the N type and chemically etching the Ti/Au film for the P type, followed by a rapid 1 min

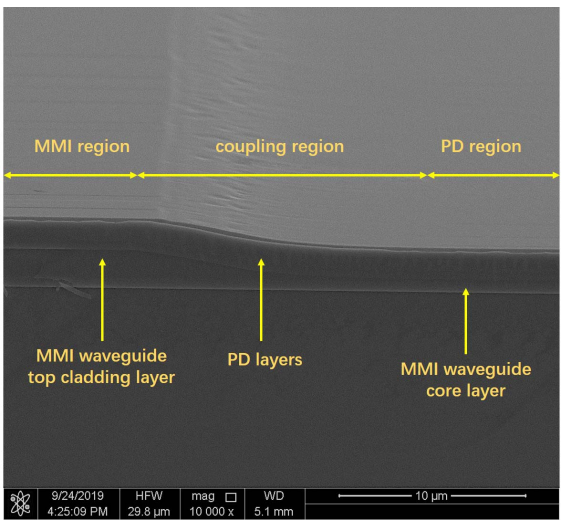

Fig. 1. Cross-section SEM image of epitaxial layers after regrowth.

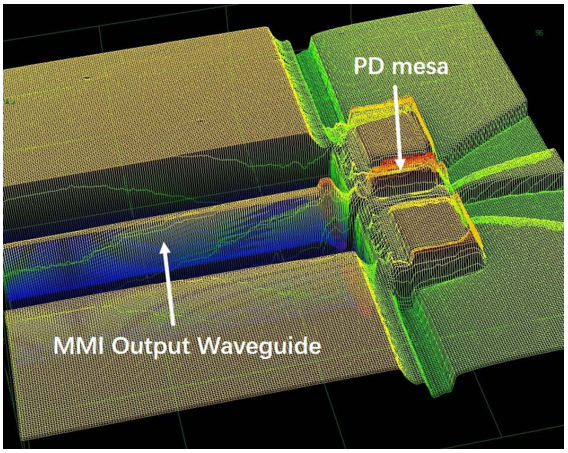

Fig. 2. PD jointed to the hybrid waveguide 3D image.

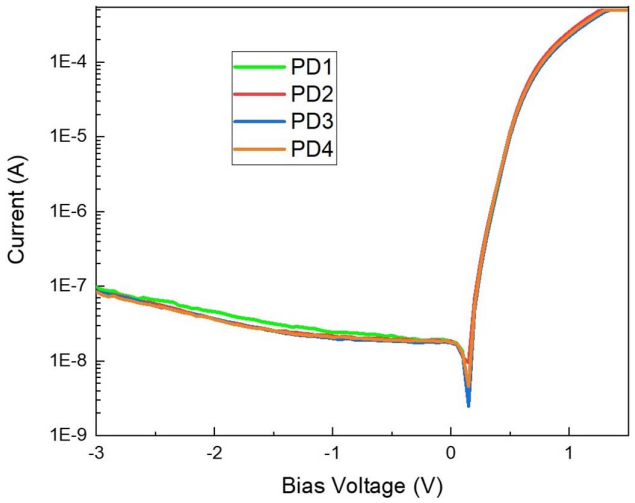

Fig. 4. Dark current of the PD array.

thermal annealing at 410°C. A thick 700 nm SiO_2 layer has been deposited by the plasma enhanced chemical vapor method before metallization to passivate the PD. After metallization, the hybrid and splitter are deeply etched simultaneously in the same run, during which the PD region is also protected by an extra SiO_2 film. Finally, the chip is cleaved at the splitter input waveguide and ready for measurement. Photos of the fabricated chip are shown in Figs. 2 and 3, and the chip has a total size of 5.15 mm × 1.28 mm, in which the splitter length is 2.77 mm.

4. Result Discussion

Measurement of the monolithic chip is conducted on a high-precision test platform using a tunable laser at TE polarization. The dark current of the each PD in the array is measured to be uniformly lower than 100 nA at −3 V and 30 nA at −1 V, as shown in Fig. 4. The dark current density of the regrown PD is on the same level as our previous monolithic de-multiplexer and PD array chip, where the PDs were grown in the first MOCVD process prior to waveguides[16], which indicates a good regrowth quality in this work. The external PD responsivities of each channel and the total responsivity, which reflects the chip's photo-electronic conversion efficiency, are measured to the single mode fiber output at the hybrid input and depicted in Fig. 5. The curves present a similar stable tendency with wavelength and remain flat over the whole L-band. However, a responsivity difference could be observed among the channels, which might come from imperfect imaging and unequal optical loss in hybrid output waveguides caused by stain spots on the paths to the PD array during fabrication, as observed in Fig. 3.

The CMRR represents this imbalance of responsivity and is defined by

$$\mathrm{CMRR}_{\mathrm{I/Q}} = -20\log\left(\left|\frac{I_{1/2} - I_{4/3}}{I_{1/2} + I_{4/3}}\right|\right), \tag{2}$$

where I_1, I_4 are used for the I channel and I_2, I_3 for the Q channel. The measured result is drawn in Fig. 6. Both inputs show a CMRR 5 dB higher for the Q channels than for the I channels due to the responsivity imbalance, but, still, all channels present a CMRR over 13.6 dB in the range of 1585–1625 nm.

The excess loss of the monolithic chip is estimated. Apart from the 6 dB intrinsic loss of an ideal four-fold imaging for each hybrid input, an excess loss also exists to represent an extra loss of on-chip passive components compared to a straight waveguide, which contains optical scattering loss from but not limited to the imperfect imaging, the waveguide bending, or other kinds of waveguide shapes and sizes. A waveguide-integrated PD (WG-PD) is fabricated on the same wafer, by the same

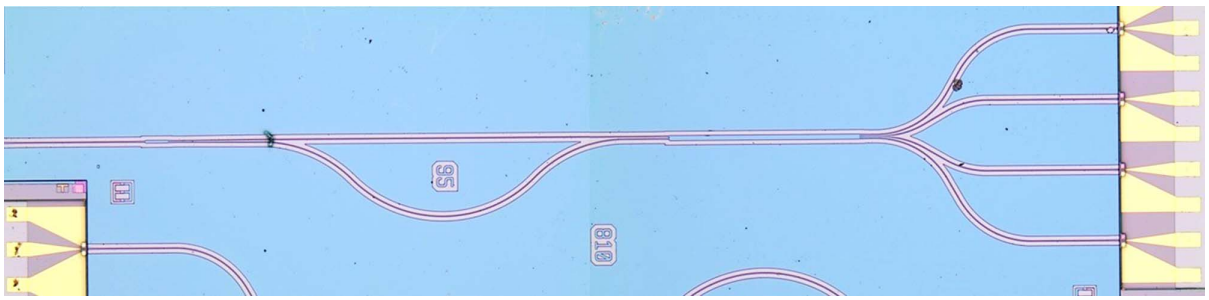

Fig. 3. Microscope photo of the fabricated monolithic chip.

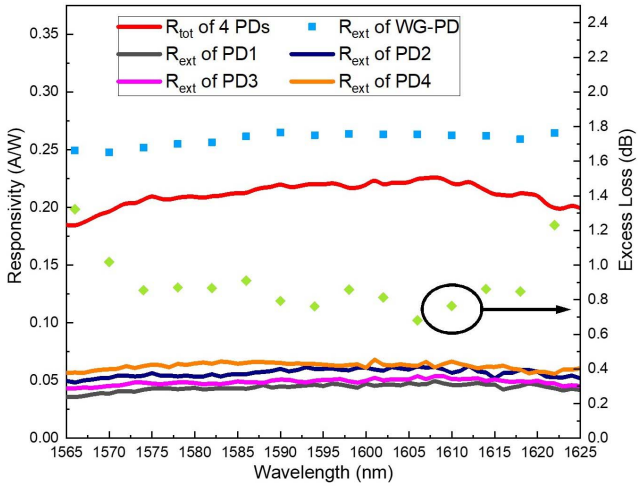

Fig. 5. Responsivities and excess loss of the monolithic chip.

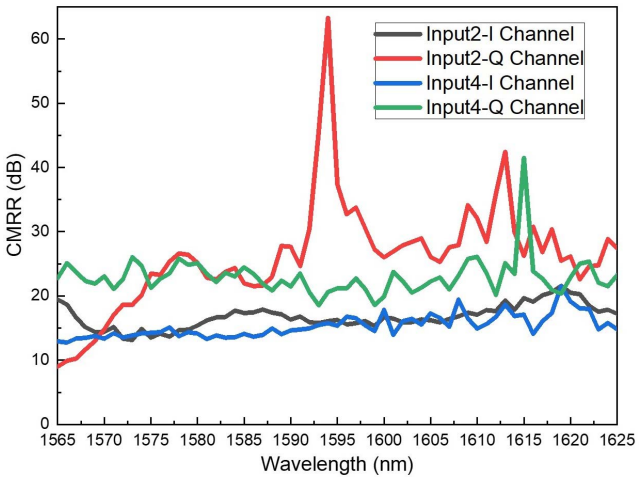

Fig. 6. CMRR of the monolithic chip.

method, in the same process for this estimation. The waveguide length is the same as the total length of the hybrid and the splitter. By deducting the WG-PD external responsivity (blue square in Fig. 5) from the total responsivity (red line in Fig. 5) of the monolithic chip, losses from the fiber end coupling could be eliminated. Consequently, a small excess loss of 0.85 dB is obtained (green diamond in Fig. 5) for almost the entire L-band. We believe that the bending loss of the designed extreme slim 2 μm waveguide and the scattering of the rough MMI sidewall are the main sources of this loss.

The phase deviation of the monolithic chip could be deduced from the spectral response measurement result with the integrated 1×2 splitter, which is shown in Fig. 7. Periodic-like response enhancements and destructions could be observed for each PD. The spectral distance between neighboring peaks or valleys is defined as the free spectrum range (FSR) and is determined by the delay line length difference ΔL:

$$\mathrm{FSR} \cong \frac{\lambda_0^2}{n_{\mathrm{eff}}^{'} \Delta L}, \tag{3}$$

where $n_{\mathrm{eff}}^{'}$ represents the effective refractive index of the single mode waveguide (3.174 at 1.595 μm). The FSR for all four channels ranges from 4.1 nm to 4.6 nm, corresponding well with the designed value of 4.65 nm.

Phase distance between channels is calculated by the peak or valley distance in the spectrum:

$$\Delta\Phi_{ij} = \frac{f_{p/v-i} - f_{p/v-j}}{\mathrm{FSR}} \cdot (2\pi), \qquad i = 1, 2, 3, 4; \quad j = 1, 2, 3, 4; \quad i \neq j, \tag{4}$$

where f denotes the frequency at the response peak or valley as the footprints p and v indicate, with i and j for different output

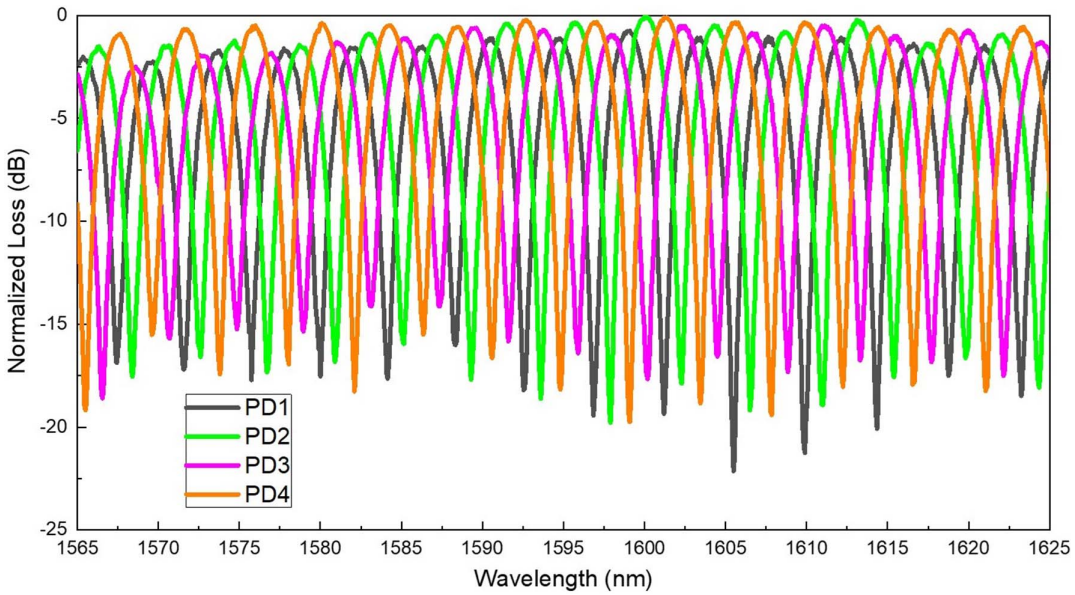

Fig. 7. Spectral response of the monolithic chip integrated with the splitter.

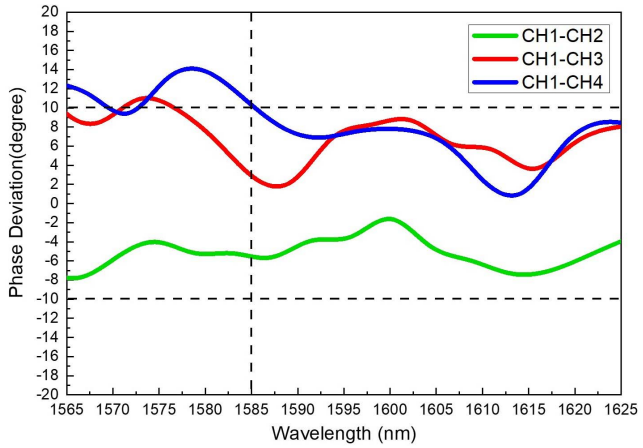

Fig. 8. Phase deviation of the monolithic chip.

channels. Since the standard phase distances for a 4×4 MMI hybrid are $\Delta\Phi_{12} = \pi/2$, $\Delta\Phi_{13} = -\pi/2$, $\Delta\Phi_{14} = \pi$, respectively, the calculated phase distance results are further compared to these standard values so that phase deviations are deduced. The estimated phase deviation result is shown in Fig. 8. All channels exhibit a stable deviation over the whole L-band and sustain it well within ±10° over 40 nm from 1585 nm to 1625 nm. Results beyond the L-band are unavailable due to equipment limit. The measured deviation is a little larger than the ±5° state-of-the-art level.

Measurement results include both fabrication and measurement errors. For one thing, the inaccurate graphic transfer process may lead to waveguide size distortion, in which width variation is the primary contributor to the larger phase deviation. Supplementary simulations are conducted for phase deviation and excess loss of the hybrid and power splitter, with a 300 nm width increase for waveguides considered. Simulation results by the finite-difference-time-domain propagation method show a phase deviation larger than 5° near 1585 nm in Fig. 9 and an excess loss decreasing from 0.8 dB to 0.05 dB in Fig. 10 for the hybrid at the 40 nm span mentioned above. The 1×2 MMI,

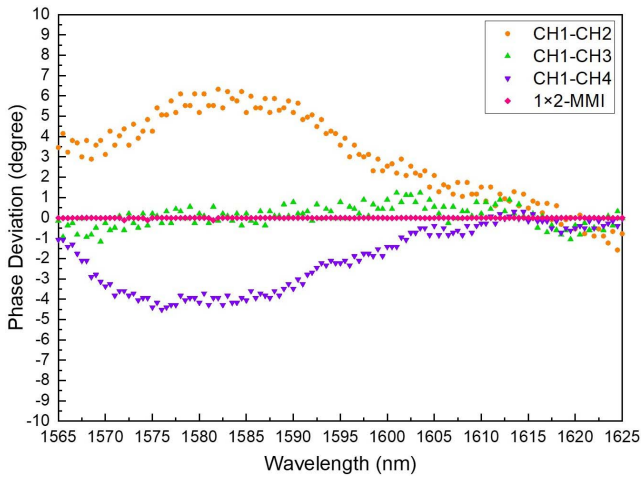

Fig. 9. Simulated phase deviation with fabrication error.

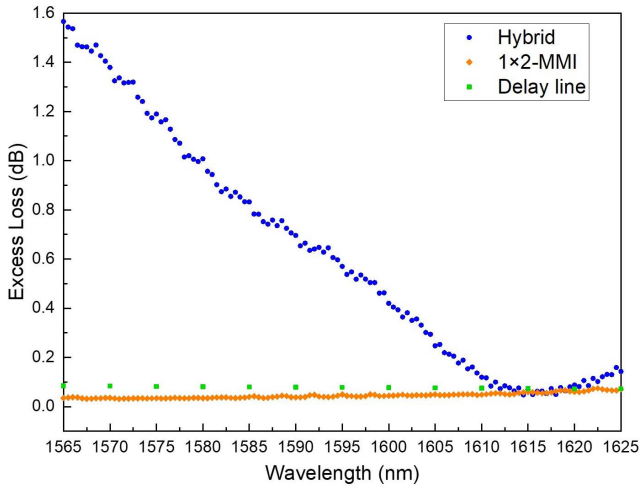

Fig. 10. Simulated excess loss with fabrication error.

however, induces almost no extra phase deviation due to its intrinsic power splitter characteristic, with a stably low excess loss below 0.2 dB for the whole L-band, which contains both losses from the 1×2 MMI and the delay line. Difference between the measured 0.85 dB excess loss and the simulated result should originate from the actual waveguide side wall scattering of optical power in the MMI region.

For the other thing, measurement errors will result in an overestimated phase deviation as well, since the phase distance between channels is deduced from peak/valley wavelengths in the spectral response curves. Therefore, any discrepancy of the test laser wavelength will lead to extra calculated phase deviations, which might come from limited equipment accuracy. In this work, ±30 pm wavelength repeatability is defined for our laser diode, which corresponds to a possible induced phase deviation increment from 2.35° to 2.63°.

Provided that the more delicate e-beam lithography and a finer tunable laser for chip fabrication and measurement are to be adopted, a better phase deviation controlled into ±5° could be expected.

5. Conclusion

A 90° hybrid monolithic with a PD array is fabricated and characterized in the L-band. The evanescent four-PDs array is monolithically integrated by MOCVD regrowth technology to ensure an intact waveguide epitaxial structure for the passive hybrid, hence a small excess loss of 0.85 dB. Still, the PD array shows a similar dark current density similar to the one without regrowth and a uniform dark current lower than 100 nA at −3 V. The monolithic chip also exhibits a stable performance over a wide 40 nm wavelength range from 1585 nm to 1625 nm, with a CMRR higher than 13.6 dB and a phase deviation within ±10°, which could be further decreased by an improved fabrication method and measurement condition.

The bandwidth of the PD array reaches 15 GHz for each PD unit, which is yet to be promoted for high-speed detection.

The primary cause is the relatively low density of 10^{17} cm^{-3} P-type-doped InP electron barrier layer, which generates a large bandgap difference at the absorber boundary to prevent holes from efficient collection by the P contact. An obvious improvement could be expected, as long as a higher dopant density over 10^{18} cm^{-3} and narrower bandgap InGaAsP material is adopted in the MOCVD process[17].

Despite all that, the integration method in this work still proves feasible for a coherent PD chip, which could conveniently include more passive structures like the MZ splitter. The chip integrated with the MZ splitter could potentially constitute together as the core module in the differential QPSK (DQPSK) receiver, where the delay line is 1 bit long in time to realize self-homodyne photo-detection with no need for local oscillators. Furthermore, the DQPSK receiver could also possibly convert DQPSK signals to 4-ary pulse amplitude modulation (PAM4) ones and hopefully cut down power consumption[18]. Higher level integration of the basic chip structure in this work could be expected to realize more multiplexing dimensions, larger channel number, and higher information transmission rate.

Acknowledgement

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