Direct phase control method for binary phase-shift keying space coherent laser communication

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An optical phase locking method based on direct phase control is proposed. The core of this method is to synchronize the carrier by directly changing the phase of the local beam. The corresponding experimental device and the supporting algorithm were configured to verify the feasibility of this method. Phase locking can be completed without cycle skipping, and the acquisition time is 530 ns. Without an optical preamplifier, a sensitivity of -34.4 dBm is obtained, and the bit error rate is 10^{-9} for 2.5 Gbit/s binary phase-shift keying modulation. The measured standard deviation of the phase error is 5.2805°.

Keywords: space coherent laser communication; direct phase control; optical phase-locked loop; IQ modulation. **DOI:** 10.3788/COL202220.060601

1. Introduction

Space laser communication has unique advantages: large bandwidth, license-free spectrum, high data rate, easy and quick deployability, less power, and low requirements^[1]. With the verification of many experiments, optical free-space communication will become an indispensable part of wide-area free-space data networks in the future^[2]. Since 2002, in various application scenarios, such as low Earth orbit (LEO)-ground, LEO-LEO, LEO-geostationary orbit (GEO), GEO-ground, and Moonground, all of these space laser communication tests have been successfully demonstrated^[3–9].

Compared with the direct detection receiver, the most significant advantage of coherent reception is the improvement in sensitivity owing to the amplification of the local oscillator light^[10]. In 2006, Lange *et al.* established a free-space optical link on homodyne binary phase-shift keying (BPSK) with a data rate of 5.625 Gbit/s between two Canary Islands, La Palma and Teneriffe^[11]. In 2008, the German Terra synthetic aperture radar X-band wavelength (SAR-X) satellite and the American near field infrared experiment (NFIRE) satellite built a coherent laser communication with a data rate of 5.6 Gbit/s, and the bit error rate (BER) was better than 10^{-9} . In 2016, a 5.12 Gbit/s coherent communication terminal developed by the Shanghai Institute of Optics and Fine Mechanics was launched with the Mozi quantum satellite, and a satellite ground laser communication link was established^[12].

Digital coherent reception requires analog-to-digital converters (ADCs) with a sampling rate greater than or equal to twice the communication rate, which is challenging for ADCs and digital signal processing (DSP)^[13]. With an increase in the communication rate, the power consumption of digital coherent demodulation continues to increase^[14]. However, space coherent laser communication requires low power consumption and simpler methods. In 2005, Herzog et al. proposed a real-world dither loop receiver, and the achieved sensitivity amounted to 36 photons/bit^[15]. In 2015, Liu et al. proposed a coherent communication scheme based on the channel-switching method, where neither an optical phase-locked loop (OPLL) nor highspeed ADCs are required^[16]. However, the scheme can only demodulate BPSK signals. In 2018, Zhang et al. proposed a differential phase-shift keying heterodyne coherent detection with local oscillation enhancement^[17]. In 2020, Xuan et al. proposed an integrated coherent optical receiver with feed-forward carrier recovery and achieved a BER better than 10⁻⁶ for BPSK at 10 Gbit/s^[18]. In 2020, Lu et al. proposed a digital-analog hybrid OPLL system based on undersampling^[19]. In the above cases, the methods of Liu et al. and Zhang et al. can only demodulate signals of a certain modulation format. The methods of Xuan et al. and Lu et al. require special electrical or optical filters. Although the most common second-order OPLL can demodulate various phase-modulated signals, the realization of phase locking depends on the phase-frequency-phase conversion.

In this Letter, the direct phase control phase locking method based on in-phase and quadrature (IQ) modulation is presented, and the corresponding experimental scheme and matching phase-locked algorithm verify its feasibility. The direct phase control method can be used not only for space communications, but also as a complementary solution for outdoor fiber optic networks and indoor data center applications^[20-25]. This scheme is suitable for M-ary phase-shift keying (MPSK) by adjusting the relevant digital processing in the field-programmable gate array (FPGA). The influence of the MPSK signal communication term is eliminated by the *M*th power operation. When calculating the actual difference, the value obtained after the Mth power calculation should continue to be divided by M. An IQ modulator was used as an external modulation device to directly increase or reduce the phase of the local oscillator light. According to the calculated phase difference, the method directly compensates the corresponding phase of the local oscillator light and avoids the phase-frequency-phase conversion. It achieves a direct closed loop from phase to phase. The performance of the BPSK homodyne coherent receiver based on this method has been examined

2. Theoretical Model

Figure 1 shows the structure of the BPSK homodyne coherent receiver based on the direct phase control method. The optical 90° hybrid combines the received signal laser with the local laser and outputs four-channel mixing light. The two in-phase light channels enter into the first balanced detector, and the two quadrature light channels enter into the second balanced detector. The output voltages of the I-arm and Q-arm are expressed as

$$V_I(t) = 2(1 - k_S) R R_L \sqrt{P_S P_{\rm LO}} \cos[\varphi_n(t) - \varphi_{\rm LO}(t) + \theta(t)] + n_I(t), \qquad (1)$$

$$V_Q(t) = 2k_S R R_L \sqrt{P_S P_{\rm LO}} \sin[\varphi_n(t) - \varphi_{\rm LO}(t) + \theta(t)] + n_Q(t),$$
(2)



Fig. 1. Schematic of the experimental device for direct phase control method.

where k_S is the power splitting ratio of the optical 90° hybrid to the Q-arm and is equal to 0.5; *R* and R_L are the responsivity of the balanced detector and the load resistance, respectively; P_S and $P_{\rm LO}$ are the received signal laser power and the local laser power, respectively; $\varphi_n(t)$ is the carrier phase difference; $\varphi_{\rm LO}(t)$ is the phase of the local laser controlled by the direct phase control method; $\theta(t)$ (=0, π) is the BPSK phase modulation; and $n_I(t)$ and $n_Q(t)$ are the shot-noise processes for the Iarm and Q-arm, respectively.

The two analog signals, $V_I(t)$ and $V_Q(t)$, were sampled and quantized synchronously by the two ADCs, and the two digitized signals were used to calculate the carrier phase difference between the signal light and the local oscillator light. They are expressed as

$$V_I(k) = A\cos[\varphi_n(k) - \varphi_{\rm LO}(k) + \theta(k)] + n_I(k), \qquad (3)$$

$$V_Q(k) = A\sin[\varphi_n(k) - \varphi_{\rm LO}(k) + \theta(k)] + n_Q(k), \qquad (4)$$

where $A = RR_L \sqrt{P_S P_{LO}}$, and *k* represents the index of the sampled signal. In order to obtain the real-time carrier phase difference, the method of pluralizing and then squaring is used to eliminate the influence of $\theta(k)$; the processed signal and the real-time phase difference are expressed as

$$V_{\text{SQUARE}}[k] = (V_I[k] + j \times V_Q[k])^2$$

= $A^2 \exp(j \times 2\theta_d[k]) + 2A \exp(j \times \theta_d[k]) \times n_I[k]$
+ $2A \exp[j \times (\theta_d[k] + \pi/2)] \times n_O[k],$ (5)

$$\theta_{\text{error}}[k] = \frac{1}{2} \operatorname{atan} 2[\operatorname{imag}(V_{\text{SQUARE}}[k])/\operatorname{real}(V_{\text{SQUARE}}[k])], \quad (6)$$

where $\theta_d[k] = \varphi_n(k) - \varphi_{LO}(k) + \theta(k)$, imag(·) represents the imaginary part of $V_{SQUARE}[k]$; real(·) represents the real part of $V_{SQUARE}[k]$; $2\theta[k]$ (=0, 2π) has no impact on the calculation; atan 2 represents the four-quadrant inverse-tangent operation, and $j = \sqrt{-1}$. The core of the direct phase control method is that each calculated $\theta_{error}[k]$ directly changes the phase of the local oscillator light, which means that if $\theta_{error}[k] = \varphi_1$, then the phase of the local oscillator light will be increased by φ_1 ; and, if $\theta_{error}[k] = -\varphi_2$, then the phase of the local oscillator light will be reduced by φ_2 .

The direct change in the local oscillator light phase depends on the cooperation between the control electrical signal and the direct phase generation external modulation module, as shown in Fig. 2. When the IQ bias controller is working normally, two orthogonal control signals are added to the radio frequency (RF) input of the IQ modulator. If the expression of the module input light is $E_{in}(t) = \sqrt{P_{L0}} \cos(\omega_{LO}t + \varphi_{LO})$, where P_{LO} is the input optical power, ω_{LO} is the angular frequency of input light, and φ_{LO} represents the initial phase of input light, the output light of the module can be expressed as



Fig. 2. Specific structure diagram of direct phase generation external modulation module.

$$E_{\rm out}(t) = -\sqrt{2p_{\rm LO}}\cos(\omega_{\rm LO}t + \varphi_{\rm LO}) \\ \times \sin\left[\frac{A_{\rm rf}\sin(\omega_{\rm rf}t + \varphi_{\rm rf} + \Delta\varphi)}{2V_{\pi}} \times \pi\right] \\ -\sqrt{2p_{\rm LO}}\sin(\omega_{\rm LO}t + \varphi_{\rm LO}) \\ \times \sin\left[\frac{A_{\rm rf}\cos(\omega_{\rm rf}t + \varphi_{\rm rf} + \Delta\varphi)}{2V_{\pi}} \times \pi\right], \quad (7)$$

where $A_{\rm rf}$ represents half of the peak–peak value of the RF signal; V_{π} represents the half-wave voltage of the IQ modulator; $\omega_{\rm rf}$ represents the angular frequency of the RF signal; $\varphi_{\rm rf}$ represents the initial phase of the RF control signal, and $\Delta \varphi$ represents the compensation phase of direct phase control, which is used for phase locking. When $A_{\rm rf}$ is small, according to the approximation sin $x \approx x$, Eq. (7) can be expressed as

$$E_{\text{out}}(t) \approx -2\sqrt{p_{\text{LO}}}\cos(\omega_{\text{LO}}t + \varphi_{\text{LO}}) \times \frac{\pi A_{\text{rf}}\sin(\omega_{\text{rf}}t + \varphi_{\text{rf}} + \Delta\varphi)}{2V_{\pi}} - 2\sqrt{p_{\text{LO}}}\sin(\omega_{\text{LO}}t + \varphi_{\text{LO}}) \times \frac{\pi A_{\text{rf}}\cos(\omega_{\text{rf}}t + \varphi_{\text{rf}} + \Delta\varphi)}{2V_{\pi}} = -2\sqrt{p_{\text{LO}}}\frac{\pi A_{\text{rf}}}{2V_{\pi}}\sin[(\omega_{\text{LO}} + \omega_{\text{rf}})t + \varphi_{\text{LO}} + \varphi_{\text{rf}} + \Delta\varphi].$$
(8)

The correctness of Eq. (8) depends on the IQ bias controller to control the IQ modulator at the direct-current bias point when realizing quadrature phase-shift keying (QPSK). Equation (8) shows that the phase change of the local oscillator light can be realized by directly changing the RF signal phase. This is the physical basis for realizing the direct phase control method; $\Delta \varphi$ is the foundation of phase locking in this method.

The frequency difference between the signal light and the local oscillator light should meet the following condition: $-F/6 < \Delta \omega < F/6$, where *F* is the output sampling rate of the two digital-to-analog converters (DACs); $\Delta \omega$ can be obtained in real time by performing a fast Fourier transform (FFT) on $V_{\text{SQUARE}}[k]$. When the direct phase control method starts, the analog signal output by the two DACs can be expressed as

$$\begin{cases} V_{IDAC}(t) = A_{rf} \cos(\omega_{base} t) \\ V_{ODAC}(t) = A_{rf} \sin(\omega_{base} t), \end{cases}$$
(9)

where $\omega_{\text{base}} = \Delta \omega$. In order to calculate the carrier phase difference accurately, smooth filtering should be performed by calculating the average of *L* samples to eliminate random noise. Next, *H* sets of data after smoothing are averaged as the phase difference of one calculation. The FPGA will calculate the first carrier phase difference $\theta_{\text{error}(1)}$. After the loop delay time τ , the analog signal outputs by the two DACs are expressed as

$$\begin{cases} V_{IDAC}(t) = A_{\rm rf} \, \cos(\omega_{\rm base}t + \theta_{\rm error(1)}) \\ V_{QDAC}(t) = A_{\rm rf} \, \sin(\omega_{\rm base}t + \theta_{\rm error(1)}) \end{cases}$$
(10)

The latter phase difference must be obtained at least after the previous phase difference calculation is completed, and then τ is performed. When the FPGA obtains *N* values of the phase difference, the analog signals output by the two DACs are expressed as

$$\begin{cases} V_{IDAC}(t) = A_{\rm rf} \cos[(\omega_{\rm base} + \omega_{\rm error(1)})t + \sum_{a=1}^{N} \theta_{\rm error(a)}] \\ V_{QDAC}(t) = A_{\rm rf} \sin[(\omega_{\rm base} + \omega_{\rm error(1)})t + \sum_{a=1}^{N} \theta_{\rm error(a)}], \end{cases}$$
(11)

where *a* is the sequence number of the calculated phase difference; $\sum_{a=1}^{N} \theta_{\text{error}(a)}$ represents the cumulative value of the first *N* phase difference; and $\omega_{\text{error}(1)}$ represents the value of the first linear phase compensation, which can be expressed as

$$\omega_{\text{error}(1)} = \sum_{a=1}^{N} \theta_{\text{error}(a)} / (N \times T), \qquad (12)$$

where *T* is the time interval for direct phase control and satisfies $T > \tau$. Therefore, the universal expression of two orthogonal analog control signals output by the two DACs is

$$\begin{cases} V_{IDAC}(t) = A_{\rm rf} \cos[(\omega_{\rm base} + \sum_{b=1}^{x} \omega_{\rm error(b)})t + \sum_{a=1}^{x \times N+y} \theta_{\rm error(a)}] \\ V_{QDAC}(t) = A_{\rm rf} \sin[(\omega_{\rm base} + \sum_{b=1}^{x} \omega_{\rm error(b)})t + \sum_{a=1}^{x \times N+y} \theta_{\rm error(a)}] \end{cases}$$
(13)

where *b* is the sequence number of the linear phase compensation; *x* is the operation time of linear phase compensation; $x \times N + y$ is the operation time of direct phase control, y < N; *b* will change when *a* changes *N* times, and the linear phase compensation is also in the form of accumulation.

In a traditional OPLL system, the voltage-controlled oscillator is a voltage-frequency conversion device, which means that the carrier phase-locking depends on the change of the control signal frequency. However, the realization of phase-locking does not necessarily depend on the changing frequency. Direct phase compensation can also achieve carrier phase-locking. This method is to complete phase lock by applying an accumulated phase change $\sum_{a=1}^{x \times N+y} \theta_{\text{error}(a)}$ to the electrical control signal. Owing to the existence of the loop delay, linear phase compensation $\sum_{b=1}^{x} \omega_{\text{error}(b)}$ is also required, which is reflected in Eq. (13).

3. Results and Discussion

In this experimental verification, the sampling rates of both ADCs were 1 GHz; F = 100 MHz; L = 10; H = 8; N = 8; $\tau = 530$ ns; and T = 880 ns. Therefore, it is equivalent to applying a direct phase control operation every 880 ns and linear phase compensation every 7040 ns. The existence of loop delay is a prerequisite for linear phase compensation.

In our experiments, the ADC model is EV10AQ190A (Teledyne e2v, UK). The DAC model is AD9747 (Analog Devices, US). The series of the FPGA is XC7K325TFFG900-2 (Xilinx, US). The IQ modulator model is FTM7962EP (FUJITSU, JPN). The IQ bias controller model is MBC-IQ-03 (plugtech, CHN). The electrical amplifier model is OA3MHQM (Centellax, US). The balanced detector model is LB-BPD10G (SDFSO, CHN). The other experimental parameters used for this verification are listed in Table 1.

Within a period of time before and after the start of the direct phase-locking method, the change curve of double phase difference is shown in Fig. 3. The details inside the two dashed boxes in Fig. 3 are shown in Fig. 4. It can be seen from Fig. 4(a) that before the direct phase control method starts, the signal laser frequency is greater than the local laser frequency, which is 4.763 MHz. The FPGA begins to compensate the frequency difference at 2.39×10^{-6} s and begins to calculate the average value of the eight phases at 2.96×10^{-6} s. The DACs perform direct phase control operations after 530 ns. After 880 ns, they obtain new phase values and continue to carry out phase compensation. It can be considered that the loop acquisition time is

Table 1. Experimental Parameters.

Parameter	Symbol	Value
Laser wavelength	λ	1554.94 nm
Received signal power	P_S	—45 to —33 dBm
Communication rate	R_b	2.5 Gbit/s
Line width (TX/RX)	ΔV	5000 Hz
Responsivity	R	0.75 A/W
Power-splitting ratio	k _s	0.5



Fig. 3. Double phase difference curve before and after direct phase control method.



Fig. 4. Partial image of double phase difference curve in Fig. 3: (a) left dashed box; (b) right dashed box.

approximately 530 ns, from the beginning of applying the direct phase control method to the completion of the phase-locking, and the phase-locking can be completed directly without cycle skipping. Next, the direct phase compensation and linear phase compensation operations will continue, as described in Eq. (13). As can be calculated from Fig. 4(b), the standard deviation of the phase-locked error is 5.2805°. The eye diagram of demodulated signal is shown in Fig. 5.

In the coherent communication experiment based on the direct phase control method, the relationship between the BER and the power of the input signal laser was measured, as shown in Fig. 6.

When the BER of 10^{-9} is obtained, the measured curve has an approximately 18 dB penalty compared to the theoretical curve.



Fig. 5. Eye diagram of 2.5 Gbit/s baseband signal after phase locking.



Fig. 6. BER versus received signal power for 2.5 Gbit/s.

The BER of the homodyne BPSK communication system can be expressed as

$$P_b(\Phi) = \frac{1}{2} \operatorname{erfc}\left(\sqrt{\operatorname{SNR}}\cos\Phi\right),\tag{14}$$

where SNR is the signal-to-noise ratio; Φ is the phase-locked error; and erfc(x) is a Gaussian error function defined as

$$\operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_{x}^{+\infty} e^{-t^{2}} \mathrm{d}t.$$
 (15)

In the case of a shot noise limit, the SNR can be expressed as

$$SNR = \frac{\eta P_S}{h\nu R_b},$$
 (16)

$$V_{\text{shot-noise}} = \sqrt{4qB_e RP_{\text{LO single}}} \times R_L, \tag{17}$$

where q is the electronic charge; B_e is the detector effective noise bandwidth, and $B_e = 10 \text{ GHz}$; R is the detector responsivity, R = 0.75 A/W; $P_{\text{LO single}}$ is the optical power entering a single input arm of the balanced detector, and $P_{\text{LO single}} = 60 \,\mu\text{W}$; and R_L is the detector transimpedance, and $R_L = 10 \text{ k}\Omega$. It is calculated that $V_{\text{shot-noise}} = 0.0054 \text{ V}$. The voltage standard deviation of the electrical signal of all noise (including thermal noise, shot noise, and relative intensity noise) was measured as $V_{\text{all-noise}} = 0.01 \text{ V}$. Therefore, cases that do not meet the shot noise limit introduce a 5.4 dB penalty. The quantum efficiency is (0.75 A/W)/(1.25 A/W) = 0.6, which introduces a 2.2 dB penalty. The residual phase-locked error of the direct phase control method introduces a 2 dB penalty. Insertion loss of the optical 90° hybrid to signal light introduces a 1.5 dB penalty. The remaining 0.9 dB penalty is from other factors, for example, the signal quality of the transmitter, the polarization dependent loss, the non-orthogonality of the IQ signals, and the imperfect heterodyne efficiency.

4. Conclusion

In summary, a 2.5 Gbit/s BPSK coherent communication system based on the direct phase control method has been studied. By directly changing the optical phase of the local oscillator, the conversion of phase-frequency-phase is avoided, and a closed loop from phase to phase is realized. In combination with reality, the various parameters corresponding to the actual algorithm have been determined. Phase locking can be achieved without cycle skipping, and the acquisition time is 530 ns. Under the condition of an input optical power of -34.4 dBm, the BER is 10^{-9} . After the phase-locking is completed, the standard deviation of the phase-locked error is 5.2805°. Using this method also takes advantage of the single-sideband modulation characteristics of the IQ modulator, which can avoid the use of narrowband optical filters and simplify the experimental equipment. This method is of great significance to the development of high-speed homodyne space coherent laser communication. In addition, the method can be optimized from reducing the loop delay, improving the quality of the DAC control signal, and utilizing a lower noise detector to further reduce the demand for laser linewidth, reducing the phase-locked error.

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