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Efficient silicon integrated four-mode edge coupler for few-mode fiber coupling

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Here, we designed a broadband, low loss, compact, and fabrication-tolerant silicon-based four-mode edge coupler, composed of a 1×3 adiabatic mode-evolution counter-taper splitter and a triple-tip inverse taper. Based on mode conversion and power splitting, the proposed structure can simultaneously realize efficient mode coupling from TE_0, TM_0, TE_1, and TM_1 modes of multimode silicon waveguides to linearly polarized (LP), $LP_{01,x}$, $LP_{01,y}$, $LP_{11a,x}$, and $LP_{11a,y}$, modes in the few-mode fiber. To the best of our knowledge, we proposed the first scheme of four LP modes coupling, which is fully compatible with standard fabrication process. The 3D finite-difference time-domain simulation results show that the on-chip conversion losses of the four modes remain lower than 0.62 dB over the 200 nm wavelength range, and total coupling losses are 4.1 dB, 5.1 dB, 2.1 dB, and 2.9 dB for TE_0-to-$LP_{01,x}$, TM_0-to-$LP_{01,y}$, TE_1-to-$LP_{11a,x}$, and TM_1-to-$LP_{11a,y}$, respectively. Good fabrication tolerance and relaxed critical dimensions make the four-mode edge coupler compatible with standard fabrication process of commercial silicon photonic foundries.

Keywords: multimode coupling; CMOS compatibility; silicon waveguide; few-mode fiber.
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1. Introduction

Silicon photonics has been attracting lots of attention in recent years[1], benefiting from the compatibility with standard complementary metal-oxide-semiconductor (CMOS) fabrication technology, which significantly reduces the fabrication cost of silicon photonic devices. The silicon-on-insulator (SOI) platform has been widely used in on-chip communication systems with low insertion loss and small footprint[2,3]. Meanwhile, in order to satisfy the rapidly increasing demands on high capacity and low power consumption data transfer, mode-division multiplexing (MDM) has also emerged as an efficient approach to further increase the transmission capability[4] with the introduction of high-order modes in both fibers and silicon chips[5,6]. Many on-chip multichannel mode (de)multiplexers have been developed[7–9], but, in order to implement a complete on-chip MDM optical network, large data transmission capacity and low-loss coupling between few-mode fibers (FMFs) and on-chip multimode waveguide are also highly needed[10].

It is a challenging task to design efficient couplers with large bandwidths, low insertion loss, and small footprint that connect on-chip multimode waveguides and FMFs due to their huge mode mismatch. Vertical and edge coupling schemes are the most common ways to realize multimode fiber-chip coupling. For vertical coupling, grating couplers (GCs)[11–14] are usually used due to their small footprint and large misalignment tolerance. However, the GCs are intrinsically sensitive to fabrication error and wavelength, which significantly limit their application in broadband wavelength-division multiplexing (WDM). Compared with GCs, edge couplers can overcome the drawbacks of polarization/wavelength sensitivity. The 3D-mode multiplexer structure based on multilayer asymmetric waveguide branches has been reported for four-mode coupling[15], while the fabrication becomes complicated for different waveguide heights. Multi-stage silicon inverse taper couplers with polymer up-cladding realized four linearly polarized (LP) modes coupling[16], but the large total length (2.68 mm) and lack of compatibility with standard CMOS fabrication process limited its application. The double-tip inverse taper was demonstrated to

realize the first, to the best of our knowledge, high-order mode coupling[17], and some three inverse tapers for two-mode coupling have been reported[10,18] with large mode conversion losses and coupling losses[10]. Although these types of couplers mentioned can meet some performance requirements, it is a challenge for an on-chip multimode coupler to simultaneously satisfy compact, low loss, wavelength-independent, and CMOS compatibility.

In this Letter, we report a silicon edge coupler based on adiabatic taper for four-mode fiber-to-chip coupling. The proposed coupler consists of a 1×3 adiabatic mode-evolution counter-taper splitter and a triple-tip inverse taper. The 3D finite-difference time-domain (FDTD) simulation results show that the on-chip conversion losses of the four-mode edge coupler (FMEC) are 0.01 dB, 0.02 dB, 0.07 dB, and 0.27 dB for the input TE_0, TM_0, TE_1, and TM_1 modes at 1.55 μm wavelength, respectively, and, in the wavelength range from 1.45 to 1.65 μm, the mode conversion loss remains lower than 0.62 dB. Meanwhile, the designed feature size is 100 nm, which is compatible with the standard process of commercial silicon photonic foundries. The calculated total coupling losses between the edge coupler and FWF are 4.1 dB, 5.1 dB, 2.1 dB, and 2.9 dB for TE_0-to-$LP_{01,x}$, TM_0-to-$LP_{01,y}$, TE_1-to-$LP_{11a,x}$, and TM_1-to-$LP_{11a,y}$, respectively. Moreover, the fabrication tolerance analysis confirms that the FMEC remains fairly low loss within a large deviation range (±50 nm for silicon waveguide width).

2. Operation Principle and Device Design

Figure 1(a) presents the schematic of the designed FMEC, which consists of a 1×3 adiabatic mode-evolution counter-taper splitter and a triple-tip inverse taper. The FMEC is designed on an SOI wafer with 220 nm thick top silicon layer, 4.5 μm thick upper SiO_2 cladding, and 3 μm thick bottom SiO_2 cladding. The operation principle in the FMEC is based on the mode evolution in a coupler that has two waveguides with cores counter-tapered[19,20]. As shown in Fig. 1(b), the width of the upper waveguide (WG1) increases from 0.25 to 0.48 μm, whereas the width of the bottom waveguide (WG0) varies from 1.0 μm to 0.77 μm. We use Lumerical finite-difference eigenmode (FDE) solver to calculate the effective refractive indices of TE_0, TM_0, TE_1, and TM_1 in WG0 and those of TE_0 and TM_0 in WG1 at the 1.55 μm wavelength. As we can see, there is a cross point for TE_1 in WG0 and TE_0 in WG1, TM_1 in WG0 and TM_0 in WG1, respectively, which means the input TE_1 and TM_1 modes in WG0 can adiabatically convert to the TE_0 and TM_0 modes in the adjacent WG1, respectively. There is no cross point with their own polarization modes for the TE_0 and TM_0 curves of WG0, which means the input TE_0 and TM_0 modes will remain propagating in the central waveguide. The width difference for both sides of tapers is chosen as 0.23 μm to ensure a large difference of effective indices, where the converted mode would not be coupled back. Thus, in the FMEC, the input TE_0 and TM_0 modes will be mapped to the central output. The input TE_1 and TM_1 modes can be converted

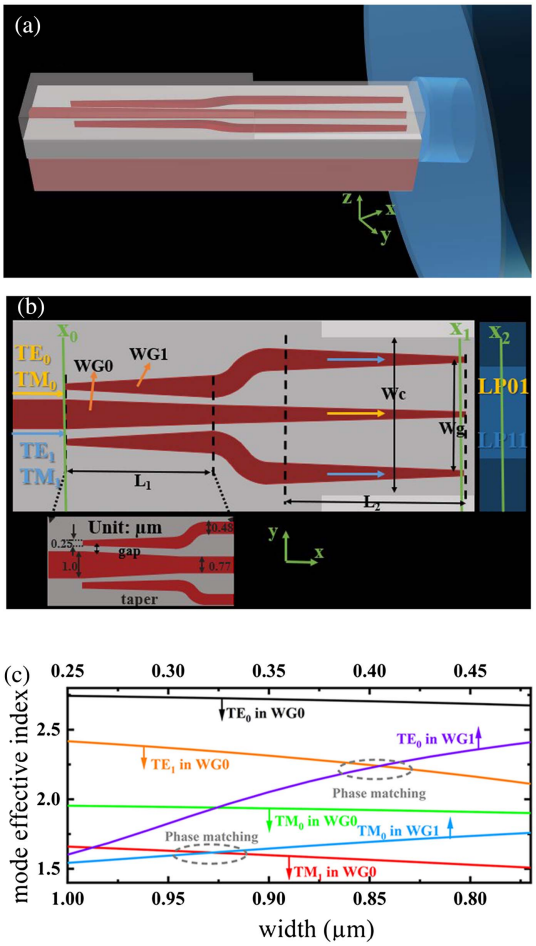

Fig. 1. Schematics of DMEC coupling with dual-mode fiber in (a) 3D view and (b) top view; the silicon waveguides are in red, and the silicon oxide layer is in gray. The modes conversion process is also demonstrated. (c) Effective refractive index of the modes in each waveguide (WG0/WG1) of the mode-evolution counter-taper with tapering width from 1 μm/0.25 μm to 0.77 μm/0.48 μm.

and divided into two TE_0 modes and two TM_0 modes with identical intensity and out-phase, and eventually output through the upper and bottom single-mode waveguides of the FMEC separately. For the triple-tip inverse taper, as the waveguide narrows, the middle inverse taper converts the mode field (TE_0/TM_0 mode) confined in the silicon waveguide into the clad layer, collected by the FMF, and eventually evolves into $LP_{01,x}$ and $LP_{01,y}$ modes. The mode fields of two side inverse tapers keep expanding between the taper tips and convert into the TE_1/TM_1 mode field at the edge of the chip, collected by FMF, and eventually evolve into the $LP_{11,x}$ and $LP_{11,y}$ modes.

3. Simulation and Analysis

3.1. Optimization of FMEC

To analyze the performance of FMEC, the simulation is separated into two parts, the on-chip mode conversion from 'x_0' – 'x_1' in Fig. 1(b), and the spatial mode coupling from the

triple-tip inverse taper to the fiber [‘x_1’ – ‘x_2’ in Fig. 1(b)]. First, we use the eigenmode expansion (EME) solver to optimize the taper length (L_1, L_2), and the parameters used in simulation are shown in Fig. 1(b). In order to satisfy the feature size of commercial silicon foundries, the gaps between the upper and bottom tapers are all set to be 200 nm, and the taper tip width is set to be 100 nm. Figures 2(a) and 2(b) show the losses from the 1×3 adiabatic mode-evolution counter-taper splitter (L_1) and inverse taper (L_2) at the 1.55 μm wavelength. The mode conversion losses are less than 0.2 dB when $L_1 > 230$ μm, and propagation losses in the inverse taper are less than 0.6 dB when $L_2 > 400$ μm. Here, we choose $L_1 = 250$ μm and $L_2 = 450$ μm to ensure a good trade-off between low loss and small footprint for both modes, and the length of the bending section between the 1×3 adiabatic mode-evolution counter-taper splitter and inverse taper is 40 μm, so the whole device has 740 μm total length. The on-chip conversion losses of FMEC are less than 0.01 dB, 0.02 dB, 0.07 dB, and 0.27 dB for the input TE_0, TM_0, TE_1, and TM_1 modes at the 1.55 μm wavelength, respectively, and, in the wavelength range from 1.45 to 1.65 μm, the mode conversion loss remains lower than 0.62 dB. With the optimized taper length, the transmission spectra of the designed mode-evolution part [‘x_0’ – ‘x_1’ in Fig. 1(b)] are simulated via the 3D-FDTD solver, as shown in Fig. 2(c).

However, the coupling between the triple-tip taper and FMF presents larger coupling loss, mainly caused by the mismatched mode fields between chip edge and FWF. In the simulation model, the diameters of core and cladding of the FMF are 14 μm and 125 μm, with the refractive indices of 1.4485 and 1.44402, respectively. The silicon substrate may cause more loss because of leaky modes, so we remove the substrate of the SOI wafer[21,22], as shown in Fig. 3. In order to optimize the coupling loss, there are two parts we needed to analyze separately: the integral of mode overlap of the FMF and SiO_2 cladding and

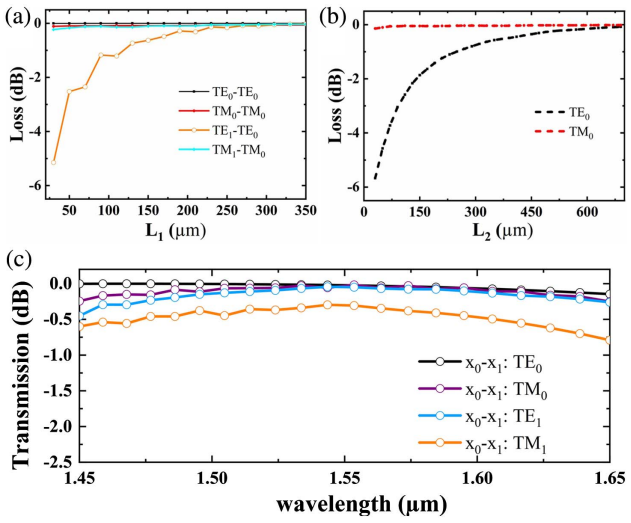

Fig. 2. (a) Mode conversion loss for the input TE_0, TM_0, TE_1, and TM_1 modes, respectively, (b) transmission loss for the TE_0 and TM_0 modes in inverse taper (L_2), and (c) wavelength dependence of the transmission from ‘x_0’–‘x_1’.

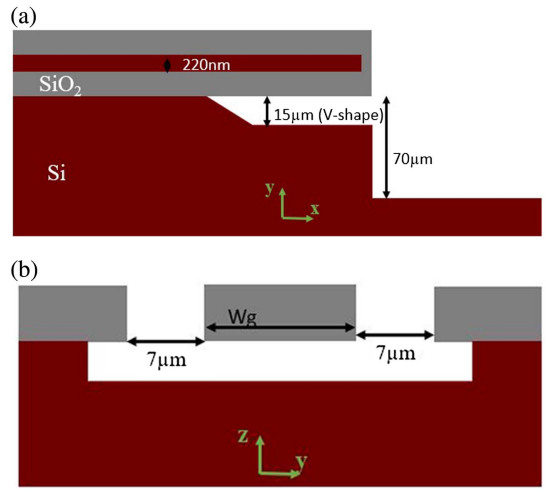

Fig. 3. Cross-sectional schematics of the edge coupling area: (a) *x*–*y* direction; (b) *y*–*z* direction.

the mode coupling loss between the FMF and silicon triple-tip taper. We first optimize the overlap integral in Fig. 4(a). The cladding width (Wc) [Fig. 1(b)] is chosen to be 19 μm in order to achieve largest average overlap for four modes. In the second step, we optimize the coupling loss of the silicon triple-tip taper with FMF, which is decided by the taper tip width

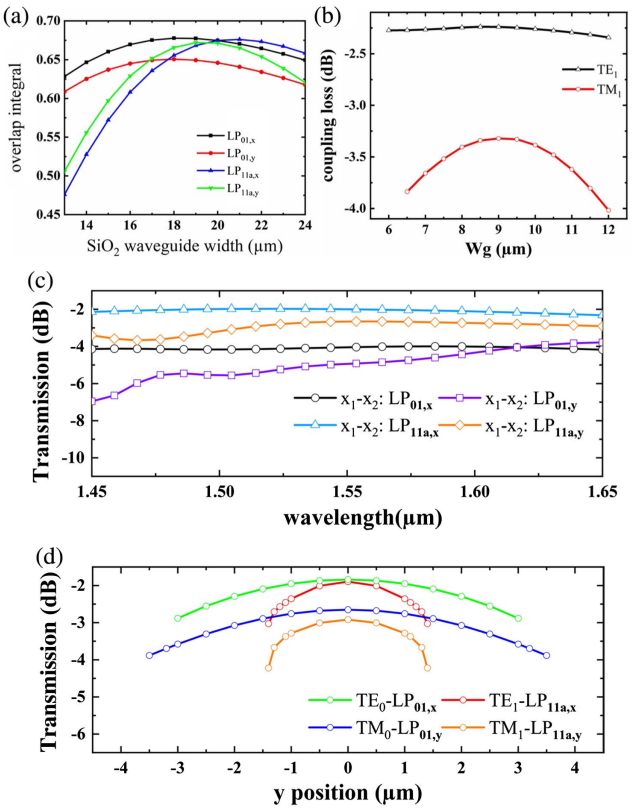

Fig. 4. (a) Simulated overlap integral of mode field between the FMF and SiO_2 cladding, (b) simulated coupling loss for different Wg, (c) spatial mode coupling (from ‘x_1’–‘x_2’), and (d) the lateral alignment tolerance of coupling efficiency (CE) for spatial mode coupling.

and the gap spacing (Wg) between upper and bottom tapers for TE_1 and TM_1 modes. Figure 4(b) shows the coupling losses for different Wg. The Wg is chosen to be 9 μm. With the optimized parameters, we calculated the coupling losses between the triple-tip taper and FMF in 3D-FDTD, which are 4.0 dB, 5.0 dB, 2.0 dB, and 2.6 dB for TE_0-to-$LP_{01,x}$, TM_0-to-$LP_{01,y}$, TE_1-to-$LP_{11a,x}$, and TM_1-to-$LP_{11a,y}$, respectively, as shown in Fig. 4(c) ('x_1' – 'x_2'). Considering that those calculation results are based on the case of center excitation, we also simulate the lateral alignment tolerances of spatial mode coupling between the chip edge and FMF. In Fig. 4(d), the simulation results show that the coupling losses of $LP_{01,x}$, $LP_{01,y}$, $LP_{11a,x}$, and $LP_{11a,y}$ present the 1 dB lateral alignment tolerances of 3 μm, 3.2 μm, 1.3 μm, and 1.3 μm. Therefore, we need a high accuracy alignment stage to measure the FMEC with high efficiency. Table 1 shows a comparison of the reported state-of-the-art multimode edge coupler. Compared to those types, the proposed FMEC exhibited low loss, more modes, and compatibility with CMOS.

The total coupling efficiency (CE) of the FMEC is 4.1 dB, 5.1 dB, 2.1 dB, and 2.9 dB for TE_0-to-$LP_{01,x}$, TM_0-to-$LP_{01,y}$, TE_1-to-$LP_{11a,x}$, and TM_1-to-$LP_{11a,y}$, respectively, and the crosstalk is less than −25 dB with broadband operation, as the spectra of CE and crosstalk shown in Figs. 5(a) and 5(b). As a double-tip inverse taper coupling scheme has been proven for the first high-order mode coupling experimentally[17], we have good potential to realize efficient FMEC with fewer losses experimentally.

Table 1. Comparison of the Reported Multimode Edge Coupler and Coupler Proposed in This Work.

Ref.	Number of Modes	Compatible with CMOS	Coupling Loss (dB)	Evaluation Method
[10]	2	Yes	$TE_0 - LP_{01}$: 10.11	Numerical
2020			$TE_1 - LP_{11}$: 8.8	
[15]	4	No	LP_{01}: 8.8	Experimental
2017			LP_{11a}: 9.0	
			LP_{11b}: 9.6	
			LP_{21a}: 9.9	
[17]	1	Yes	$TE_1 - LP_{11}$: 3	Numerical
2017			$TE_1 - LP_{11}$: 5.5	Experimental
[16]	4	No	No data	/
2020				
This work	4	Yes	$TE_0 - LP_{01,x}$: 4.1	Numerical
			$TM_0 - LP_{01,y}$: 5.1	
			$TE_1 - LP_{11a,x}$: 2.1	
			$TM_1 - LP_{11a,y}$: 2.9	

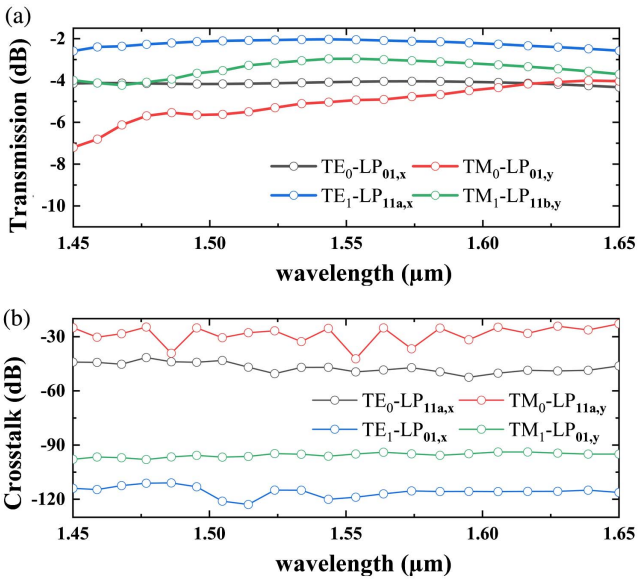

Fig. 5. (a) Total CE and (b) crosstalk of the FMEC in the span of 200 nm.

Figures 6(a)–6(p) show the simulated mode propagation for the input TE_0, TM_0, TE_1, and TM_1 modes, respectively, illustrating the mode conversion and coupling as we expected. Compared to the latest research[10], their simulation results show that the on-chip conversion efficiencies of the dual-mode edge coupler (DMEC) are 69% and 62% for TE_0 and TE_1, respectively, with 3 dB bandwidth of more than 200 nm. By using a multimode interference (MMI) structure, the large conversion loss enlarged the total coupling loss between the on-chip

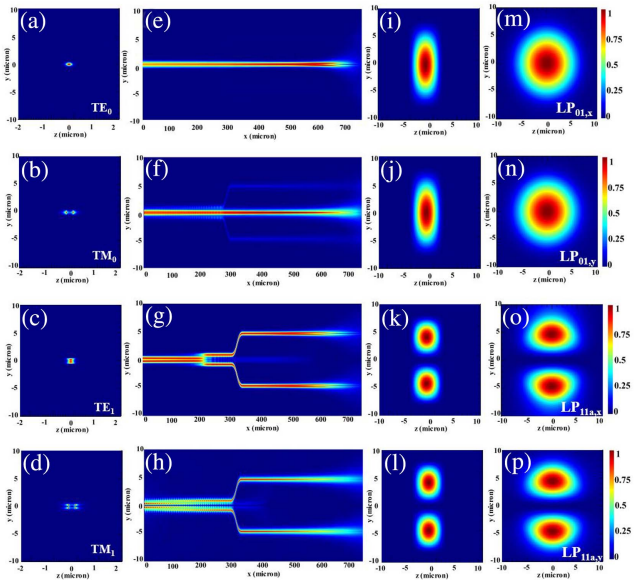

Fig. 6. Simulated electrical field mode profiles of (a) TE_0, (b) TM_0, (c) TE_1, and (d) TM_1 modes at position 'x_0' in Fig. 1(b); transmission profiles of the input (e) TE_0, (f) TM_0, (g) TE_1, and (h) TM_1 modes; mode profiles of the (i) TE_0, (j) TM_0, (k) TE_1, and (l) TM_1 modes in the SiO_2 waveguide; mode profiles of (m) $LP_{01,x}$, (n) $LP_{01,y}$, (o) $LP_{11a,x}$, and (p) $LP_{11a,y}$ modes supported in FMF.

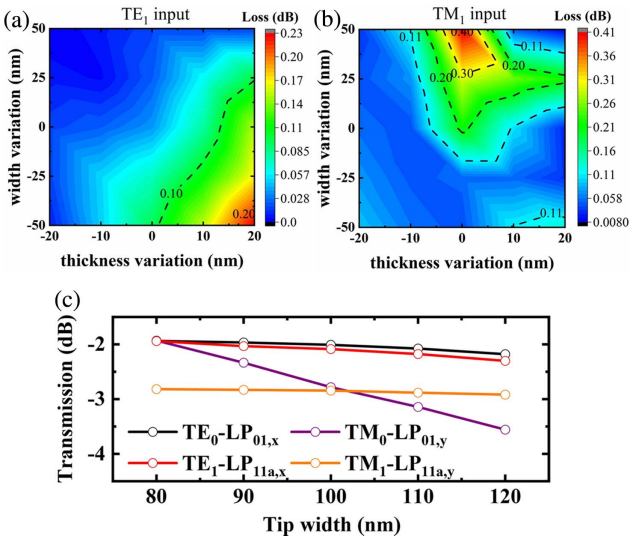

Fig. 7. Fabrication tolerance to deviation (a) of the waveguide width and thickness for TE_1 input mode, (b) of the waveguide width and thickness for TM_1 input mode, (c) of the tip width.

multimode waveguide and FWF, resulting in the total coupling loss of DMEC being more than 10 dB numerically. With our scheme, it can significantly reduce the on-chip conversion loss and scale up to four-mode coupling simultaneously.

3.2. Analysis of fabrication tolerance

In order to ensure reliability, Figs. 7(a) and 7(b) show the fabrication tolerance for on-chip conversion using EME by scanning the thickness and tapers waveguide width (which also causes gap distance variations), where the widths of both ends of the tapers vary simultaneously. Compared with that of high-order modes, the loss of input fundamental modes is negligible, so we only consider the conversion loss variations of the input TE_1 and TM_1 modes under the different fabrication error. The calculated conversion losses are always below 0.42 dB, as long as the waveguide width and thickness are controlled within the fabrication error variations of ±50 nm and ±20 nm, respectively, which can be readily achieved by commercial silicon photonics foundries. The fabrication tolerance of the mode conversion based on counter-tapers[23] and power splitting based on adiabatical tapers[24,25] have been proved. In addition, the tolerance simulation for the tip width was also performed. Considering 10% fabrication error, the increase of coupling loss between the inverse taper tip and fiber is below 0.28 dB, as shown in Fig. 7(c).

4. Conclusions

We design a compact, low loss, broadband, and fabrication-tolerant silicon photonic FMEC based on mode-evolution counter-tapers and a triple-tip inverse taper, serving as a bridge between the FMF and multimode chip, so that the input TE_0, TM_0, TE_1, and TM_1 modes can simultaneously couple into the FMF. The rigorous 3D-FDTD simulations show that the on-chip conversion losses of FMEC are 0.01 dB, 0.02 dB, 0.04 dB, and 0.27 dB for TE_0, TM_0, TE_1, and TM_1, respectively, and less than 0.62 dB in the wavelength range from 1.45 to 1.65 μm, which is negligible for the total coupling loss between FMEC and FMF compared with the coupling loss between triple-tip inverse taper and FMF. The total coupling losses are 4.1 dB, 5.1 dB, 2.1 dB, and 2.9 dB for TE_0-to-$LP_{01,x}$, TM_0-to-$LP_{01,y}$, TE_1-to-$LP_{11a,x}$, and TM_1-to-$LP_{11a,y}$, respectively, and less than 7 dB in the wavelength range from 1.45 to 1.65 μm theoretically. Considering fabrication and misalignment errors experimentally[17], we have the potential to realize efficient FMEC with fewer losses experimentally. The device's compatibility with existing silicon photonics foundries and good fabrication tolerance enables the wide usage of the multimode edge coupler on a variety of silicon photonics applications. Considering the conversion loss is small enough for FMEC, further improvements could be adopted by reducing the coupling loss between the triple-tip inverse taper and FMF. A lensed or tapered FWF can be adopted to decrease the mode field area, which can obtain a better agreement with mode field distribution of FMEC. The inverse taper can also realize a better match of the mode field with the FMF and a larger misalignment tolerance through well-designed structures[26–28]. Without a complex design and fabrication process, the proposed structure provides much more convenience for both designers and manufacturers. Meanwhile, it also shows good performance under the consideration of fabrication errors. Limited by the silicon thickness of SOI waveguides, this design cannot be applied to vertical higher-order modes, but, combining with different waveguided-core heights, it is also possible to develop more higher-order modes. Further improvements can be done to realize a better performance multimode edge coupler, which can be potentially used to further increase the transmission capability for optical interconnections and communications.

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