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Optimization of optical signal-to-distortion ratio in a channel-interleaved photonic ADC via a coherent multi-frequency RF driver

Junyan Li (李俊燕), Na Qian (钱 娜), Shiyu Hua (化世玉), and Weiwen Zou (邹卫文)*

State Key Laboratory of Advanced Optical Communication Systems and Networks, Intelligent Microwave Lightwave Integration Innovation Center (iMLic), Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China

*Corresponding author: wzou@sjtu.edu.cn

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A microwave-chip-based coherent multi-frequency RF driver is developed for a channel-interleaved photonic analog-to-digital converter (PADC) system, which comprises a multi-class optical demultiplexer and supports a sampling speed of 40 GSa/s. The generated signals from the RF driver are adjustable in both amplitude and phase. We analyze the relationship between the characteristics of the generated RF driver signals and the demultiplexing performance in theory based on the optical signal-to-distortion ratio (OSDR). It is the most effective parameter to evaluate the performance of the demultiplexer in a PADC system without an electronic analog-to-digital converter. By precisely adjusting the amplitude and phase of signals, the OSDR is optimized. The results verify the compatibility between the RF driver and the PADC system.

Keywords: photonic analog-to-digital converter; multi-frequency RF driver; optical signal-to-distortion ratio.
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1. Introduction

With the increasing demand for high-speed sampling technology, photonic analog-to-digital converter (PADC) technology is regarded as an ideal solution that can overcome the bottleneck faced by electronic analog-to-digital converters (EADCs)[1–4]. To achieve an ultra-high sampling rate with high resolution, one of the most feasible PADC schemes is proposed, consisting of a photonic sampling front-end and an electronic digitization back-end[5,6]. In terms of the channel-interleaved PADC[7], many breakthroughs have been made in recent years[8–16]. Most of all, a previous research has demonstrated the application of a time-domain channel-interleaved demultiplexer in a high-speed PADC, which converts sampling series of 20 GSa/s into two parallel channels of 10 GSa/s[17]. This scheme is constructed by an array of photonic switches that are driven by RF signals. The characteristics of the RF signals are crucial to the performance of photonic switches as well as the demultiplexer[18]. However, multiple RF components separately packaged in modules result in bulkiness, high cost, and large power consumption, even when there are only two demultiplexed channels[17].

On the other hand, the technology of RF modules with a single or multichip is mature[19,20]. Passive and active elements can be integrated in organic laminates or low temperature co-fired ceramic (LTCC) substrates. In the multichip module, internal separating walls between cavities distribute the gain and isolate the cavities with minimum parasitic effects on chip parameters. Microstrip lines and gold wires are the main methods of connecting different chips. In this way, we can connect amplifiers and filters without microwave cables, which bring about large power loss and instability. Based on this situation, we design a compact RF module, which supports more demultiplexed channels to satisfy the requirement in practical applications of PADC.

2. Principles

In this Letter, we analyze the relationship between the characteristics of RF driver signals and the performance of a time-domain channel-interleaved demultiplexer based on photonic switches. The optical signal-to-distortion ratio (OSDR) is regarded as the most effective parameter to evaluate the demultiplexer performance. A multi-frequency RF driver is designed for the optimization of the OSDR in the PADC system. In our design, low noise amplifiers (LNAs), power amplifiers (PAs), variable attenuators (VAs), and variable phase shifters (VPSs) are cascaded to obtain sufficient gain and well-managed amplitude and phase. Then, the RF driver is applied in an eight-channel PADC system with a sampling rate of 40 GSa/s. The performance is verified in the demultiplexer of the sampling series.

A schematic of an eight-channel 40 GSa/s PADC system with a channel-interleaved demultiplexer based on photonic switches is illustrated in Fig. 1. In this scheme, an actively mode locked laser (AMLL) with a high repetition rate serves as a photonic sampling clock generator, and a Mach–Zehnder modulator (MZM) is used as a sampling gate. For the demultiplexer, an array of dual-output MZMs (DOMZMs) is applied as the photonic switches. The demultiplexed series are detected via photodiodes (PDs) and then digitized by EADCs for digital processing.

The topological structure of the demultiplexer can be considered as a binary tree of DOMZMs. In this structure, two DOMZMs are connected to each output port of the DOMZM in the previous class. A three-class cascaded scheme is shown in the inset of Fig. 1, which can convert the sampling series of 40 GSa/s into eight parallel channels with the speed of 5 GSa/s. In the channel-interleaved demultiplexer, the DOMZM in the first class is driven by an RF signal of 20 GHz, and the frequencies of the driver signals are 10 GHz and 5 GHz for the second and third classes, respectively.

The parameters of each RF signal should be properly managed. In mathematics, the conclusion in Ref. [17] can be extended to multi-channel cases. As for a demultiplexer consisting of multiple classes of DOMZMs, the switching response of one DOMZM in the Kth class can be expressed as

$$\alpha_K(t) = (\alpha_{\max,K} - \alpha_{\min,K})[1 + \eta_K(t)]/2 + \alpha_{\min,K}, \quad (1)$$

where $K = 1, 2, 3$, and $\alpha_{\max,K}$ and $\alpha_{\min,K}$ are the maximum and minimum transmittances of the DOMZM. $\eta_K(t)$ is demultiplexing modulation determined by the RF driver signal, which can be derived as

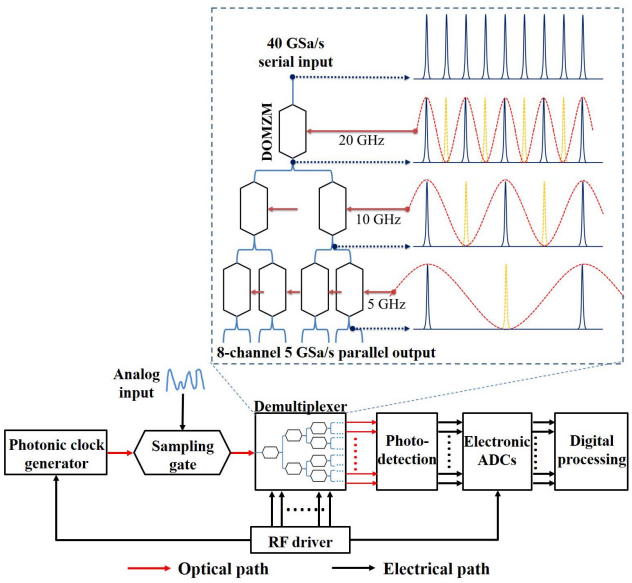

Fig. 1. Schematic of a 40 GSa/s eight-channel PADC with a channel-interleaved demultiplexer based on a binary tree of dual-output Mach–Zehnder modulators (DOMZMs). The inset shows the working mechanism of a three-class demultiplexer, which converts sampling series of 40 GSa/s into eight parallel channels of 5 GSa/s.

$$\eta_K(t) = \sin[\pi(V_K/V_{\pi,K})\cos(2\pi t/2^K T_S + \varphi_K)], \quad (2)$$

where V_K and φ_K are the amplitude and phase offsets of the applied driver signal in the Kth class, respectively. T_S is the temporal period of the photonic sampling clock, and $V_{\pi,K}$ is the AC half-wave voltage of the Kth-class DOMZM, which operates with DC quadrature bias. According to Ref. [17], the waveform of the driver signal should remain sinusoidal, and its amplitude should not exceed $V_{\pi,K}/2$ to avoid unexpected distortion.

In a three-class DOMZM-based demultiplexer, one of the demultiplexed series from the output of Kth-class DOMZM can be expressed as

$$s_{\text{demux}}(t) = s_{\text{ori}}(t)\prod_{K\le L}^{3}\alpha_L(t), \quad (3)$$

where $s_{\text{demux}}(t)$ and $s_{\text{ori}}(t)$ are the demultiplexed series and the original input series before demultiplexing, respectively. As shown in Eq. (3), the original input series is time-interleaved into eight parallel channels after three-class switching, as depicted in Fig. 2(a). In one period (i.e., $8T_S$) of each demultiplexed channel, a sampling pulse is selected to pass while the rest is suppressed by the switching response in Eq. (1). Assume that the maximums of each $\alpha_K(t)$ are temporally aligned at $t = 0$ with the sampling pulse selected to pass. Using Eqs. (1)–(3), the intensity of the selected pulse after the Kth-class DOMZM can be derived as

$$I_S = I_0\prod_{L\le K}^{3}\alpha_{+,L}, \quad (4)$$

where I_0 is the intensity of the original sampling series. I_S is the intensity of the selected pulse and $\alpha_{+,K} = \alpha_K\ (t = 0)$. As shown in Fig. 2(a), there are several remnants, which are considered as distortions, in the suppressed pulses after demultiplexing. The intensity can also be evaluated by Eqs. (1)–(3) as follows:

$$I_{D,K} = I_0\prod_{L<K}^{3}\alpha_{+,L}\times\alpha_{-,K}, \quad (5)$$

where $I_{D,K}$ $(K = 1, 2, 3)$ represents the intensity of the distortions, which are marked in Fig. 2(a) and measured from the output of the Kth-class DOMZM, and $\alpha_{-,K} = \alpha_K\ (t = 2^{K-1}T_S)$. Based on Eqs. (4) and (5), the demultiplexing performance of the Kth-class DOMZM could be evaluated by the ratio between the intensity of the selected pulse and distortions. It is a specific OSDR measured at the output of the Kth-class DOMZM as

$$\text{OSDR}_K = I_S/I_{D,K} = \alpha_{+,K}/\alpha_{-,K}, \quad (6)$$

where I_S and $I_{D,K}$ are defined by Eqs. (4) and (5), respectively. With the expression in Eq. (6), the OSDR of the final demultiplexed series after three-class DOMZMs can be calculated by Eqs. (3)–(5) as follows:

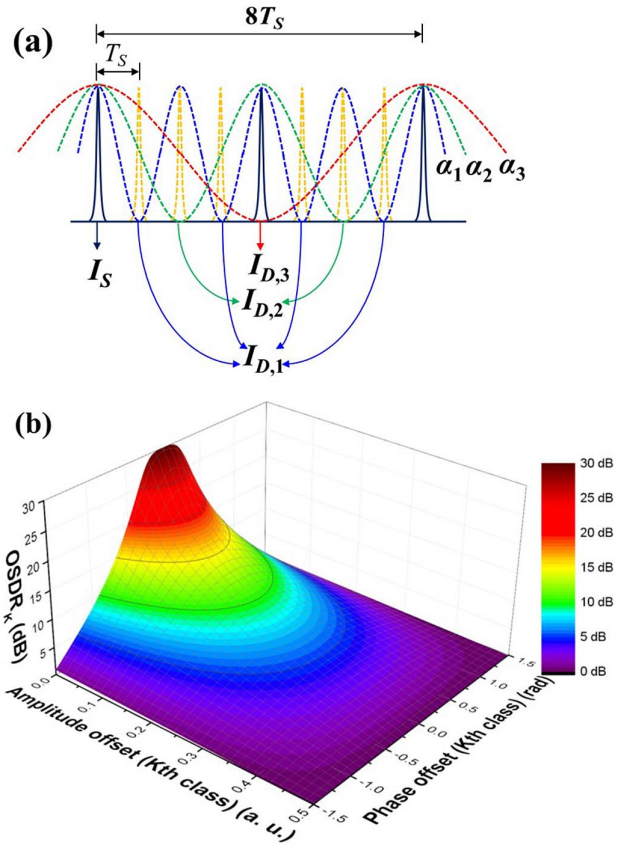

Fig. 2. (a) Schematic of the selected pulse and induced distortions in a three-class DOMZM-based demultiplexer. α_K is the switching response of one DOMZM in the Kth class (K = 1, 2, 3), I_S is the intensity of the selected pulse, and $I_{D,K}$ is the intensity of the distortions induced in the Kth class. (b) Simulated optical signal-to-distortion ratio (OSDR) at each single-class DOMZM versus both amplitude and phase offsets of the RF driver signal. The colors on the surface refer to the magnitude of the OSDR$_K$. The subscript K represents an integer, which can be 1, 2, or 3.

$$\mathrm{OSDR}=\left\{\sum_{K=1}^{3}\left[\prod_{L>K}^{3}(\alpha_{\max,L}/\alpha_{+,L})\times\mathrm{OSDR}_K^{-1}\right]\right\}^{-1}. \quad (7)$$

According to Eqs. (6) and (7), to achieve an optimized OSDR, each OSDR$_K$ should be maximized. Since $\alpha_{\max,K}$ and $\alpha_{\min,K}$ are inherent characteristics of DOMZMs, the demultiplexing modulation η_K ($t=0$) in Eq. (2) should be maximized in each class. It is obvious that the ideal condition can achieve the maximum OSDR, which is η_K ($t=0$) = 1, corresponding to $V_K = V_{\pi,K}/2$ and $\varphi_K = 0$.

To investigate the effect of the parameters of RF driver signals, their amplitude and phase can be normalized as

$$\Delta V_K = 0.5 - V_K/V_{\pi,K}, \qquad \Delta\varphi_K = 0 - \varphi_K, \quad (8)$$

where ΔV_K and $\Delta\varphi_K$ represent the offsets of V_K and φ_K from the ideal condition (i.e., $V_K = V_{\pi,K}/2$ and $\varphi_K = 0$), respectively. There $\Delta V_K = 0$ and $\Delta\varphi_K = 0$ in the ideal condition, where $\eta_K = 1$. Figure 2(b) shows a numerical result of OSDR$_K$ versus ΔV_K and $\Delta\varphi_K$ with a preset maximum of 30 dB. It indicates that OSDR$_K$ is closer to maximum when the offsets are smaller. In this sense, the amplitude and phase of the RF driver signals must be properly managed to optimize the demultiplexing performance.

3. RF Driver Design

As for the demultiplexer, a DOMZM (EOSpace AX-1x2-0MSS-40) of 40 GHz is used as the photonic switch working at 20 GHz in the first class. In the second class, two DOMZMs (EOSpace AX-1x2-0MSS-10) of 10 GHz working at 10 GHz are applied. In the third class, four DOMZMs (EOSpace AX-1x2-0MSS-10) of 10 GHz working at 5 GHz are adopted. According to the transmission curve of the DOMZMs, the AC half-wave voltages for each class are measured to be 5.8 V at 20 GHz, 5.1 V at 10 GHz, and 4.3 V at 5 GHz, respectively. The half-wave voltages are determined by the maximum and minimum output intensities of each DOMZM. As the match impedance is $R = 50\ \Omega$, the power at $\Delta V_K = 0$ in Eq. (8) should be $V_{\pi,K}^2/4R$, namely 19.3 dBm for the signal of 20 GHz in the first class, 18.2 dBm for each signal of 10 GHz in the second class, and 16.7 dBm for each signal of 5 GHz in the third class. As for the phase offset, the ideal condition $\Delta\varphi_K = 0$ can be determined by the intensity of the pulse, which is selected to pass and reaches its maximum. In practice, the channel-interleaved demultiplexer is not the only component that requires RF signals in the PADC system, as illustrated in Fig. 1. The AMLL should be seeded to generate the photonic sampling clock at 40 GHz. The EADCs should be triggered to perform the digitization at 5 GHz. All RF signals should be synchronized for coherence.

According to the requirements of RF signals, we design a microwave chain using commercial chips, as shown in Fig. 3(a). In this scheme, the chain adopts a signal of 20 GHz with a power of 0 dBm as the original input, which is divided into four paths by two-class cascaded 1×2 power splitters (PSs). For the first path, through an LNA (WFD180240-L17) and a frequency multiplier (FM, WBD220440-B2), a signal of 40 GHz with a maximum power of 14 dBm is achieved to seed the AMLL. The signal in the second path is directly amplified to 6 dBm by an LNA (WFD180240-L17) and then reaches the maximum power at 25 dBm by a PA (WFD196220-P25). It is used as the driver signal of 20 GHz in the first class. The frequency of the signal in the third path is first divided into 10 GHz by a frequency divider (FD, HMC492LP3). The signal is amplified to 18 dBm by an LNA (WFD060180-L18) and split into two outputs by a 1×2 PS (microstrip line), which is further amplified to 24 dBm in the maximum by PAs (WFD080120-P24) to drive the DOMZMs in the second class. As for the fourth path, the frequency of the signal is divided into 5 GHz by an FD (HMC493LP3). The signal splits into five outputs. Among them, four are amplified to 20 dBm in the maximum by LNAs (WFD020060-L10) and PAs (WFD020060-P26) in sequence for the DOMZMs in the third class, and one is amplified to 10 dBm by an LNA (WFD020060-L10) to serve as the trigger

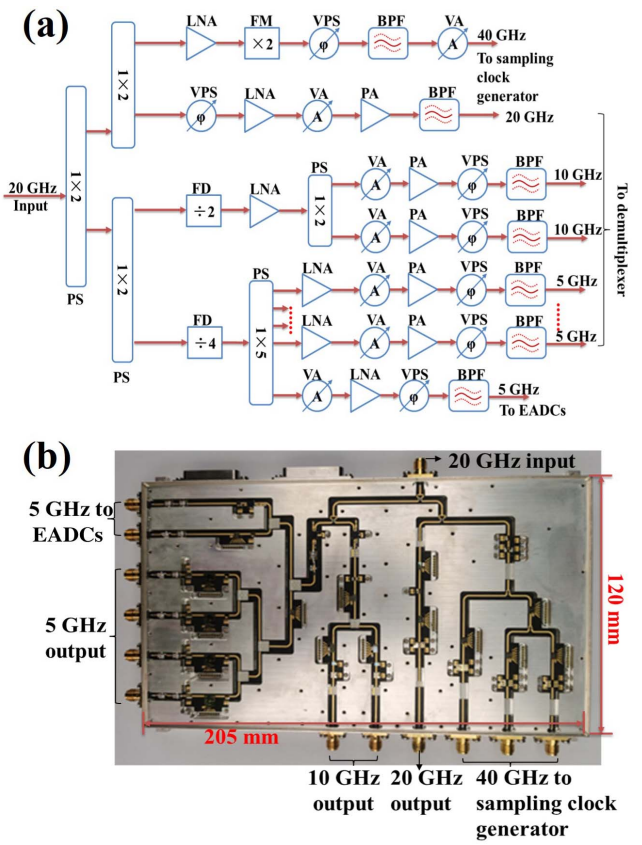

Fig. 3. (a) Design schematic of the microwave-chip-based RF driver and (b) its photo. PS, power splitter; LNA, low noise amplifier; PA, power amplifier; FM, frequency multiplier; FD, frequency divider; VA, variable RF attenuator; VPS, variable RF phase shifter; BPF, band-pass filter; EADC, electronic ADC.

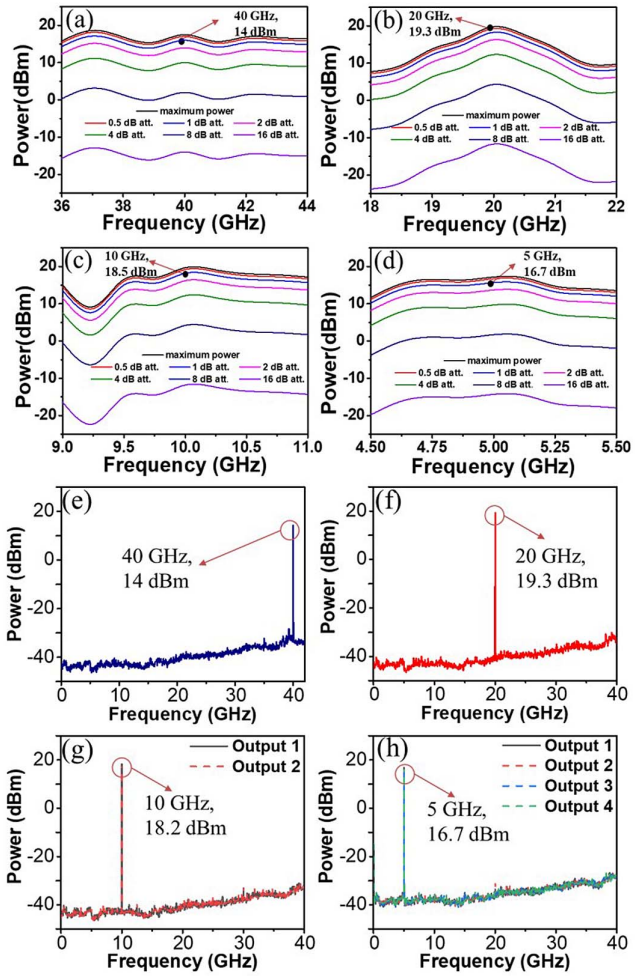

Fig. 4. (a)–(d) Typical frequency responses of the output ports of the RF driver module with different frequencies and different power. The adjustment precision in power is 0.5 dB and 6 bits. The working frequencies and power are marked as black dots. (e)–(h) The spectra of the output driver signal from the ports in (a)–(d). All plots are marked with the frequency and the power.

clock for the EADCs. Besides, all the output signals are filtered via band-pass filters (BPF), VAs, and VPSs, to guarantee good waveform and precise adjustment of both amplitude and phase of the output signals.

In implementation, the module includes a front board for RF components and a back board for DC bias. The metal box is used to support the boards and guarantee the performance under various conditions. The size of the module is 120 mm × 205 mm × 15 mm, as shown Fig. 3(b). It should be noted that there are three paths of seed signals of 40 GHz and two paths of the trigger clock at 5 GHz. The redundant outputs are reserved for the synchronization of peripherals in potential applications.

In terms of performance of the RF driver module, the input bandwidth is 18–22 GHz. Figures 4(a)–4(d) show the typical responses of the output ports of the RF driver module with different frequencies, which are measured by a spectrum analyzer (R&S FSW43). By adjusting the VAs, we can obtain different power. The effect in the phase shift can be observed from the results of the demultiplexer. The adjustment precisions in power and phase shifts are 0.5 dB (6 bits) and 5.6° (6 bits), respectively, depending on the specifications of VAs and VPSs. The spectra of generated RF signals after adjustments are measured, as shown in Figs. 4(e)–4(h). From these spectra, it can be found that the amplitudes of these signals can match well with the requirements of the demultiplexer. These spur-free spectra also indicate good sinusoidal temporal waveforms. In this situation, the power consumption of the module is 15.8 W.

4. Experiments

The RF driver module is further applied in a 40 GSa/s PADC for laboratory test. In this system, the AMLL (Calmar PSL-40-1 T) is successfully seeded by the RF driver to generate a sampling clock of 40 GSa/s, which is channel-interleaved by the demultiplexer based on three-class DOMZMs. The demultiplexing performance in each class is tested and optimized one by one based on the adjustment of the amplitude and phase of RF driver signals. Figure 5 shows the temporal waveforms of the demultiplexed series of each class under different conditions of RF

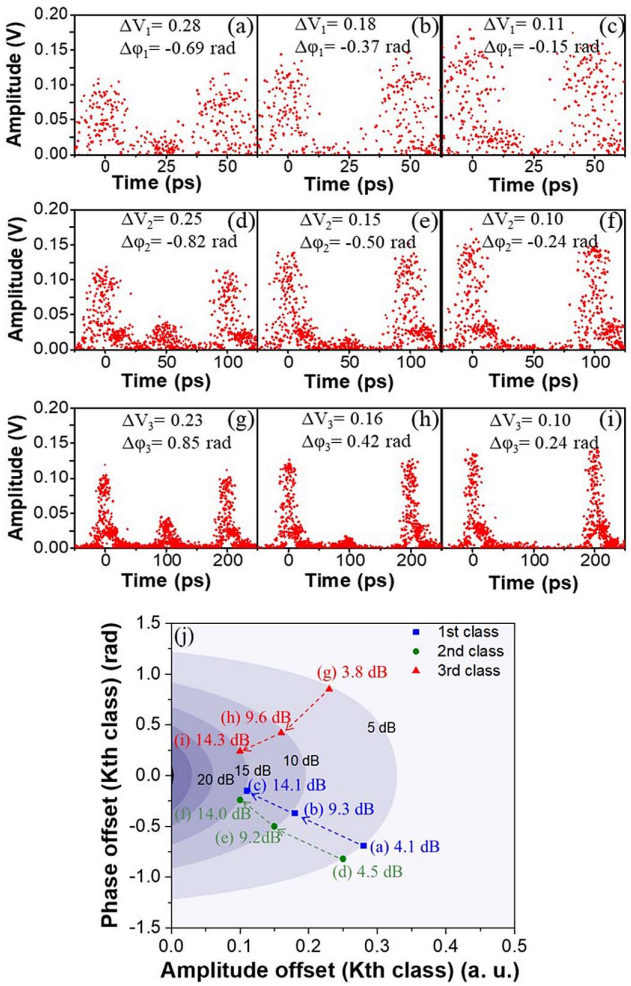

Fig. 5. Temporal waveforms of demultiplexed series from each class under different conditions of the amplitude and phase of RF driver signals in (a)–(c) first class, (d)–(f) second class, and (g)–(i) third class. (j) Comparison between the theoretically estimated and the experimentally measured $OSDR_K$ according to (a)–(i). The measured values are labeled, and the contours are based on the theoretical model.

driver signals. The waveforms are captured by a sampling oscilloscope (Agilent DCA-X 86100D). Only one channel is illustrated as a representative of each class. It can be found that the series of 40 GSa/s is demultiplexed into series of 20 GSa/s, 10 GSa/s, and 5 GSa/s after each class, respectively. In Figs. 5(a)–5(i), the amplitude and phase offsets of RF driver signals in each class are marked along with the measured waveforms. To evaluate the demultiplexing performance in each class, the $OSDR_K$ can be calculated with the measured peak intensity of the pulses in Figs. 5(a)–5(i) according to the definition in Eq. (6). The theoretical estimation can also be derived from Eq. (6) based on the amplitude and phase offsets. Figure 5(j) depicts the $OSDR_K$ in each class, which are calculated from the waveforms in Figs. 5(a)–5(i). Note that the maximum and minimum transmittances of DOMZMs are 0.5 dB and 25 dB, respectively. The theoretical estimations are derived from Eq. (6) and compared with the experimentally measured results.

From Fig. 5(j), it can be found that the values of $OSDR_K$ increase from ~5 dB to ~15 dB in all three classes along with suppressed amplitude and phase offsets. The feasibility of the theoretical analysis in Eq. (6) can be verified from the consistence between the measured and estimated results. Furthermore, the final demultiplexed 5 GSa/s series under different conditions of amplitude and phase of the RF driver signals applied in each class [i.e., the cases shown in Figs. 5(a)–5(i)] are depicted in Fig. 6. The values of OSDRs are calculated from the waveforms and compared with their estimation derived from Eq. (7) based on the values of $OSDR_K$ in each class. A good consistence also verifies the analysis in Eq. (7). In these cases, Fig. 6(a) depicts the temporal waveforms of final demultiplexed series with $OSDR_1$, $OSDR_2$, and $OSDR_3$ according to Figs. 5(a), 5(d), and 5(g), respectively. Similarly, Fig. 6(b) depicts the temporal waveforms of final demultiplexed series according to Figs. 5(b), 5(e), and 5(h). Figure 6(c) depicts the temporal waveforms of the final demultiplexed series according to Figs. 5(c), 5(f), and 5(i). The OSDR of the final demultiplexed series increases with the $OSDR_K$ in each class, as shown in Figs. 6(a)–6(c). The best measurable OSDR of the final demultiplexed series after three classes

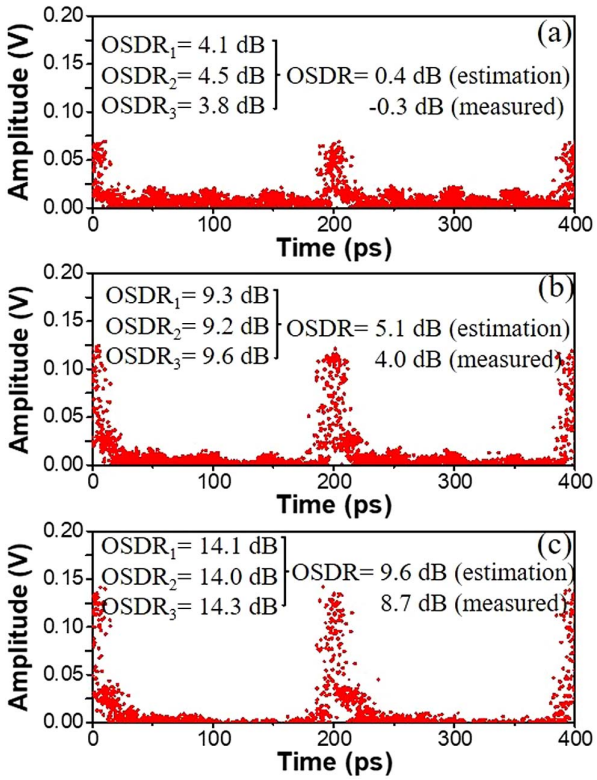

Fig. 6. Temporal waveforms of final demultiplexed 5 GSa/s series under the conditions depicted in Figs. 5(a)–5(i) in each class: (a) Fig. 5(a) as the first class, Fig. 5(d) as the second class, and Fig. 5(g) as the third class; (b) Fig. 5(b) as the first class, Fig. 5(e) as the second class, and Fig. 5(h) as the third class; (c) Fig. 5(c) as the first class, Fig. 5(f) as the second class, and Fig. 5(i) as the third class. The $OSDR_K$ in each class is labeled as depicted in Fig. 5(j). The final OSDR is measured and compared with its theoretical estimation, which increases along with the $OSDR_K$ in each class.

of DOMZMs reaches ~10 dB with a voltage detection precision of ~17 mV. Furthermore, the precision can be further improved by eliminating the noise with ultra-high-speed real-time oscilloscopes through heterodyne detection and the averaging method. Without an EADC, the OSDR is considered as the most effective parameter to evaluate the performance of the demultiplexer. As the OSDR increases, the improvement in the performance of the PADC can be evaluated by the effective number of bits (ENOB). The relationship between the OSDR and the ENOB will be studied in future research.

5. Conclusion

A microwave-chip-based coherent multi-frequency RF driver module is developed and applied to the channel-interleaved demultiplexer in a PADC system of 40 GSa/s. We theoretically analyze the relationship between the characteristics of generated RF driver signals and demultiplexing performance. In laboratory test, a beam sampling series of 40 GSa/s is converted into eight parallel channels of 5 GSa/s with RF driver signals, which drive the photonic switches. By precisely adjusting the amplitude and phase of these signals, the OSDR is optimized. The results verify the compatibility between the RF driver and the PADC system. With its compact size, the RF driver is considered as one step towards practical application and the next-generation of PADC systems in a module or on a chip.

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References

1. G. C. Valley, "Photonic analog-to-digital converters," Opt. Express **15**, 1955 (2007).
2. P. W. Juodawlkis, J. C. Twichell, G. E. Betts, J. J. Hargreaves, R. D. Younger, J. L. Wasserman, F. J. O'Donnell, K. G. Ray, and R. C. Williamson, "Optically sampled analog-to-digital converters," IEEE Trans. Microwave Theroy Tech. **49**, 1840 (2001).
3. Y. Han and B. Jalali, "Photonic time-stretched analog-to-digital converter: fundamental concepts and practical considerations," J. Lightwave Technol. **21**, 3085 (2003).
4. A. Khilo, S. J. Spector, M. E. Grein, A. H. Nejadmalayeri, C. W. Holzwarth, M. Y. Sander, M. S. Dahlem, M. Y. Peng, M. W. Geis, N. A. DiLello, J. U. Yoon, A. Motamedi, J. S. Orcutt, J. P. Wang, C. M. Sorace-Agaskar, M. A. Popović, J. Sun, G. Zhou, H. Byun, J. Chen, J. L. Hoyt, H. I. Smith, R. J. Ram, M. Perrott, T. M. Lyszczarz, E. P. Ippen, and F. X. Kärtner, "Photonic ADC: overcoming the bottleneck of electronic jitter," Opt. Express **20**, 4454 (2012).
5. T. R. Clark, J. U. Kang, and R. D. Esman, "Performance of a time- and wavelength-interleaved photonic sampler for analog-digital conversion," IEEE Photon. Technol. Lett. **11**, 1168 (1999).
6. R. Williamson, P. Juodawlkis, J. Wasserman, G. Betts, and J. Twichell, "Effects of crosstalk in demultiplexers for photonic analog-to-digital converters," J. Lightwave Technol. **19**, 230 (2001).
7. G. Yang, W. Zou, L. Yu, K. Wu, and J. Chen, "Compensation of multi-channel mismatches in high-speed high-resolution photonic analog-to-digital converter," Opt. Express **24**, 24061 (2016).
8. H. Zhang, W. Zou, G. Yang, and J. Chen, "Dual-output modulation in time-wavelength interleaved photonic analog-to-digital converter based on actively mode-locked laser," Chin. Opt. Lett. **14**, 030602 (2016).
9. G. Yang, W. Zou, Y. Yuan, and J. Chen, "Wideband signal detection based on high-speed photonic analog-to-digital converter," Chin. Opt. Lett. **16**, 030601 (2018).
10. F. Yang, W. Zou, L. Yu, S. Xu, and J. Chen, "Impact of optical–electrical conversion responsivity in sub-sampled photonic analog-to-digital converter," Chin. Opt. Lett. **17**, 040602 (2019).
11. K. Zheng, W. Zou, L. Yu, N. Qian, and J. Chen, "Stability optimization of channel-interleaved photonic analog-to-digital converter by extracting of dual-output photonic demultiplexing," Chin. Opt. Lett. **18**, 012502 (2020).
12. S. Xu, X. Zou, B. Ma, J. Chen, L. Yu, and W. Zou, "Deep-learning-powered photonic analog-to-digital conversion," Light: Sci. Appl. **8**, 41377 (2019).
13. R. Wang, S. Xu, J. Chen, and W. Zou, "Ultra-wideband signal acquisition by use of channel-interleaved photonic analog-to-digital converter under the assistance of dilated fully convolutional network," Chin. Opt. Lett. **18**, 123901 (2020).
14. G. Yang, W. Zou, X. Li, and J. Chen, "Theoretical and experimental analysis of channel mismatch in time-wavelength interleaved optical clock based on mode locked laser," Opt. Express **23**, 2174 (2015).
15. F. Scotti, F. Laghezza, S. Pinna, P. Ghelfi, and A. Bogoni, "High precision photonic ADC with four time-domain-demultiplexed interleaved channels," in *OptoElectronics and Communications Conference and Photonics in Switching* (Optical Society of America, 2013), paper TuO1_3.
16. G. Yang, W. Zou, L. Yu, and J. Chen, "Investigation of electronic aperture jitter effect in channel-interleaved photonic analog-to-digital converter," Opt. Express **27**, 9205 (2019).
17. L. Yu, W. Zou, G. Yang, X. Li, and J. Chen, "Switching response of dual-output Mach–Zehnder modulator in channel-interleaved photonic analog-to-digital converter," Chin. Opt. Lett. **16**, 120602 (2018).
18. N. Qian, L. Yu, J. Chen, and W. Zou, "Influence of the demultiplexer on channel-interleaved photonic analog-to-digital converters," IEEE Photon. J. **12**, 5502110 (2020).
19. R. Gugulothu, S. V. Bhalke, A. A. Naik, K. Lalkishore, and R. Dasari, "Multichip module based GaAs MMICs packaging for L-band high gain application," in *IEEE MTT-S International Microwave and RF Conference* (IEEE Press, 2019), p. 1.
20. Y. Zhang, S. Shi, R. Martin, A. Wright, P. Yao, K. Shreve, C. Harrity, and D. Prather, "Packaging of high-gain multichip module in multilayer LCP substrates at W-band," IEEE Trans. Compon. Packag. Manuf. Technol. **7**, 1655 (2017).