Integrated optoelectronic chip pair for transmitting and receiving optical signals simultaneously

Kai Liu (刘 凯)*, Qi Wei (位 祺), Yongqing Huang (黄永清), Xiaofeng Duan (段晓峰), Qi Wang (王 琦), Xiaomin Ren (任晓敏), and Shiwei Cai (蔡世伟)

State Key Laboratory of Information Photonics and Optical Communications, Beijing University of Posts and Telecommunications, Beijing 100876, China

**Corresponding author: kliu@bupt.edu.cn*

Received November 1, 2018; accepted January 15, 2019; posted online April 3, 2019

An integrated optoelectronic chip pair, which can transmit and receive optical signals simultaneously, is proposed in this Letter. The design and optimization of its key structure, the vertical cavity surface emitting laser's distributed Bragg reflector, are presented. Analysis is also done for its influence on the integrated chip's performance. Moreover, the chip pair's performance under dynamic conditions is analyzed. Their 3 dB modulation bandwidths are higher than 10 GHz, and their 3 dB photo-response bandwidths are around 23 GHz. Their applications will further improve the performances of the optical interconnects.

OCIS codes: 130.3120, 130.0250, 250.7260, 230.5160.
doi: 10.3788/COL201917.041301.

In recent years, ultra-wideband applications, such as cloud computing, big data services, and 5G wireless systems, have been developing rapidly. They are requiring more and more network capacity, especially in the field of information interconnects in and among the data centers[1]. Moreover, to fulfill the ever-increasing demand for reducing network power consumptions, increasing signal transmission bandwidth, and extending information exchanging distance, the optical interconnects are now the most efficient solution for it[2]. Such optical links are constructed with optoelectronic devices, like vertical cavity surface emitting laser (VCSEL)[3,4] and positive-intrinsic-negative (PIN) photodetector (PD)[5]. Among these optoelectronic devices, VCSEL is the most utilized transmitting device for short distance (less than 300 m) optical interconnects in data centers due to its benefits of low power consumption, high modulation speed, and high coupling efficiency to multimode fibers[6]. To further increase the integration level of the optical transceiver at such an optical links end, some attempts of integrating light emitting and detecting functions into one single chip have also been made based on the VCSEL[7–11]. On the basis of these works, we proposed a pair of monolithically, vertically, and coaxially integrated optoelectronic chips for transmitting and receiving optical signals simultaneously and improving the optical interconnects' transceiving performance[12]. They are both constructed by integrating a VCSEL on top of a PIN-PD, as shown in Fig. 1, and are designed for working under the wavelength division multiplexing (WDM) scheme, which means the transmitting/receiving wavelength will be set at 850/805 nm for one chip and at 805/850 nm for the other chip correspondingly. To realize such a WDM working scheme, the key problem to solve is the special structure design of the distributed Bragg reflectors (DBRs) that form the VCSEL's cavity. In this Letter, we will analyze the effects of the specially designed VCSEL's DBR on the integrated chip's static performance. Then, the input light's influence on the integrated chip's specially designed VCSEL unit will be analyzed. Moreover, the dynamic performances of the integrated chips are simulated.

The special structure of the VCSEL's DBR is constructed by inserting a $\lambda/4$ DBR, which has its central reflection wavelength λ setting at the chip's transmitting wavelength and has a high reflectivity of higher than 99%, into a low Q value resonant cavity, which has its resonant wavelength setting at the chip's receiving wavelength. Then, the low Q cavity is optimized for making the corresponding VCSEL's DBR obtain high transmittivity around the chip's receiving wavelength. With such specially designed VCSEL's DBRs, the integrated chip pairs' optical structures can be designed and optimized.

The design and optimization of the VCSEL's DBR are conducted by applying the optical thin film transfer matrix method[13]. Both VCSEL's DBRs are composed of alternately grown $Al_{0.15}Ga_{0.85}As/Al_{0.9}Ga_{0.1}As$ layers. For the chip emitting light around 850 nm, its top DBR is

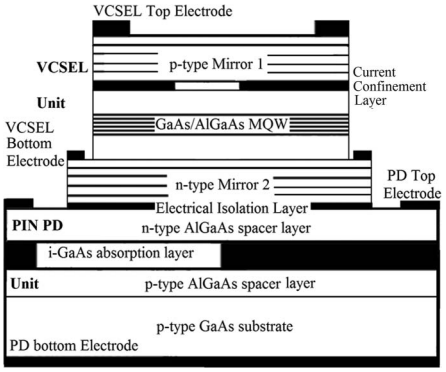

Fig. 1. Structure of the proposed integrated optoelectronic chip.

composed of 20 pairs of $\lambda/4$ DBR with $\lambda = 850$ nm, and its low Q cavity is constructed by a reflector formed by the semiconductor/air interface and a reflector formed by two pairs of $\lambda_0/4$ DBR with $\lambda_0 = 805$ nm; the low Q cavity length will be optimized and results will be shown below. Its bottom DBR is composed of 28 pairs of $\lambda/4$ DBR with $\lambda = 850$ nm, and its low Q cavity is constructed by a reflector formed by one pair of $\lambda_0/4$ DBR and another reflector formed by two pairs of $\lambda_0/4$ DBR with $\lambda_0 = 805$ nm; the low Q cavity length will be optimized and results will be shown below. For the chip emitting light around 805 nm, its VCSEL's DBR structure is the same as that stated above. The difference is only that of $\lambda = 805$ nm and $\lambda_0 = 850$ nm.

The reflection spectra of the VCSEL's DBR around their optimized low Q cavity parameters are shown in Figs. 2 and 3. Figure 2 shows the reflection spectra of the VCSEL's top DBR and its bottom DBR for the chip emitting at a wavelength around 850 nm. From it, we can find that, when the DBR's low Q cavity length changes from −5% to +5% from its original value, it has little effect on the DBR's reflectivity around 850 nm. The major influence is on the 805 nm wavelength range, which shows that when the changes are forwarding to the positive part, the performance deterioration is less than in the case forwarding to the negative part. Figure 3 shows the reflection spectra of the VCSEL's top DBR and its bottom DBR for the chip emitting at a wavelength around 805 nm. From it, we can find that, when the DBR's low Q cavity length changes from −5% to +5% from its original value, it results in a decrement of the top DBR's reflectivity around 805 nm, while the changes are forwarding to the negative part. But, the bottom DBR's performance is almost not influenced. For this chip, its performance on the receiving wavelength range has less deterioration when the changes are forwarding to the negative part than when those are forwarding to the positive part.

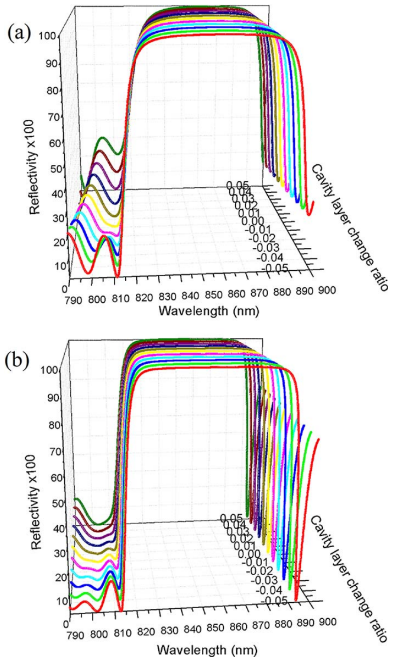

Fig. 2. Reflection spectra of the (a) top DBR and (b) bottom DBR that form the integrated chip, which emits light at a wavelength around 850 nm and receives light at a wavelength around 805 nm. In these figures, the length of the low Q cavity changes from −5% to +5% from its original value.

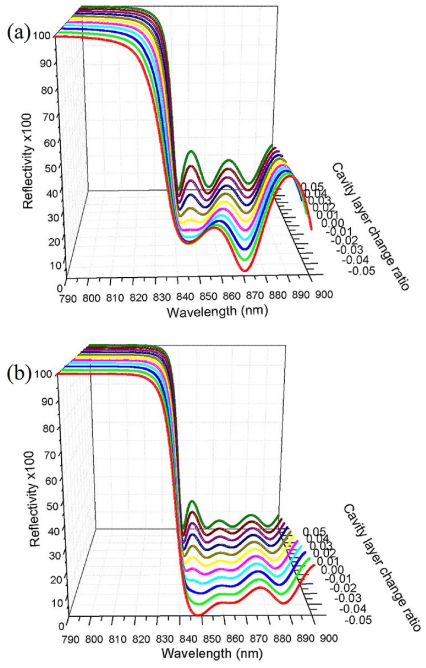

Fig. 3. Reflection spectra of the (a) top DBR and (b) bottom DBR that form the integrated chip, which emits light at a wavelength around 805 nm and receives light at a wavelength around 850 nm. In these figures, the length of the low Q cavity changes from −5% to +5% from its original value.

In the device performance simulation, the effective frequency method[14] and self-consistent two-dimensional model[15] were used. The material parameters were taken from Ref. [15]. The chip's structure size used for simulation is described below. The chip's VCSEL mesa is set with a radius of 13 μm, and its Al_2O_3 current confinement layer is wet oxidizing transferred from a layer of $Al_{0.96}Ga_{0.04}As$ with a 6 μm aperture in the center. The size of its PIN-PD unit is set with a radius of 25 μm. The electrodes of its VCSEL unit and its PIN-PD unit are set as shown in Fig. 1. The VCSEL unit's bottom electrode and the PIN-PD unit's top electrode are set to contact the ground.

As stated, the VCSEL's DBR parameters will have effect on the integrated chip's performance. For different chips in the chip pair, the effect is different. Thus, we will first verify such effects with device performance simulations.

Firstly, the effect on the VCSEL units' static performance is simulated, and results are shown in Fig. 4. The VCSEL units are forward biased at a current changing from 0 mA to around 5.0 mA. The VCSEL DBR's low Q cavity length changes from −3% to +3% from its

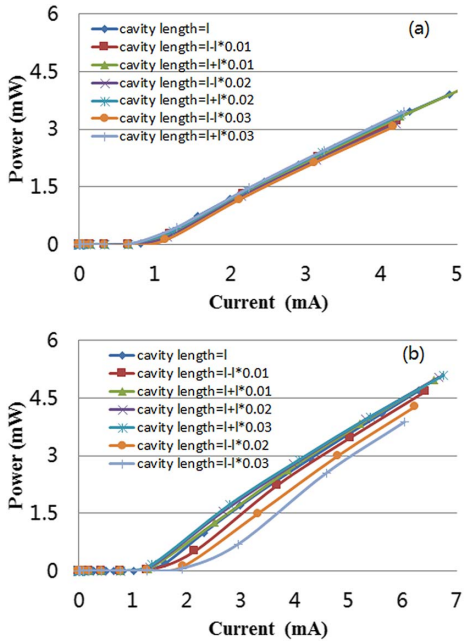

Fig. 4. VCSEL units' static performances: (a) the chip transmitting light at a wavelength around 850 nm; (b) the chip transmitting light at a wavelength around 805 nm.

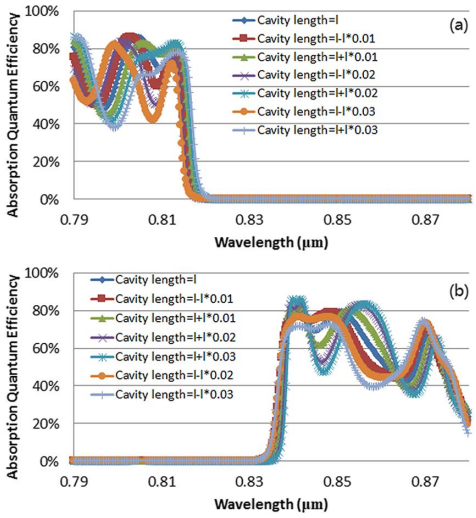

Fig. 5. Spectral photo-response performances of the integrated chip pairs: (a) the chip transmitting light around a wavelength of 850 nm and receiving light at a wavelength around 805 nm; (b) the chip transmitting light around a wavelength of 805 nm and receiving light at a wavelength around 850 nm.

original value. From Fig. 4, it can be drawn that, within the low Q cavity length changing range, the performance of the VCSEL unit emitting light at a wavelength around 850 nm remains stable, and the lasing wavelength is 848.1 nm with the original low Q cavity length. But, the performance of the VCSEL unit emitting light at a wavelength around 805 nm, where the lasing wavelength is 805.3 nm with the original low Q cavity length, is quite different. When the low Q cavity length is changing to the positive part, the VCSEL unit's performance is keeping stable. On the other hand, when the low Q cavity length is changing to the negative part, the VCSEL unit's performance deteriorates. The threshold current increases with the decreasing low Q cavity length. This can be explained by its VCSEL's DBR performance. As shown in Fig. 3(a), when its low Q cavity length is reduced, its top DBR's reflectivity is also reduced at a wavelength around 805 nm. However, when its low Q cavity length is increased, its top DBR's reflectivity is staying stable.

Secondly, the spectral photo-response performances of the integrated chip pairs are simulated. Here, the input light intensity is set to be 10 W/cm^2, and its wavelength is set, changing from 0.79 to 0.88 μm; the VCSEL unit is biased at 1.9 V (above the threshold conditions), and the PIN-PD unit is biased at −5 V. The obtained absorption quantum efficiency (AQE) spectra of the integrated chip pairs are shown in Fig. 5. For the integrated chip receiving light at a wavelength around 805 nm, as shown in Fig. 5(a), its AQE performance is better when the low Q cavity length is increased than when it is reduced. It coincides with the performance of its VCSEL's DBR. When the low Q cavity length changing range is between 0 and 3% from its original value, the absorption range remains wider than 12 nm for its AQE higher than 60%. For the integrated chip receiving light at a wavelength around 850 nm, its AQE performance is better when the low Q cavity length is reduced than when it is increased. It also coincides with the performance of its VCSEL's DBR. When the low Q cavity length changing range is between −3% and 0 from its original value, the absorption range remains wider than 15 nm for its AQE higher than 60%.

Next, to evaluate the influence of the input light intensity on the VCSEL unit's performance, the rate equation of the VCSEL unit's carrier will be used, as shown in Eq. (1)[16]. Since there is extra input light from outside, then Eq. (1) should be modified to Eq. (2):

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \eta_i \frac{I}{qV} - R_{\mathrm{sp}} - R_{\mathrm{nr}} - g\nu_g N_p, \tag{1}$$

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \eta_i \frac{I}{qV} - R_{\mathrm{sp}} - R_{\mathrm{nr}} - g\nu_g N_p + B_{12}N_{\mathrm{in}}. \tag{2}$$

Considering static working conditions, then Eq. (2) can be modified to Eq. (3):

$$I = (R_{\mathrm{sp}} + R_{\mathrm{nr}} + g\nu_g N_p - B_{12}N_{\mathrm{in}})\frac{qV}{\eta_i}. \tag{3}$$

In these equations, η_i is the current injection efficiency, I is the VCSEL unit's electrode current, q is the electronic charge, V is the active region volume, R_{sp} is the spontaneous recombination rate, R_{nr} is the nonradiative recombination rate, $g\nu_g N_p$ is the stimulated recombination rate of the carriers, and $B_{12}N_{\mathrm{in}}$ is the absorption rate of the input light. From Eq. (3), it can be concluded that, if the VCSEL unit is not biased or biased just around the threshold, then a current with a negative value will be

generated at its electrode. It means that the photo-response current of the VCSEL unit is drawn out. But, if the VCSEL unit is biased high above the threshold, then a current with a positive value will be generated at its electrode. It means that the input light is optically pumping the VCSEL now. The simulation results prove the analysis and are shown in Fig. 6. The optically pumped VCSEL unit's performance of the integrated chip pairs by the input light is shown in Fig. 7. It shows that, for both chips, even when the input light intensity is as high as 1000 W/cm^2 (corresponding to an input light power 19.6 mW), the optically pumped VCSEL unit's output light power is less than 0.18 μW. Corresponding to the 3 mW VCSEL unit's electrically pumped output power, the optical isolation level is larger than 40 dB.

Moreover, based on the optimized integrated chip pairs, the dynamic performances are simulated. For such simulations of the PIN-PD units, they are both biased at a voltage −5 V. A static input light intensity of 450 W/cm^2 (corresponding to an input light power of 9 mW) is set for static optical signal biasing. The small AC input light intensity is set to be 150 W/cm^2 (corresponding to an input light power of 3 mW), and its frequency is set, changing from 1 MHz to 100 GHz. Under such conditions, the PIN-PD units obtain a 3 dB bandwidth of about 23 GHz, as shown in Fig. 8. The electric isolation capability between the chip pairs' VCSEL units and their PIN-PD units is deducted here by comparing the VCSEL units' photo-response currents with the PIN-PD units' photo-response currents. Results are shown in Fig. 9. It can be concluded that, when the isolation level is set to be −40 dB, the chip receiving light at 848.1 nm obtains an isolation bandwidth up to 10.9 GHz, while the chip receiving light at 805.3 nm obtains an isolation bandwidth up to 15.5 GHz.

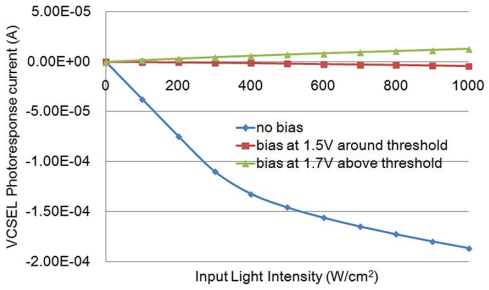

Fig. 6. Photo-response performances of the VCSEL unit with different input light intensities changing from 0 to 1000 W/cm^2, while the VCSEL is not biased or biased at 1.5 and 1.7 V.

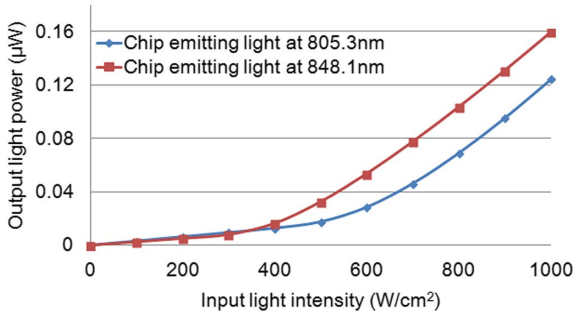

Fig. 7. Optically pumped VCSEL unit's performance of the integrated chip pairs by the input light.

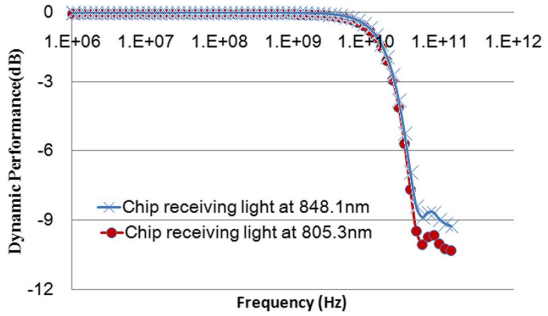

Fig. 8. Simulated PIN-PD units' dynamic performances of the integrated chip pairs.

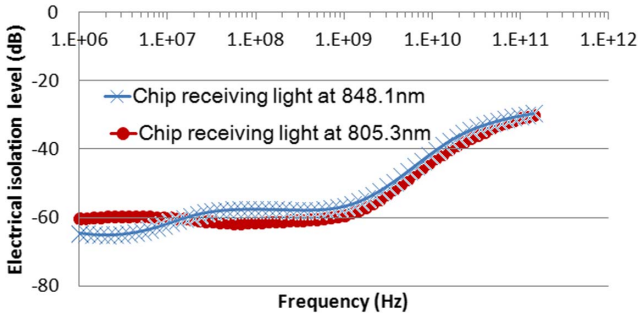

Fig. 9. Electric isolation capability between the chip pairs' VCSEL units and their PIN-PD units deducted from the PIN-PD units' dynamic performance analysis by comparing the VCSEL units' photo-response currents with the PIN-PD units' photo-response currents.

For analyzing the dynamic performance of the chip pairs' VCSEL units, they are biased at 1.75 V (848.1 nm VCSEL) and 1.8 V (805.3 nm VCSEL), respectively. The dynamic performance analysis is conducted by applying a pulse voltage of 0.1 V on the VCSEL and analyzing the fast Fourier transform of its pulsed photo-response signal, respectively. The VCSEL unit emitting light at 848.1 nm obtains a 3 dB bandwidth of about 15.1 GHz, while another VCSEL emitting light at 805.3 nm obtains a 3 dB bandwidth of about 10.2 GHz, as shown in Fig. 10. The electrical isolation capabilities between the chip pairs' VCSEL units and their PIN-PD units are deducted by comparing the PIN-PD units' photo-response currents with the VCSEL units' driving currents under different frequencies, as shown in Fig. 11. From it, it can be concluded that, when the isolation level is set to be −40 dB, the chips emitting light at 848.1 or 805.3 nm both obtain an isolation bandwidth up to 30 GHz. With such an isolation level of −40 dB, if the AC modulation amplitude of the VCSEL unit's driving signal is 2 mA, then a corresponding optical noise level of less than −28 dBm will be generated to the PIN-PD unit.

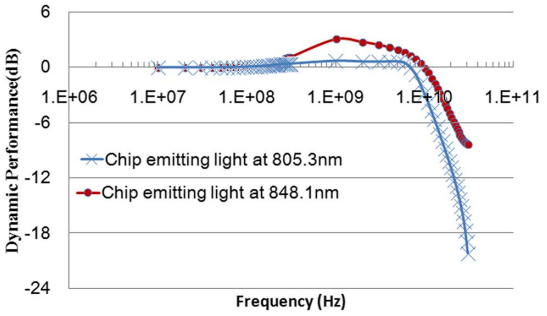

Fig. 10. Simulated VCSEL units' dynamic performances of the integrated chip pairs.

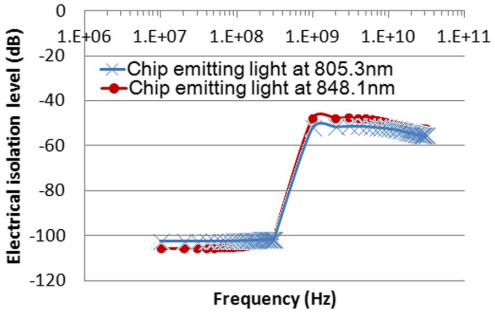

Fig. 11. Electric isolation capability between the chip pairs' VCSEL units and their PIN-PD units deducted from the VCSEL units' dynamic performance analysis by comparing the PIN-PD units' photo-response currents with the VCSEL units' driving currents.

As mentioned above, integrated optoelectronic chip pairs, which can transmit and receive optical signals simultaneously, are proposed. The design and optimization of its key structure, the low Q cavity VCSEL's DBR, are presented. Its effect on the integrated chips' static performance is analyzed. For the chip transmitting light at a wavelength around 850 nm, its performance will remain stable, while its low Q cavity length is increased. On the contrary, the chip, which transmits light at a wavelength around 805 nm, has a stable receiving performance, while its low Q cavity length is reduced, but its transmitting performance is stable, while its low Q cavity length is increased, due to the influence of its top VCSEL's DBR. Further optimization on it would be required. For both chips, their absorption wavelength range is wider than 10 nm if an AQE higher than 60% is required. Furthermore, the influence of the input light intensity on the performance of the integrated chip's VCSEL unit is analyzed, and conclusions are made. Under common working conditions, such effects can be ignored due to the obtained optical isolation level of higher than 40 dB. Moreover, under dynamic working conditions, the VCSEL unit emitting light at 848.1 nm (805.3 nm) obtains a 3 dB bandwidth of about 15.1 GHz (10.2 GHz); both PIN-PD units obtain 3 dB bandwidths of about 23 GHz. With a bandwidth range up to 30 GHz, the two composing units of the integrated chip pairs are electrically isolated with an isolation level of −40 dB. So, the two units of the proposed integrated optoelectronic chip pairs can work independently from each other as designed, both optically and electrically. Compared with other integrated transceiver schemes proposed by other research groups[7–11], which are either integrating VCSELs and PDs laterally or packaging VCSELs and PDs vertically, the monolithically vertical and coaxial integration scheme proposed in this Letter will have better thermal performance and can simplify the chip's future coupling scheme to a multimode fiber, while being used for applications of bi-directional full-duplex optical interconnects in a single fiber and lowering the packaging cost at the same time. The proposed chip pairs can be applied for further performance improvements of optical interconnect systems.

This work was supported by the National Natural Science Foundation of China (Nos. 61874147, 61574019, 61674020, and 61674018), the Fund of State Key Laboratory of Information Photonics and Optical Communications (No. IPOC2016ZT10), the Specialized Research Fund for the Doctoral Program of Higher Education of China (No. 20130005130001), and the 111 Project (No. B07005).

References

1. S. Elby, in *Optical Fiber Communication Conference*, 2015 OSA Technical Digest Series (Optical Society of America, 2015), paper Tu2H.5.
2. M. Fayyaz and K. Aziz, in *Proceedings of 12th International Conference on Frontiers of Information Technology* (2014), p. 61.
3. P.-K. Shen, C.-T. Chen, and C.-H. Chang, IEEE Photon. J. **6**, 2500310 (2014).
4. H. Qiu, Z. Wu, T. Deng, Y. He, and G. Xia, Chin. Opt. Lett. **14**, 021401 (2016).
5. H. Nasu, T. Kise, K. Nagashima, and N. Nishimura, in *European Conference on Optical Communication (ECOC)* (2014), paper Tu.4.5.2.
6. C. Xie, in *Asia Communications and Photonics Conference (ACP)* (2015), paper ASu4C.1.
7. R. Rivers, K. Komirisetty, and D. Geddis, in *Photonics Conference IEEE* (2014), paper TuB2.4.
8. N. Jogan, J. Hayakawa, T. Kondo, A. Murakami, J. Sakurai, X. Gu, and F. Koyama, in *IEEE International Semiconductor Laser Conference (ISLC)* (2016), paper WE9.
9. A. Kern, A. Al-Samaneh, D. Wahl, and R. Michalzik, IEEE J. Sel. Top. Quantum Electron. **19**, 6100313 (2013).
10. T. Maier, G. Strasser, and E. Gornik, IEEE Photon. Technol. Lett. **12**, 119 (2000).
11. J. W. Shi, F. M. Kuo, T. C. Hsu, Y. J. Yang, A. Joel, M. Mattingley, and J. I. Chyi, IEEE Photon. Technol. Lett. **21**, 1444 (2009).
12. K. Liu, H. Fan, Y. Huang, X. Duan, Q. Wang, X. Ren, Q. Wei, and S. Cai, Chin. Opt. Lett. **16**, 091301 (2018).
13. K. Liu, Y. Huang, and X. Ren, Proc. SPIE **3532**, 122 (1999).
14. H. Wenzel and J. Wunsche, IEEE J. Quantum Electron. **33**, 1156 (1997).
15. Z.-M. Li, K. M. Dzurko, A. Dellge, and S. P. McAlister, IEEE J. Quantum Electron. **28**, 1209 (1992).
16. C. Wilmsen, H. Temkin, and L. Coldren, *Vertical-Cavity Surface-Emitting Lasers* (Cambridge University, 1999).