

Compact phase-lock loop for external cavity diode lasers

Chunhua Wei (魏春华)^{1,2}, Shuhua Yan (颜树华)^{1,2,*}, Aiai Jia (贾爱爱)^{1,2},
Yukun Luo (罗玉昆)^{1,2}, Qingqing Hu (胡青青)^{1,2}, and Zehuan Li (厉泽环)^{1,2}

¹Department of Instrument Science and Technology, College of Mechatronic Engineering and Automation,
National University of Defense Technology, Changsha 410073, China

²Interdisciplinary Center for Quantum Information, National University of Defense Technology,
Changsha 410073, China

*Corresponding author: yanshuhua996@163.com

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We present a compact, low-noise, and inexpensive optical phase-lock loop (OPLL) system to synchronize the frequency and the phase between two external cavity diode lasers. Based on a direct digital synthesizer technique, a programmable radio-frequency generator is implemented as the reference signal source. The OPLL has a narrow beat note linewidth below 1 Hz and a residual mean-square phase error of 0.06 rad² in a 10 MHz integration bandwidth. The experimental test results prove the competent performance of the system, which is promising as a low-budget choice in atomic physics applications.

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Phase-coherent lasers play an important role in many atomic physics experiments, such as high-resolution atomic spectroscopy^[1,2], quantum communication^[3], Raman velocity selection^[4], and atom interferometry^[5]. Especially in atom interferometry, Raman pulses are generated with phase-coherent lasers. If the required frequency difference is relatively small, the phase coherence between laser beams can easily be produced by directly diffracting a single laser with an acousto-optic or an electro-optic modulator to shift its frequency while conserving the phase. However, when the required frequency difference increases past the gigahertz level, it is often preferable to use two separate sources. In this case, an optical phase-lock loop (OPLL) is introduced to synchronize the phase between two individual lasers^[6,7]. Based on this method, the frequency difference of the two lasers is tunable up to several gigahertz^[8,9].

In the last two decades, a number of OPLL designs have been proposed and implemented^[10–15]. In 1995, Freearge *et al.* reported a simple model for use in the design of phase-lock loops for diode lasers. In 2008, Guo *et al.*^[16] reported an OPLL to lock external cavity diode lasers (ECDLs) with a frequency difference up to 9.2 GHz while remaining phase locked. In 2012, Lu *et al.*^[17] reported a digital OPLL based on a field-programmable gate array (FPGA). However, most of these schemes require expertise in microwave frequency electronics as well as expensive equipment to generate stable microwave-range reference signals. At present, there are many commercially available microwave-range generators on the market, but these generators are generally of large size and high cost.

In this Letter, we present a compact, low-noise, and digital OPLL with two ECDLs. The OPLL presented here is made from inexpensive off-the-shelf components. Compared with the method of frequency mixing, we chose a divider to down-convert the beat note signal and design

an ultra-low phase noise radio-frequency (RF) generator as the reference signal. In this way, we avoided the use of an extra commercial microwave and RF generator. The whole cost of the OPLL board and reference signal board is less than 700 dollars. In order to test the performance of our OPLL, we lock a slave laser (SL) to a master laser (ML) with a frequency difference of approximately 6.834 GHz. A mean-square phase error of approximately 0.06 rad² is achieved, with a beat linewidth below 1 Hz between the two ECDLs. The phase noise reaches a flat floor of -100 dBc/Hz in the offset frequency range from 1.1 kHz to 1 MHz.

The structure of our digital OPLL is shown in Fig. 1. Two ECDLs running at about a 780 nm wavelength are used in the scheme. The ML (TA pro, TOPTICA) is locked to a naturally broadened atomic transition

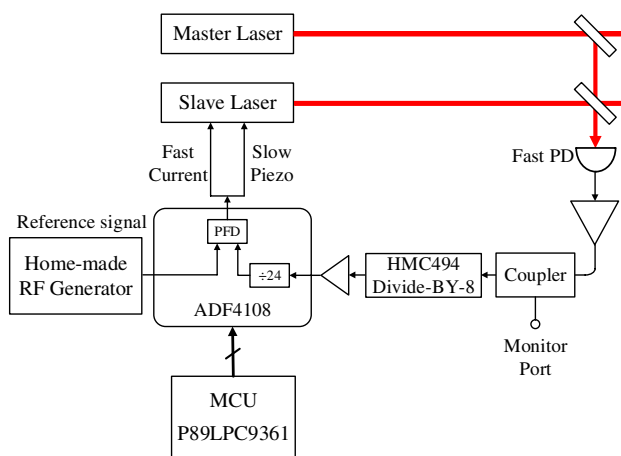


Fig. 1. Structure of OPLL. PFD, phase frequency detector; MCU, microcontroller unit; Fast PD, fast photodiode.

using saturated absorption spectroscopy. The SL (DL 100, TOPTICA) is locked to the ML by the OPLL.

The output optical beams from the ML and SL are overlapped by a beam splitter and sent to an ultrafast photodiode (G4176, Hamamatsu) with a sensitivity of 0.3 A/W @780 nm for generating the beat note signal. The total optical power of the two lasers that reaches the photodiode is about 2 mW. After a wideband (0.2 MHz to 12 GHz) and high-speed response bias tee (ZX85-12G+, Mini-Circuits), the beat note signal at about 6.834 GHz is amplified by a low-noise, ultra-wideband (0.01 to 12 GHz), and excellent gain flatness (± 0.7 dB typ: 0.05–8 GHz) microwave amplifier (GVA-123+, Mini-Circuits). An unbalanced coupler splits the microwave power after the microwave amplifier and sends a small proportion to an output port. The coupler is not essential for regular operation, but could be used to monitor the frequency fluctuation and the lock performance when initially setting up the system.

After the pre-amplifier, we use a prescaler (HMC494, ADI) to realize down-conversion. HMC494 is a low-noise divide-by-8 static divider. It has ultra-low single sideband (SSB) phase noise (-150 dBc/Hz) and a very wide bandwidth (DC-18 GHz). As the output power of HMC494 is small (-4 dBm), another amplifier (HMC474, ADI) is added after the divider. HMC474 has low-phase noise and excellent gain stability (15 dB, DC-6 GHz). Since the frequency of the beat note signal has been divided by 8, a wide bandwidth is not required for this amplifier.

The divided and amplified beat note signal is sent into a low-noise digital phase and frequency detector chip (ADF4108, ADI) and then it is compared with a reference signal. ADF4108 has a very high bandwidth (up to 8 GHz). This chip could divide the beat signal by a factor N and the reference signal by a factor R digitally and then compare the frequency and phase of both divided signals. ADF4108 is interfaced with a micro-controller (P89LPC9361) to control the divider coefficients R and N easily upon start-up. In our scheme, the R counter is set to 1, and the N counter is set to 24. Theoretically (restricted by the bandwidth of the amplifier, etc.), the permissible frequency difference of phase-locking ranges from sub-megahertz to 12 GHz. Thus, to address the full range of the target locking range, the reference signal should range from several kilohertz to 62.5 MHz.

The digital phase and frequency detector produces a phase error signal by comparing the phase of the down-converted beat note signal with that of the reference signal from the homemade RF generator. The phase error signal is divided into two paths for the slow and fast feedback loops of the OPLL. The fast loop acts directly on the injection current of the slave ECDL to suppress high-frequency fluctuations in synchronization. A resistance capacitance (RC) phase-advanced filter is used here to balance the roll-off in the diode laser response and therefore to extend the loop bandwidth. Long-term corrections are performed by changing the cavity length of the slave ECDL through the slow loop. As the ECDLs and optical

elements can be regarded as an equivalent voltage-controlled oscillator (VCO), a complete OPLL has been implemented: it consists of a digital phase frequency detector (DPFD), an external loop filter, and a VCO. Detailed circuit diagrams circuits have been uploaded to the internet^[18]. The size of our OPLL board is 11.1 cm \times 7.1 cm.

There are many commercially available RF generators, but generally they are large and expensive. In addition, much of their phase noise generally does not meet the requirements of a high-performance OPLL. A direct digital synthesizer (DDS) can be well-integrated on-chip with an excellent performance and is capable of providing a trigonometric output with a high frequency resolution, low phase noise, and continuous phase and frequency modulation. We have designed a programmable reference signal source based on the DDS technique. In order to reduce the phase noise of the reference signal, an oven-controlled crystal oscillator (OCXO) is selected as the reference clock of the DDS. The OCXO (O23B, DAPU) has an ultra-low phase noise, a temperature stability of $\pm 2 \times 10^{-10}$ /K (@ $-20^\circ\text{C} \sim 70^\circ\text{C}$), and an aging rate of $\pm 5 \times 10^{-8}$ /year.

The schematic configuration of the homemade RF generator is shown in Fig. 2. It mainly includes three modules: the power supply module, the DDS module, and the control and communication module. The core of the system is an FPGA module EP4CE6E22 from Altera (Cyclone IV), which connects to a user-interface computer via a single USB cable for data transfer. The control parameters, such as the frequency, phase, and amplitude, required by the DDS (AD9910, ADI) are automatically generated by the FPGA after the calculation. The FPGA only needs to initialize DDS and sets corresponding register values of DDS. Then, the DDS chip can output the desired RF waveform. The AD9910's highest frequency output can be up to 400 MHz, and its tuning resolution is 0.23 Hz.

The structure of this system is simple and clear. Aside from the ECDLs and the optical elements for the beat measurement, the loop is implemented digitally through two boards. The homemade RF generator board provides a low-phase-noise reference signal to the OPLL board.

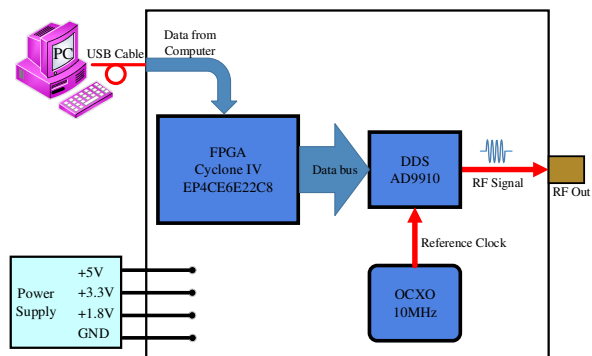


Fig. 2. Schematic configuration of homemade RF generator.

The OPLL board outputs fast and slow feedback signals to the SL to close the phase loop.

The advantages of our structure are obvious: the use of a divider instead of a microwave mixer to down-convert the beat note saves the use of a microwave source. We locked an SL to an ML by using just two boards without any additional electronic equipment (excluding the control computer). In our system, we can realize a low-noise phase-lock loop with a large frequency differences without the need for an extra commercial microwave or an RF signal source.

With the monitor port on the OPLL board, the beat note signal can be checked when the loop is closed. First, the spectrum of the closed-loop beat note signal is obtained through a spectrum analyzer. A typical 6.834 GHz closed-loop beat note signal is shown in Fig. 3. In Fig. 3(a), the resolution bandwidth of the spectrum analyzer is set to be 10 kHz. We can find that the total feedback bandwidth is approximately 1.6 MHz.

The beat note signal at a span of 100 Hz is shown in Fig. 3(b). In this condition, the resolution and video bandwidth of the spectrum analyzer are both 1 Hz. However, the width of the carrier signal could not be resolved even with the lowest-resolution bandwidth. This implies that the actual linewidth between the two phase-locked ECDLs is below 1 Hz.

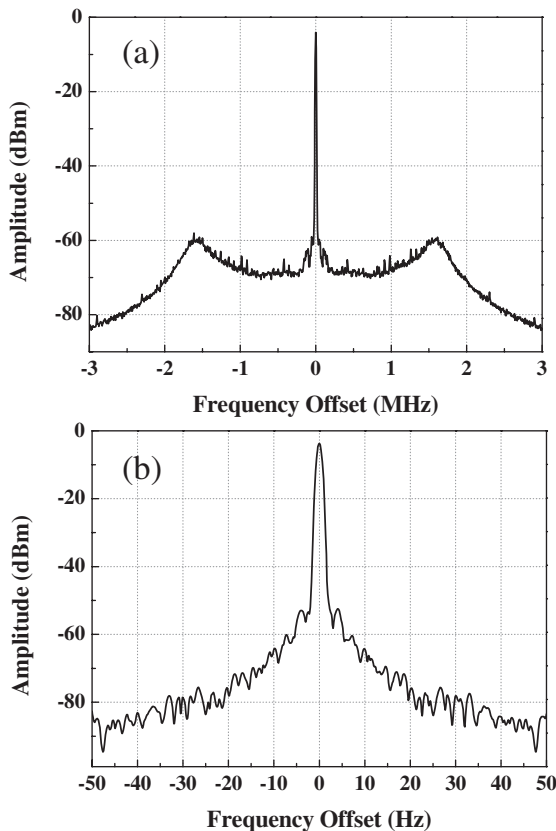


Fig. 3. (a) A typical spectrum of the closed-loop beat note signal (resolution bandwidth is 10 kHz). (b) Expanded view of the beat note signal (resolution bandwidth is 1 Hz)

Phase noise is an important index to evaluate the performance of a phase-locked loop. In our OPLL system, the phase noise of the beat note signal depends on the phase noise of the homemade DDS signal source, the noise introduced by the feedback circuit, and the feedback bandwidth. By choosing components with good performance, the noise of the circuit can be reduced. We select an ultra-low phase noise OCXO as the reference clock of the RF generator to reduce the phase noise of the reference signal source.

The phase noise of the homemade RF generator at the operating frequency is shown in Fig. 4(a), and the phase noise spectrum of the beat note signal is shown in Fig. 4(b). As the frequency divider can reduce the phase noise, the phase noise of the reference signal is better than the beat note signal. The phase noise of the beat note signal reaches a flat floor of -100 dBc/Hz in the offset frequency range of 1.1 KHz to 1 MHz. The peak at 1.6 MHz indicates the bandwidth of feedback loop. It is consistent with the results in the preceding paragraph. The above results have clearly shown that our OPLL has good phase-noise suppression.

We also calculate the mean-square phase error $\langle \Delta\varphi^2 \rangle$ to evaluate the performance of the OPLL. This error can be obtained by measuring the power fraction of the carrier in the beat note signal. It is given by:

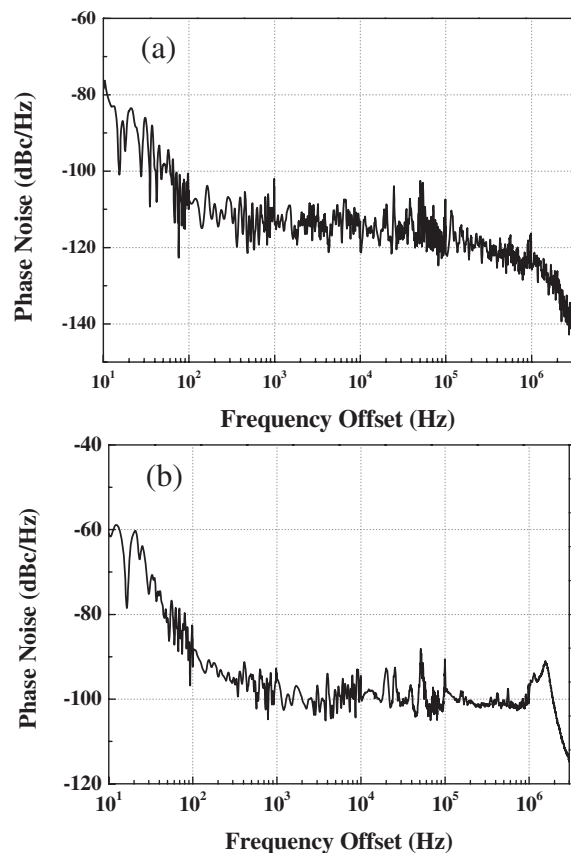


Fig. 4. (a) Phase noise spectrum of the reference signal. (b) Phase noise spectrum of the OPLL.

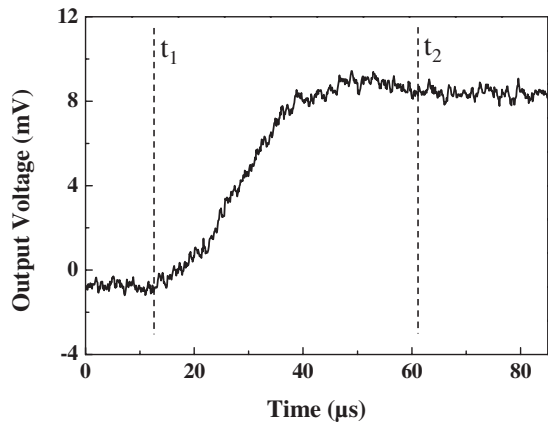


Fig. 5. Dynamic performance of the OPLL. Transition time between t_1 and t_2 is approximately 50 μs .

$$\exp(-\langle\Delta\phi^2\rangle) = \frac{P_{\text{carrier}}}{\int_{-\infty}^{\infty} P(v)dv}, \quad (1)$$

where $\int_{-\infty}^{\infty} P(v)dv$ represents the integrated power in the full spectrum. From the spectrum similar to Fig. 5, the residual mean-square phase error $\langle\Delta\phi^2\rangle$ of 0.06 rad^2 is achieved in the 10 MHz integration bandwidth. This result is comparable to conventional OPLLs utilizing microwave frequency mixing to fulfill the frequency down-conversion.

The dynamic performance of the OPLL can be tested through monitoring the amount of time the OPLL requires to recover phase locking after a sudden changes in the reference. It is an indication of the frequency turning agility. When the OPLL was stably locked, we applied frequency hopping on the reference signal to create a frequency difference of about 20 MHz. Then the output of the OPLL was recorded; it is drawn in Fig. 5. As the frequency of reference signal was hopped, the phase error exploded abruptly at t_1 . In this situation, the output voltage of the current control changed simultaneously to control the SL's frequency in order to match the reference signal. At t_2 , the output value was stable again, which means the transition process was finished and the phase had been locked again. It is found that the transition time between t_1 and t_2 is about 50 μs .

In conclusion, we present a compact, low-noise, and inexpensive OPLL. Compared with a conventional OPLL, the OPLL uses a divider instead of a microwave mixer to down-convert the beat note signal. In this way, the microwave reference signal is omitted. We also design

an ultra-low phase noise RF generator as the reference signal. The whole cost of the two boards is less than 700 dollars. The mean-square phase error is found to be 0.06 rad^2 , and the beat note linewidth of two phase locked ECDLs reaches sub-hertz levels. All the test results prove the competent performance of our system, which is promising as a low-budget choice in the fields of cold-trapped atoms, cold atom interferometry, and so on.

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