A dither-free bias voltage and driver signal amplitude control technique for optical 8PSK generator

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We propose a dither-free 8-phase-shift-keying (8PSK) generator control scheme for adjusting the bias voltage of Mach–Zehnder modulator (MZM) and the electrical driver signals of two cascaded phase modulators (PMs). The control module includes a delay-line interferometer (DLI), a balanced photo-detector (BPD), and asynchronous sampling data processing. Both analysis and simulation results show that the bias voltage and the driver signal amplitude control can be achieved independently between these cascaded modulators with only one tap point and one control configuration. Finally, the influence of the bit number of A/D converter (ADC) for asynchronous sampling is also discussed for the practical implementation.

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With the bandwidth demand driven by the growing internet traffic, higher-order advanced modulation formats have been employed to achieve higher spectral efficiency (SE). Multilevel phase-shift-keying (PSK)[1–5] and quadrature amplitude modulation (QAM)[6–8] formats offer high spectral efficiency transmission for next-generation ultra-larger-capacity optical transmission systems[9,10]. Quadraturephase-shiftkeying (QPSK) with polarizationdivisionmultiplexing[11,12] has been utilized to achieve over 100Gb/s capacity in 50-GHz-grid wavelength-division multiplexed (WDM) transmission systems. PolMux-RZ-8PSK modulation format has been utilized experimentally to obtain a record SE of 4.2 bit/s/Hz successfully[1,4]. The typical transmitters in these high-order modulation formats (m-PSK/m-QAM) schemes usually include more than one Mach–Zehnder modulators (MZMs) and one or more phase modulators (PMs). In these transmitters, the operating parameters including bias voltage and driver signal amplitudes will be fluctuated and drifted away from their optimal points due to environmental temperature fluctuation, device aging and amplifier heating. Therefore, automatic control of these physical parameters is one of the enabling technologies for long-term stability in practical transmitter implementation. Most existing literature mainly focus on automatic bias control in dual-parallel MZM for QPSK signal generation or arbitrary signals generation[13–16]. The monitored parameters for feedback control mainly include optical power[13–14] and its statistics (mean and variance)[16], low-frequency RF energy[13], and the differential phase[15]. Meanwhile, the driver signal amplitude of phase modulator is equivalently important for multi-level PSK/QAM transmitters' implementations[1,4,17]. Recently, a simple and robust control strategy for driver signal amplitude of one phase modulator was proposed by Yang *et al.*[18]. Neither, however, deals with cascaded situation including both MZMs and PMs.

In this paper, a dither-free control scheme is proposed for bias voltage and driver signal amplitude of the cascaded modulators used in 8-phase-shift-keying (PSK) generation. The generator includes one MZM with 180 degrees phase-shift keying and two PMs with 90 degrees and 45 degrees phase modulation, respectively. The scheme adjusts bias voltage and driver signal amplitudes simultaneously in a dither-free manner with only one tap point and one control configuration. To the best of our knowledge, we believe that this is the first work that shows how to control both bias voltage and driver signal amplitude in one control scheme. The control performances for the case of 8PSK are numerically simulated with regard to the control strategy, the influence of non-ideal implementations, and the bit number of ADC. System penalty due to the introduction of the dither signal can be avoided by this scheme. This advantage is especially important because the tolerated phase error will be smaller for higher order modulator implementation.

The system model is shown in Fig. 1. A typical 8PSK transmitter consists of a MZM, PM1 and PM2. D1 to D3 are the data from pulse pattern generator (PPG). The control module includes a delay-line interferometer (DLI),

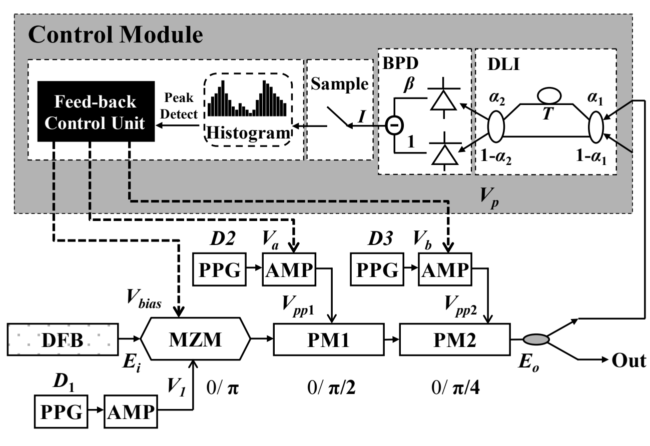

Fig. 1. Block diagram of the proposed control scheme for 8PSK generators. DFB—Distributed Feedback Laser; PPG—Pulse Pattern Generator; AMP— Amplifier.

a balanced photo-detector (BPD), and asynchronous sampling data processing shown in the gray box. One arm of the DLI has a delay of symbol period T. The output optical signal from the DLI is converted into an electrical signal by the BPD, which is then sampled asynchronously at low speed and then constructs histograms. The input parameters of the feedback control unit are the multiple peak locations, which are calculated in the histograms including the cases of normal mode of MZM or working without phase difference of it. By monitoring these input parameters, the control module can automatically adjust the output parameters of the bias voltage of MZM, and the gain voltages V_a and V_b of the driver amplifiers, which subsequently adjust the driver signal amplitudes V_{pp1} and V_{pp2}. Finally the control module ensures the generated phase shifts of the MZM, and two PMs are stabilized at the specified values.

There is no cascade situation in the previous scheme[18], and therefore generated histograms are relatively simple. Peaks in histogram will not appear too much and overlap to each other. But in reality, we have to face more complex signal, cascaded PMs would have the same or 2 times the modulation angle, which will cause more peaks and overlaps in histogram. We cannot use histogram of single peak to control simply with these signals. Another benefit that can be got from the scheme is that the other arm of DLI in the control module does not need phase offset as mentioned in[18]. In the case of cascaded 8PSK modulation format, controlling the bias voltage of MZM and the driver signal amplitude of PMs simultaneously become very necessary. So a more effective feedback control method has been put forward.

The representation of the output optical field E_o after the PM2 is expressed in the form

$$E_o(t) = E_i \cdot \sin\left(\frac{V_{bias}}{2V_\pi}\pi\right)\cdot \exp\left[i\left(\frac{V_{bias}}{2V_\pi} + \frac{V_1}{V_\pi}d_1(t) - \frac{1}{2} + \frac{V_{pp1}}{V_\pi}d_2(t) + \frac{V_{pp2}}{V_\pi}d_3(t)\right)\pi\right]. \quad (1)$$

Here, we have assumed that the value of V_1 is V_π, V_{bias} is around V_π, V_{pp1} is around $V_\pi/2$, and V_{pp2} is around $V_\pi/4$.

The output signal I of the BPD is

$$\begin{aligned} I = &\left\{\alpha_1(1-\alpha_2) + \alpha_2(1-\alpha_1) - \beta\left[\alpha_1\alpha_2 + (1-\alpha_1)(1-\alpha_2)\right]\right\}E_o^2 \\ &+ 2\sqrt{\alpha_1\alpha_2(1-\alpha_1)(1-\alpha_2)}(1+\beta) \\ &\mathrm{Re}\left\{E_o(t-T)\cdot E_o^*(t)\right\} = C_1P + C_2P \cdot \\ &\cos\left\{\left[d_1(t-T) - d_1(t)\right]\pi + \left(d_2(t-T) - d_2(t)\right)\theta_1 + \left(d_3(t-T) - d_3(t)\right)\theta_2\right\}. \end{aligned} \quad (2)$$

$E_o(t)$ has the power $P = E_i^2 \cdot \sin^2(\pi/2 \cdot V_{bias}/V_\pi)$. Assuming that the generated phase shift of PM1 is $\theta_1 = V_{pp1}/V_\pi$, the phase shift of PM2 is $\theta_2 = V_{pp2}/V_\pi$, θ_1 should be hold on $\pi/2$ and θ_2 on $\pi/4$. The power of I is only affected by V_{bias} since V_1, $V_{pp1,}$ and V_{pp2} have constant values. No matter what the data from the PPG, are V_{bias} can be adjusted by maximizing the absolute value of I. That is easy to implement within the histogram constructed by the sampled values of I as the error signal.

In the following, the focus is on the controlling of θ_1 and θ_2. In Eq. (2), I depends on the phase shift θ_1 generated by PM1, θ_2 generated by PM2, and the phase difference φ between two consecutive bits in MZM. We use $I_{i,x}$ (i = 1, 2…5) to represent the values of I_i when the phase difference $\varphi = x$ degrees. The BPD output signals I have values:

$$\begin{aligned} &I_{1,\varphi} = C_1P + mC_2P\cos(\theta_1 + \theta_2), I_{2,\varphi} = C_1P + mC_2P\cos(\theta_1), \\ &I_{3,\varphi} = C_1P + mC_2P\cos(\theta_1 - \theta_2), I_{4,\varphi} = C_1P + mC_2P\cos(\theta_2), \\ &I_{5,\varphi} = C_1P + mC_2P, \begin{cases} m = 1 \quad \varphi = 0 \quad d_1(t-T) - d_1(t) = 0 \\ m = -1\, \varphi = \pm\pi \;\; d_1(t-T) - d_1(t) = \pm 1. \end{cases} \end{aligned} \quad (3)$$

With Eq. (3), the phase shift θ_1 generated by the PM1 can be calculated by

$$\cos\theta_1 = \frac{2I_{2,0} - \left(I_{5,0} + I_{5,\pm\pi}\right)}{I_{5,0} - I_{5,\pm\pi}} \quad (4)$$

The phase shift θ_2 generated by the PM2 can be estimated by

$$\cos\theta_2 = \frac{2I_{4,0} - \left(I_{5,0} + I_{5,\pm\pi}\right)}{I_{5,0} - I_{5,\pm\pi}} \quad (5)$$

The driver signal amplitude V_{pp1} can be tuned adaptively to achieve a stable phase shift $\pi/2$ by monitoring the error signal $\varepsilon_1 = 2I_{2,0} - (I_{5,0} + I_{5,\pm\pi})$ and making it approach to zero. V_{pp2} can be tuned to achieve a stable phase shift $\pi/4$ by monitoring the error signal $\varepsilon_2 = 2I_{4,0} - (1+\sqrt{2}/2)I_{5,0} - (1-\sqrt{2}/2)I_{5,\pm\pi}$ and making it approach to zero. But for practical implementation, the situation $\theta_1 = 2\theta_2$ appears, which will cause the overlap of $I_{i,x}$. Thus, we should carefully choose proper $I_{i,x}$ for monitoring in order to achieve stable phase modulation. The analysis above has considered the non-ideal splitting ratios of the two couplers and the responsivity difference between the two PDs, indicating that the control technique has robust performance against these imperfections.

In Fig. 1, the modulator part will generate 8PSK optical signal if two cascaded PMs have the phase shifts of 90 and 45 degrees respectively, and the MZM have an ideal 180 degrees deviation under the push–pull operation. The MZM have two operative modes in the simulation: one is normal mode with phase difference between two consecutive bits is 0 or ±180°, the other is operating with continued 0 at D1 which means the phase difference maintains 0. The proposed amplitude control scheme can be utilized to achieve stable 90° and 45° phase shift for two cascaded PMs. The DLI has a fixed delay time of one symbol period, the output electrical signal of the BPD is then measured and asynchronously sampled. The histograms are constructed with these samples.

Fig. 2(a-c) shows the plotted histograms of the samples when PM1 has the phase shift of 90 degrees and PM2 has three phase shifts of 35 degrees, 45 degrees,

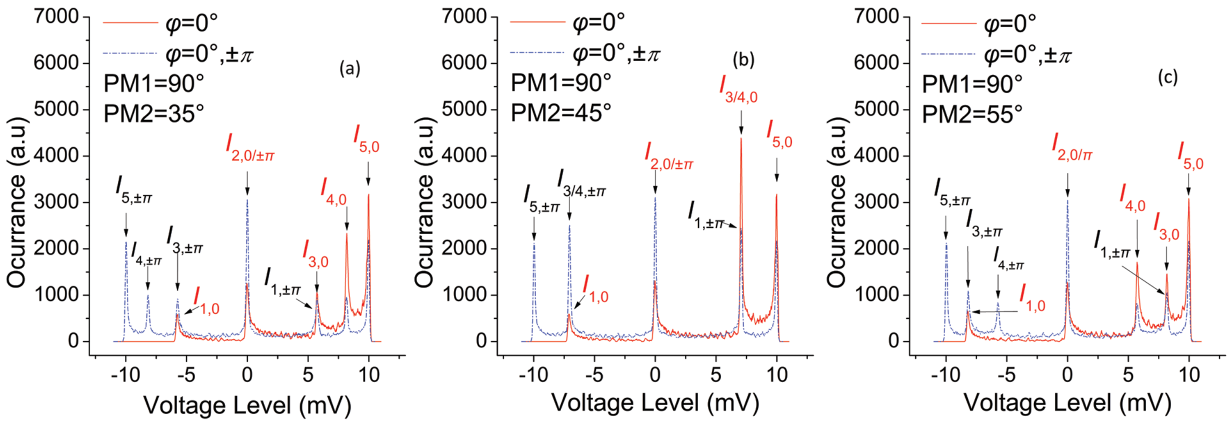

Fig. 2. Histograms of the sampled BPD output signal when the module depth are (a) PM1 = 90 degrees, PM2 = 35 degrees; (b) PM1 = 90 degrees, PM2 = 45 degrees; (c) PM1 = 90 degrees, PM2 = 55 degrees. The histograms for the MZM phase difference φ of 0 and 0& ± 180 degrees are plotted in red solid line and blue dash-dotted line respectively.

and 55 degrees, respectively. $I_{5,\pm\pi}$ and $I_{5,0}$ have the minimum and maximum voltage levels respectively for easy identification in histograms. I_1 to I_5 are obtained by finding the peak locations in the plotted histograms.

In order to ensure that the PM1 has a stable phase shift of 90°, V_{pp1} should be adjusted to make the monitor signal $\varepsilon_1 = 2I_{2,0}-(I_{5,0}+I_{5,\pm\pi})$ approaches to zero. $I_{5,0}$ and $I_{5,\pm\pi}$ can be got when MZM is working normally, and $I_{2,0}$ can be got since MZM does not work or works without phase difference. We use continued 0 at D1 in the simulation to control a stable phase shift of PM1. As shown in Fig 2(a–c), the peak for $I_{2,0}$ overlaps with that for $I_{2,\pm\pi}$ when PM2 has three phase shifts of {35 45 55} degrees, which means the PM1 has a stable phase shift of 90 degrees. The phase shift of the PM2 can be controlled automatically to be 45 degrees with the error signal $\varepsilon_2 = 2I_{4,0}-(1+\sqrt{2}/2)I_{5,0}-(1-\sqrt{2}/2)I_{5,\pi}$. Unfortunately, $I_{3,0}$ will overlap $I_{4,0}$ when PM2 has the phase shift near 45 degrees, as seen from Fig. 2. It is difficult to acquire the accurate peak locations in the presence of the overlapping between peaks. Therefore, the $I_{i,x}$ in the expression of the error signals should be chosen carefully to avoid the overlapping between them in histograms. Here, an improved phase shift estimator for PM2 is proposed with Eq. (3) with $\theta_1 = 90°$:

$$\sin\theta_2 = \frac{I_{5,0}+I_{5,\pi}-2I_{1,0}}{I_{5,0}-I_{5,\pm\pi}}, \tag{6}$$

in which the peak of $I_{1,0}$ can be found easily and will not overlap with other neighboring peaks. Consequently, the improved monitoring error signal becomes $\overline{\varepsilon}_2 = (1-\sqrt{2}/2)I_{5,0}+(1+\sqrt{2}/2)I_{5,\pi}-2I_{1,0}$. V_{pp2} should be adjusted to make the monitor signal $\overline{\varepsilon}_2$ approach to zero, and then the phase shift of PM2 can be stabilized at 45 degrees. Here, we also need the continued 0 at $D1$ for finding the peak of $I_{1,0}$.

Fig. 3 presents the monitored error signals of $\varepsilon_1 = 2I_{2,0}-(I_{5,0}+I_{5,\pm\pi})$ as a function of the actual phase shift for PM1 with the PM2 having different phase shifts of {35 40 45 50 55} degrees. As we assumed the V_π is $5\,V$ in the simulation and the V_{pp1} and V_{pp2} can be converted from voltage to angle in order to facilitate analysis. The error signal decreases monotonically with the actual phase shift for PM1, and it is close to zero when the phase shift approaches 90 degrees. The simulation results confirm that the amplitude control on PM1 is independent of the phase shift of PM2. Meanwhile, under the two different devices parameters, the simulated curves of the monitored signal are almost the same around the 90 degrees. This means that the performance of the control scheme is not degraded by the non-ideal specifications of the DLI and the BPD.

Figs. 4(a) and (b) shows the monitored error signal for amplitude control for PM1 and PM2, respectively. The main parameters are set as follows: the ADC has the bit number of {6, 8, 10}; the DLI has non-ideal splitting ratios of 0.45:0.55; the BPD has unbalanced responsivity of 1:0.8. The curves of the monitored error signal for 6 bit resolution fluctuates obviously, which can induce the significant phase deviation from ideal value during the feedback procedure. The control performance is improved when the bit resolution increases.

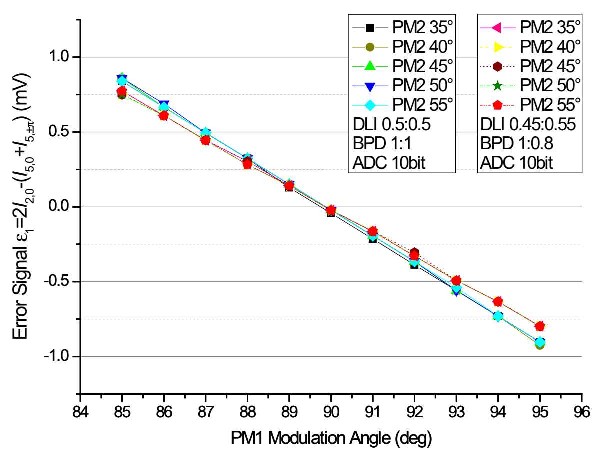

Fig. 3. Error signal is a function of the phase shift for PM1 when the PM2 has different phase shift of {35 40 45 50 55} degrees respectively. Two different devices parameters are used: (I) the splitting ratios of DLI is 0.5:0.5, responsivities of BPD is 1:1; (II) the splitting ratios of DLI is 0.45:0.55, responsivities of BPD is 1:0.8.

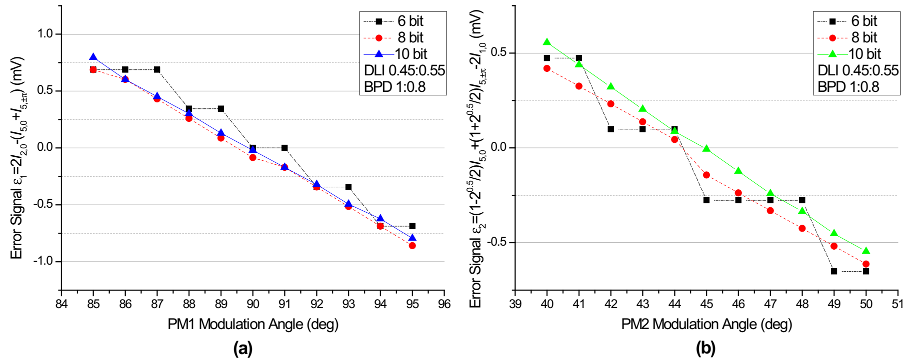

Fig. 4. (a) Error signal of the amplitude control for PM1 when the phase shift of PM2 is fixed at 45 degrees; (b) Error signal of the amplitude control for PM2 when the phase shift of PM1 is fixed at 90 degrees.

The 8-bit resolution is the moderate specification for practical implementation with the trade-off between performance and cost. Also, the phase shift can be controlled more precisely by increasing the number of samples to construct the histograms. It's noted that the above simulations focus on the case of non-return-zero optical signal. In the case of optical return-zero signals, the distribution profile of zero voltage level in the detected histograms is enhanced remarkably, which makes it difficult to identify multiple peaks for acquiring the accurate error signals. Therefore it's suggested that the control configuration should be placed before pulse carving in practical transmitter implementations.

We propose and apply a dither-free 8-phase-shift-keying (8PSK) generator control scheme for adjusting the MZM bias voltage and the respective driver signal amplitudes of cascaded phase modulators. It is proved analytically that the resultant phase deviations can be automatically stabilized at any arbitrary values. Numerical simulation with 8PSK modulation transmitter implementation demonstrates that the effectiveness of the control can be achieved independently for these modulators with one control configuration. The scheme is inherently not sensitive to the non-ideal specifications of the DLI and the BPD. In practice, 8-bit ADC resolution is moderate in term of performance and cost. The proposed control scheme has lower specification on devices and the advantage of dither-free manner. It has wide applications to stabilize the phase shift of cascade phase modulators for implementing various PSK/QAM transmitters.

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