Fabrication of low threshold current monolithic DFB laser with an MMI combiner

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We fabricate low threshold current monolithic distributed feedback (DFB) laser with a multi-mode interface (MMI) combiner using butt-joint metal-organic chemical vapor deposition technology with different waveguide structures. Multi-layer mask self-aligned photolithography technology is used to form different waveguides in active and passive regions, respectively. The result shows that the laser threshold current is lower than 10 mA, with 50 dB side-mode suppression ratio.

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Today, with the development of optical network, especially access network, monolithic integrated optoelectronic device plays a very important role because of its potential low cost and high yield[1]. However, compared with electronic integrated device, optoelectronic integrated device is more complex and hard to fabricate. So far, many different integrated optoelectronic devices with distributed feedback (DFB) laser have been reported as DFB laser's high performance and stability[2–4]. Actually, discrete DFB laser has been applied in backbone network for many years. So, DFB-based integrated optoelectronic devices are one of the most interesting devices for researchers. Two typical devices using DFB laser array are monolithic DFB laser array with multi-mode interface (MMI) combiner or with arrayed waveguide gratings (AWGs). Although AWG is powerful especially in the case of lager channel number, it is large and hard to fabricate with high performance. So it is just suitable for high-end application such as optical line terminal. Although the performance of MMI is relatively lower, it is smaller with larger tolerance which means high yield, low cost, and suitable for optical network unit. However, the threshold current of the DFB laser is often larger than discrete commercial chip as different regions in the device are often hard to optimize and fabricate independently. In this letter, an extreme low threshold current monolithic DFB laser with an MMI combiner is fabricated using butt-joint regrowth (BJR) and multi-layer mask self-aligned photolithography technologies. The result shows that the threshold current is lower than 10 mA with 50 dB side-mode suppression ratio (SMSR), which is comparable to discrete chip with the same structure which means that using this fabrication process, the laser in the integrated device can work as good as discrete chip.

Figure 1 shows the schematic structure of the four-channel multi-wavelength DFB laser array with an MMI combiner. The laser section is 250 μm long with 250 μm gap for adjacent laser diode (LD). The S-band is 1350 μm long. The MMI coupler is 20 μm wide and 270 μm long, which is calculated using commercial photonic software (Rsoft). The simulation results are shown in Fig. 2.

The fabrication process can be described as follows: first, the epitaxial materials should be prepared. BJR technology is used to integrate active and passive materials together. Compared with other integration technology such as selective area growth[5] and quantum well intermixing[6] it can provide the capacity to optimize

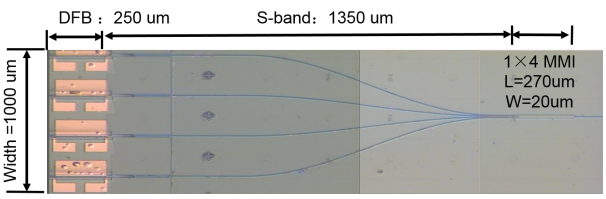
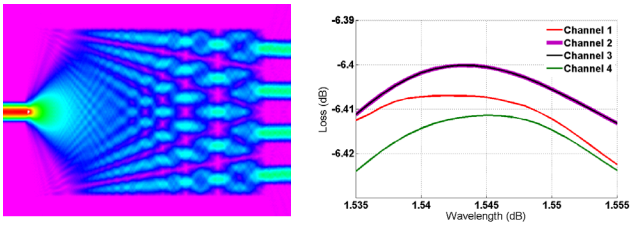


Fig. 1. Photomicrograph of the device.



(a) (b)

Fig. 2. Simulation results of the MMI combiner: (a) BPM propagation result and (b) transmission spectrum.

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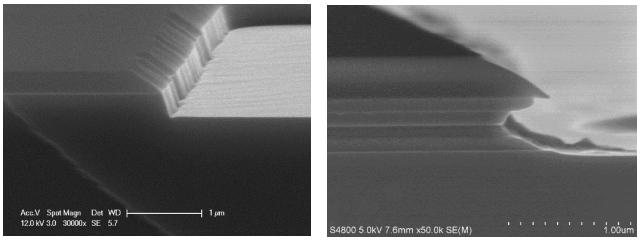


(a) (b)

Fig. 3. SEM images of (a) after dry etching using RIE process and (b) after wet etching using 311 solution.

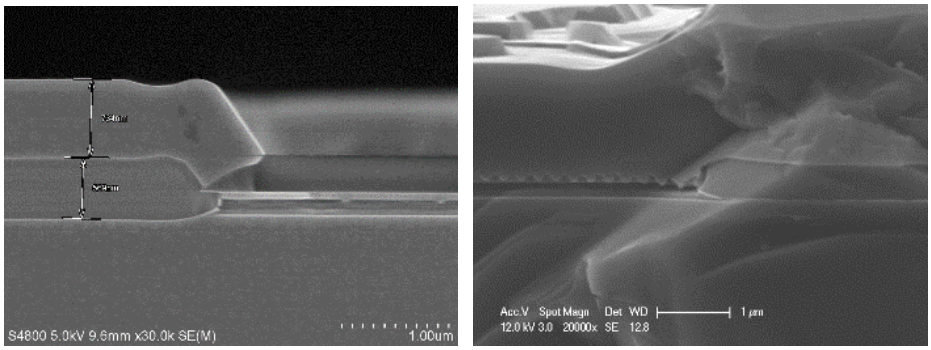
the materials in different regions independently and can also get the largest band-gap differences.

The detailed process is described as follows: firstly, an active structure with multi-quantum wells (MQWs) is grown by metal-organic chemical vapor deposition (MOCVD) on InP substrate, which consists of six compressive strain quantum wells/tense strain barriers with 5 and 10 nm, respectively, and separation confinement hetero-structure layer. Then an SiO_2 layer is deposited by plasma-enhanced chemical vapor deposition (PECVD) technology. The active region is defined by photolithography and then the SiO_2 on the passive region is removed by reactive ion etching (RIE) technology. In BJR process, the profile of the undercut is very important to suppress the overgrowth in the interface as the increased reactant concentration on the SiO_2 mask. The undercut structure for BJR is fabricated by two-step etching process combing with dry etching and wet etching[7]. Secondly, RIE process is used to etch the MQW structure in the passive region of buffer layer (Fig. 3(a)). Then 311 (H_2SO_4:H_2O:H_2O_2) selective solution is used to etch the sidewall for about 150–350 nm and to stop on the InP buffer. The profile of the fabricated undercut is shown in Fig. 3(b). BJR process is followed including 400 nm thick InGaAsP waveguide layer with a band gap of 1 eV (photoluminescence (PL) peak = 1.24 μm) and 400 nm thick InP layer without doping to reduce free-carrier absorption.

After BJR process, the SiO_2 layer is removed, then soft stamp nanoimprint technology is used to fabricate the $\lambda/4$ phase-shifted grating on the active region as reported above[8]. Then the third MOCVD process is followed including 50 nm InP spacer, 20 nm etching stop layer, 1600 nm InP cladding layer, and 200 nm InGaAs layer. The scanning electron microscope (SEM) images of the cross profiles are shown in Fig. 4 and the PL spectrum of the wafer is shown in Fig. 5.

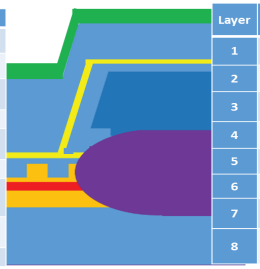
The waveguide of the laser is shallow etched, whereas the MMI is deep etched. Here multi-layer self-aligned photolithography technology is introduced to fabricate the structure. The detailed process is shown in Fig. 6. Firstly, an SiO_2 layer is deposited on the wafer, and then the waveguide of active and passive regions is defined by one-step photolithography simultaneously[9] to avoid waveguide break or misalignment in two-step photolithography[10]. As in common lithography, the overlay accuracy is often larger than 1 μm, which is too large for waveguide alignment.

However, in order to get different etch depths, one of the two regions should be protected first when we etch another. Unlike the process reported in Ref. [10], as the



(a) (b)

Layer	Material	Thick	Doping	Function
1	p-InGaAs	200 nm	1×10^{19}	Contact layer
2	P-InP	1600 nm	1×10^{18}	Cladding layer
3	p-1.05Q	20 nm	1×10^{18}	Etching stop layer
4	p-InP	50 nm	1×10^{18}	Spacer
5	1.2Q	100 nm	1×10^{18}	Up cladding layer
6	MQW	100 nm	1×10^{18}	PL:1540 nm
7	1.2Q	100 nm	1×10^{18}	Down cladding layer
8	n-InP buffer	500 nm	1×10^{18}	
9	Sub			



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4	P-InP	50 nm	1×10^{18}	Spacer
5	u-InP	400 nm	Uid	Cladding layer
6	1.24Q	400 nm	Uid	Waveguide layer
7	n-InP buffer	100 nm	1×10^{18}	Down cladding layer
8	sub			

(c)

Fig. 4. SEM images of the butt-joint interface: (a) after BJR process, (b) after the whole process, and (c) materials structure for the two parts.

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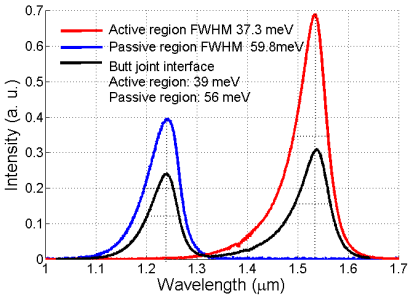


Fig. 5. PL spectrum of the wafer.

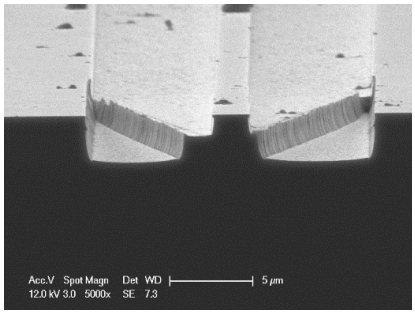


Fig. 7. SEM image of the transition structure.

deep-etched region of our chip is much larger than the shallow-etched region, lift-off process should be applied in smaller shallow-etched region avoiding failure. So, multi-layer mask is used to protect the smaller active region during inductively coupled plasma (ICP) process and then be selectively removed by acetone like the lift-off process. The detailed description is as follows: firstly, a negative photoresist is spin on the wafer (Fig. 6). Low-temperature PECVD process is used to depose an SiO_2 layer on the resist. The passive region is defined by photolithography and then the SiO_2 on the passive region is removed by the RIE process. O_2 RIE process is applied to remove the resist in the passive region sequentially. Secondly, ICP etching process is used to etch the passive waveguide to a suitable depth. After this the wafer is dipped in acetone and the upper SiO_2 on the active region is removed just like the lift-off process. ICP process is used again to etch the whole wafer to form active and passive waveguides. Finally, resist is used to protect the passive region using lithography technology, and then wet etching is applied to get the active waveguide to etching stop layer.

The SEM image of the fabricated taper between active and passive waveguides is shown in Fig. 7. After the fabrication of waveguide, sputtered Ti/Pt/Au p-type and evaporated Au/Ge/Ni n-type electrical contacts are formed, completing the process flow. All output facets of the device are formed by cleaving and coating with anti-reflection film.

The *P–I* curves of the two facets for the four lasers are shown in Fig. 8(a). For ideal λ/4 phase-shifted DFB laser, the output power from both facets are the same[11]. So the loss of the passive waveguide can be clearly characterized by the *P–I* curves. The average slop efficiency of the MMI side output port is about 0.0049 W/A, whereas for the DFB side is about 0.0987 W/A. The passive waveguide loss for each channel is about 13 dB, which is calculated from the *P–I* curves of the two sides. According to our analysis, the loss can be divided into three parts: inherent loss of the MMI (6.0 dB), propagation loss (2–3 dB) for about 2 mm long waveguide[12], and coupling loss of about 3–4 dB.

Compared with the results reported in Refs. [13–16], the threshold current of our device is quite low, less than 10 mA which is comparable to the discrete device. This is because the laser fabrication process is almost the same with the discrete device, there is no degradation in the integrated device. The results indicate that multi-layer self-aligned photolithography technology is suitable for the fabrication of integrated device.

The spectrum of the four-channel laser from the MMI side is tested with 60 mA injected current at 25 °C (Fig. 8(b)). The measured lasing wavelengths are 1549.21, 1550.26, 1551.58, and 1553.16 nm for the four channels, respectively. Using linear regression method analysis, the average wavelength space is about 1.39 nm, which can be corrected to design value of 1.6 nm by thermal electrode. The SMSR is around 50 dB which is rather high in integrated device as λ/4 phase-shifted DFB laser is used as light source. The asymmetric spectrum for λ/4 phase-shifted DFB laser indicated residual reflection in butt-joint interface. But from the *P–I* curves, there are no serious kinks, which means that the reflection is not large.

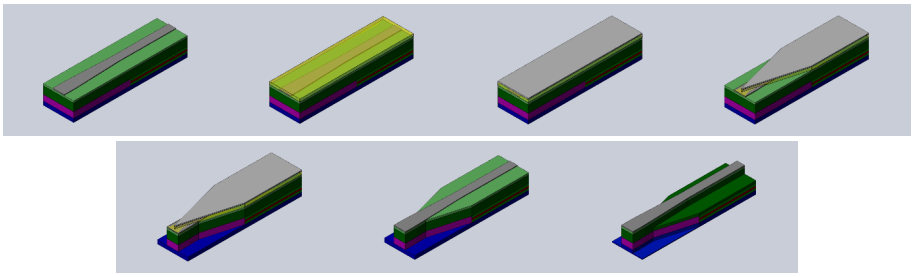
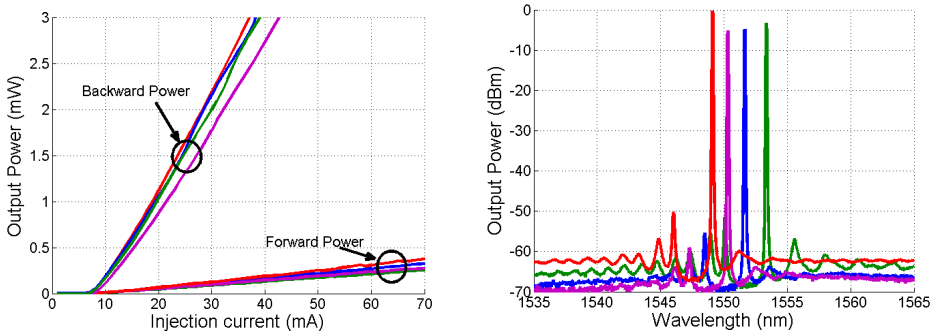


Fig. 6. Fabrication process of the multi-layer self-aligned photolithography technology.



(a) (b)

Fig. 8. (a) *P–I* curves and (b) spectrum of the chip.

In conclusion, we fabricate the monolithic DFB laser integrated with an MMI combiner using BJR and multi-layer mask self-aligned photolithography technologies. The low threshold current is rather low, that is, of about 6–10 mA, which is comparable to discrete chip. The laser can work in single-mode state with a high SMSR larger than 50 dB. The results indicate that, following the fabrication process, the laser in integrated chip can work as well as a discrete chip.

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