Tunneling in submicron CMOS single-photon avalanche diodes

Mohammad Azim Karami*, Armin Amiri-Sani, and Mohammad Hamzeh Ghormishi

Department of Electrical Engineering, Iran University of Science and Technology, Hengam St., Narmak, Tehran, Iran

**Corresponding author: karami@iust.ac.ir*

Received October 6, 2013; accepted November 19, 2013; posted online December 25, 2013

Tunneling is studied in two main single-photon avalanche diode (SPAD) topologies, which are n-tub guard ring (NTGR) and p-tub guard ring (PTGR). Device simulation, $I-V$ measurements, and dark count calculations and measurements demonstrate that tunneling is the main source of noise in NTGR, but it is less dominant in PTGR SPADs. All structures are characterized with respect to dark noise, photon detection probability, timing jitter, afterpulsing probability, and breakdown voltage. Noise performance is disturbed because of tunneling, whereas jitter performance is disturbed because of the short diffusion time of photo-generated minority carriers in NTGR SPADs. The maximum photon detection probability is enhanced because of an improvement in absorption thickness.

OCIS codes: 250.1345, 250.5403.

doi: 10.3788/COL201412.012501.

Single-photon avalanche diodes (SPADs) are photodiodes that are biased above the breakdown voltage in Geiger mode. SPAD noise is represented in terms of mean dark count rate (DCR) and originates from thermal generation, band-to-band tunneling (BTBT), and trap-assisted tunneling[1].

A high DCR is reported in SPADs implemented in 90-nm standard complementary metal-oxide-semiconductor (CMOS) technology[2]. N-tub guard ring (NTGR) is employed in this device; however, previous SPADs incorporated into 0.8-, 0.35-, 0.18-, and 0.13-μm CMOS technologies[3–6] are p-tub guard ring based (PTGR based). Noise that originates from tunneling in NTGR SPADs is compared with that in PTGR SPADs. Device simulation and characterization measurements suggest that intrinsic high tunneling in NTGR SPADs originates from inappropriately high doping levels in the multiplication region. The tunneling effect in several types of SPAD devices is characterized and measured. Some research groups have applied special layers in other technologies to reduce tunneling current[7].

The use of NTGR to prevent premature edge breakdown has been proposed in the first planar SPADs[8]. NTGR has been combined with double-epitaxial technologies to boost SPAD performance in Ref. [9].

Figure 1 shows the cross-sections of PTGR and NTGR SPADs. Photon absorption generates an electron-hole pair in the depletion region. Free carriers trigger an avalanche as a result of impact ionization. The avalanche current is quenched with the use of active and passive methods to prevent destruction of the device. Similar methods are used to induce device recharge, i.e., reverting the device to its idle state to detect the next impinging photon. The NTGR SPAD discussed in this letter is shown in Fig. 2. It was selected from among several structures implemented in 0.35-μm standard CMOS technology.

The characteristics of NTGR SPAD device are interesting because electrons are the minority carriers in the multiplication region. Electrons have a high impact-ionization probability, which potentially enhances SPAD sensitivity under certain conditions.

Figure 3 depicts the $I-V$ characteristic in NTGR SPADs. The breakdown current in the SPAD introduced in this letter measures several hundred nanoamperes, which is much higher than those in previous SPADs (5, 3, and 7 nA for 2, 3, and 6, respectively).The increased breakdown current can be attributed to either enhanced thermal generation in the depletion region or the high tunneling current in the junction. The reverse current attributed to thermal generation can be calculated with[10]

$$I_{\mathrm{R-G}} = -\frac{qAn_{\mathrm{i}}}{2\tau_0}W, \tag{1}$$

where q is the electron charge, A is the pn junction surface, n_{i} is the intrinsic carrier concentration, W is the

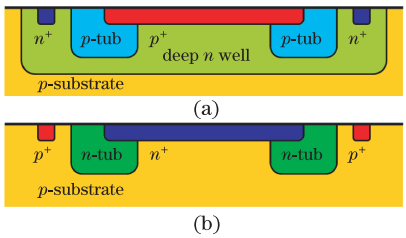

Fig. 1. (Color online) Cross-section of (a) PTGR SPAD and (b) NTGR SPAD.

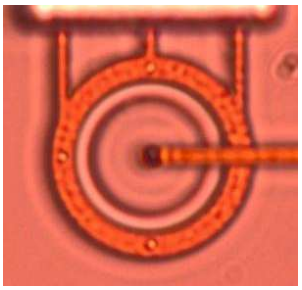

Fig. 2. (Color online) Photomicrograph of NTGR SPAD implemented in 0.35-μm technology.

 © 2014 Chinese Optics Letters

depletion width, and τ_0 is computed by[10]

$$\tau_0 = \frac{1}{2}\left(\tau_p \frac{n_1}{n_i} + \tau_n \frac{p_1}{n_i}\right), \quad (2)$$

where τ_p is the lifespan of the hole in the n side of the junction with a donor density of n_1, and τ_n is the lifespan of the electron at the p side of the junction with an acceptor density of p_1.

Equation (1) results in a thermal generation current that is several orders of magnitude lower than the measured reverse current. Therefore, reverse currents may have mainly originated from tunneling. The tunneling generation rate can be calculated with Kane's model:

$$n = \frac{F^2\sqrt{m_r}}{18\pi h^2\sqrt{E_g}} \exp\left(\frac{-\pi\sqrt{m_r}E_g^{3/2}}{2hF}\right), \quad (3)$$

where n is the number of electrons per s·cm^3 that leaks from the valence band to the conduction band, m_r is the reduced mass as a consequence of the combination of electrons and holes, h is the reduced Planck's constant, E_g is the material bandgap, and F is the electric-field magnitude[11]. Substitution of these parameters can generate 3.3×10^{11} electron-hole pairs/(s·cm^3) in NTGR SPADs and 1.4×10^9 pairs/(s·cm^3) in PTGR SPADs.

Figure 4 exhibits the contours of tunneling generation in NTGR and PTGR SPADs calculated with TCAD® device simulator. The simulation results show the presence of significant BTBT in NTGR SPADs compared with PTGR SPADs. The electron-hole pair generation rates reach 6.1×10^{11} pairs/s(·cm^3) in the long interface between the n+ and p substrates in NTGR SPADs. A

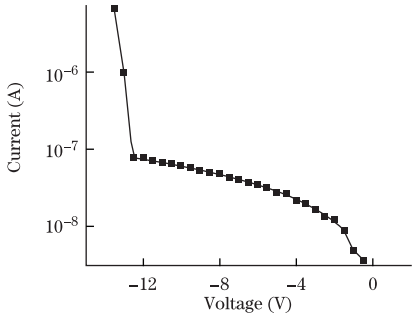

Fig. 3. Reverse bias SPAD behavior.

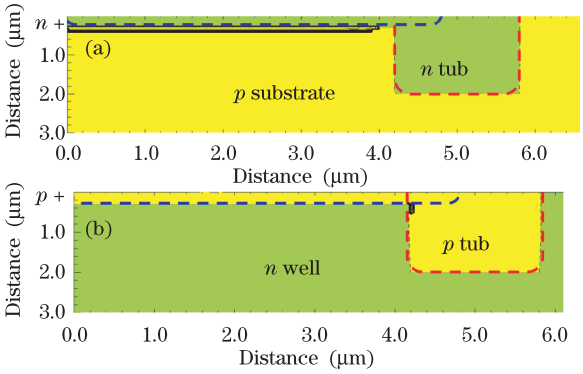

Fig. 4. (Color online) Tunneling contours in (a) NTGR and (b) PTGR SPADs.

generation rate of 1×10^{10} pairs/(s·cm^3) is reached in the PTGR SPAD simulation but only at the edges of the interface between p+ and the guard ring.

Tunneling DCR can be calculated with

$$\mathrm{DCR_{tunneling}} = \mathrm{DCR_{BTBTtunneling}} + \mathrm{DCR_{trapassissted}}, \quad (4)$$

where the values of trap-assisted tunneling and BTBT are derived from

$$\mathrm{DCR_{trapassisted}} = S \cdot \int_{Z_0}^{Z_w} P_p(z) G_{\mathrm{trapassissted}}(z)\mathrm{d}z, \quad (5)$$

$$\mathrm{DCR_{BTBTtunneling}} = S \cdot \int_{Z_0}^{Z_w} [G_{\mathrm{BTBTtunneling}}(z) \cdot P_p(z)]\mathrm{d}z, \quad (6)$$

where S is the surface between the n and p regions, Z_0 and Z_w are the start and end points of the depletion region, respectively, $P_p(z)$ is the probability of avalanche initiation by an electron-hole pair at a given depth z, $G_{\mathrm{BTBTtunneling}}(z)$ is the BTBT generation rate, and $G_{\mathrm{trapassissted}}(z)$ is the trap-assisted generation rate[12]. Trap-assisted tunneling is calculated by equation sets presented in Ref. [12] in this study. The direct BTBT generation rate is calculated by

$$G_{\mathrm{tunneling}}(z) = B.|\xi(z)|^{5/2} \cdot D \cdot \exp\left[\frac{-\xi_0}{|\xi(z)|}\right], \quad (7)$$

where the B factor is 4×10^{14} cm$^{-0.5}$V$^{-2.5}$s^{-1}, ξ_0 is 1.9×10^7 Vcm^{-1}, and D is unity, with the exception of the depletion-region edges (where it is 0, and $\xi(z)$ is below the electric field[13]). BTBT is calculated only for NTGR SPADs because BTBT generation occurred only at the edges of the guard ring in the PTGR SPADs. Figure 5 shows the electric field distribution in the NTGR structures as applied in Eq. (7) as ζ(z). The following coupled equation must be solved to obtain $P_p(z)$[13]:

$$\begin{cases} \frac{\mathrm{d}P_e}{\mathrm{d}x} = (1-p_e)\alpha_e[P_e + P_h - P_eP_h] \\ \frac{\mathrm{d}P_h}{\mathrm{d}x} = -(1-p_h)\alpha_h[P_e + P_h - P_eP_h] \end{cases}, \quad (8)$$

where P_e and P_h are the probabilities of avalanche initiation by an electron and a hole, respectively, and α_e and α_h are the electron and hole ionization coefficients. The probability of avalanche initiation by an electron-hole pair is calculated from P_e and P_h with the use of

$$P_p(z) = P_e(z) + [1 - P_e(z)] \cdot P_h(z). \quad (9)$$

Figure 6 shows P_e, P_h, and P_p with 1.4 V of excess bias voltage at different locations in the z direction, as calculated with Eqs. (7) and (8).

Figure 7 depicts the tunneling count rate calculated by Eqs. (4)-(7) for the NTGR structures in different excess bias voltages. Figure 8 displays the DCR measurements of the SPADs in various excess bias voltages and at different temperatures. The slight difference between the DCR curves at various temperatures is another sign of tunneling domination in DCR because DCR is less dependent on temperature.

Table 1 summarizes the performance of the new NTGR

SPAD that was presented in this letter and that has an active area diameter of 10 μm. The high jitter in NTGR structures can be attributed to red and infrared photon absorption deep in the substrate. This absorption results in a long photogenerated-carrier travelling time. High photon detection probability (PDP) may be the result of a lack of deep-well usage in NTGR structures. Therefore, photon absorption is not confined to deep wells.

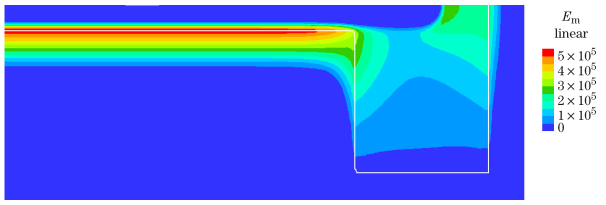

Fig. 5. (Color online) Electric field distribution of the NTGR structure at 1.4 V of excess bias voltage.

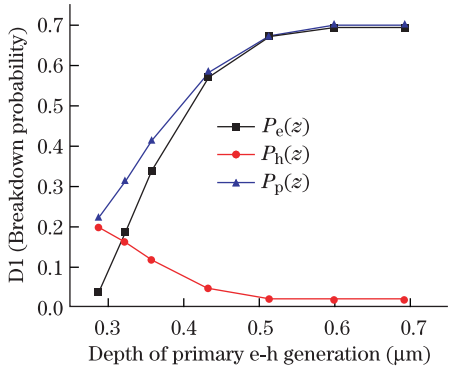

Fig. 6. (Color online) P_e, P_h, and P_p as functions of z at 1.4 V of excess bias voltage.

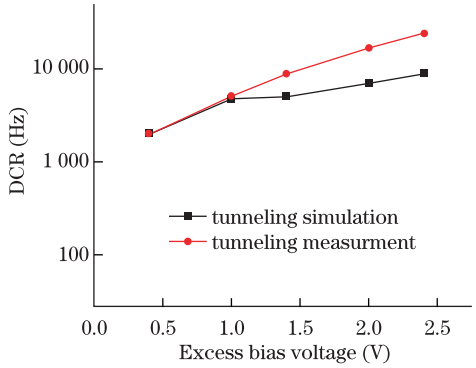

Fig. 7. (Color online) Tunneling noise in NTGR structures at different excess bias voltages at room temperature.

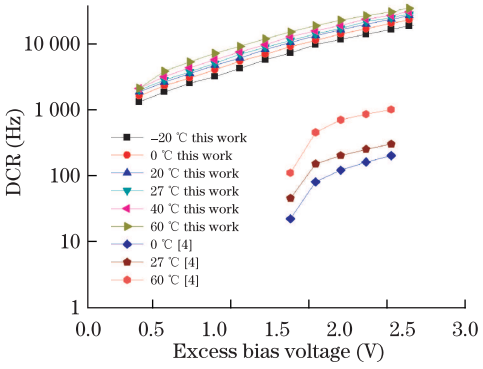

Fig. 8. (Color online) DCR behavior of SPADs at different excess bias voltages and temperatures.

Table 1. Comparison of NTGR and PTGR SPADs

Performance	This Work (NTGR)	PTGR[4]	Comments
DCR	10 kHz	11 Hz	At 1.5 V Excess Bias Voltage and at Room Temperature
PDP	43%	40%	Maximum PDP
Timing Jitter (FWHM)	152 ps	80 ps	At 405-nm Wavelength Illumination
Afterpulse Probability	25%	23%	At the Nominal Dead Time
V_{br}	13.6 V	17.7 V	Breakdown Voltage at Room Temperature

In conclusion, the tunneling effects in two main SPAD topologies used in planar technologies and notably in most CMOS processes are evaluated. Device simulations that are supported by $I-V$ measurements, as well as DCR calculations and measurements, demonstrate higher tunneling than PTGR structures because of certain doping profiles in NTGR SPADs.

SPAD realizations and simulations were performed by the group of Professor E. Charbon of TU Delft, the Netherlands. The authors are grateful for his support.

References

1. M. A. Karami, L. Carrara, C. Niclass, M. Fishburn, and E.Charbon, IEEE Electron Device Lett. **31,** 692 (2010).
2. M. A. Karami, M. Gersbach, H. J. Yoon, and E. Charbon, Proc. SPIE **7780,** 77801F (2010).
3. A. Rochas, M. Gosch, A. Serov, P. A. Besse, R. S. Popovic, T. Lasser, and R. Rigler, IEEE Photon. Technol. Lett. **15,** 963 (2003).
4. C. Niclass, M. Sergio, and E. Charbon, Proc. SPIE **6372,** 63720S (2006).
5. N. Faramarzpour, M. J. Deen, S. Shirani, and Q. Fang, IEEE Trans. Electron Dev. **55,** 760 (2008).
6. M. Gersbach, "Single-Photon Detector Arrays for Time-Resolved Fluorescence Imaging" PhD. Thesis (École Polytechnique Fédérale De Lausanne, 2009).
7. R. K. Henderson, J. Richardson, and L. Grant, in *Proceedings of International Image Sensor Workshop* 26 (2009).
8. A. Goetzberger, B. Mcdonald, R. H. Haitz, and R. M. Scarlett, J. Appl. Phys. **34,** 1591 (1963).
9. A. Lacatia, M. Ghioni, and S. Cova, Electron. Lett. **25,** 841 (1989).
10. R. F. Pierret, *Semiconductor Device Fundamentals* (Addison-Wesley Publication Company, Boston, 1996).
11. E. O. Kane, J. Phys. Chem. Solids **12,** 181 (1960).
12. A. Rochas, "Single Photon Avalanche Diodes in CMOS technology" PhD. Thesis (École Polytechnique Fédérale De Lausanne, 2003).
13. W. G. Oldham, R. S. Samuelson, and P. Antognetti, IEEE Trans. Electron Dev. **19,** 1056 (1972).