# Design and implementation of real-time high definition aerial camera based on ADSP-BF561

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To meet application requirements of high resolution and high frame rate for the aerial camera, a real-time high definition (HD) aerial camera imaging system is designed and developed. A KAI-01050 charge-coupled device (CCD), ADSP-BF561, and AD9920A are used in the system. ADSP-BF561 is used to configure registers of AD9920A for generating the timing-driven signals to meet CCD parameter needs, and image stitching through ping-pong operation of collected video signals is achieved, then the image is displayed correctly. In the end, the system is developed, 1 M pixels and 60 frame rate are realized, and running results on the system verify effectiveness of the design program.

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Charge coupled devices (CCD) sensor integrates the photo-electric conversion, store and transfer charge. Because of its many advantages, includeing small size, strong anti-interference, high resolution, good stability, small measurement errors, CCD is widely used in various imaging systems[1]. In practical application, the aerial camera capture stationary objects moving target requires high resolution and high frame rate, respectively, so the frame rate and resolution is the key indicators of the aerial camera application. In this letter, we used Kodak's high performance area array interline transfer (KAI-01050) as CCD image sensor, based on the ADI's dual-core digital signal processor (DSP) and high-performance analog- front-end (AFE) devices (AD9920A), designed and implemented 1 M pixels, 60-Hz high definition real-time aerial camera, and gave the each test results of the system.

The development of aerial camera can be dated back to the middle of 1970s. ITEK's company tried to adapt the type film KA-102 camera into CCD camera and film KA-102A/EO. This was the first generation mechanical reconnaissance CCD camera, which was with linear CCD device and push-broom way of working. Since then, aerial cameras get the further development, as more and more kinds of camera plus performance improving, long focal length, wide spectral, large field, high resolution, and high autoimmunization are the developing direction of modern aerial camera[2−5].

At present, there are two methods of obtaining high resolution and high frame CCD image. One is to adopt multiple high speed and small area CCD simultaneously acquire, implement carring a CCD through optical assembly or the output image by software joint. The other is to utilize single big CCD imaging, CCD signal at the same time multiple-channeled output carried it out. Because the difference of CCD field angle and image quality influence, the former method increased the treatment time. However, the latter one ensured the high resolution in the premise of raising frame frequency.

Block diagram of CCD imaging system is shown in Fig. 1. It mainly consist of the CCD image sensor, CCD timing control and analog-digital conversion module, DSP control module, video output module, etc. When system worked, the object image was through the optical system and project in light-sensitive array of CCD image sensor, which converted optical signal into charge signal; and then under the control of the drive timing pulse, the image pixel charge signal was followed out and amplified into two-channel analog signals with different voltage amplitudes, this two-channel signals were sent to the two analog-digital conversion chips AD9920A separately. Lastly, AD9920A output 12-bit parallel digital signal which converted by the AFE of the analog-to-digital (A/D) converter. ADSP-BF561 stitched the two digital image signals which is collected by PPI0 and PPI1 interfaces, and ultimately stored in the SDRAM, or via HDMI Interface displayed[6].

Kodak's KAI-01050 was used in this system for image sensor. KAI-01050 is a million effective pixel interline-transfer area array CCD, which has a flexible readout

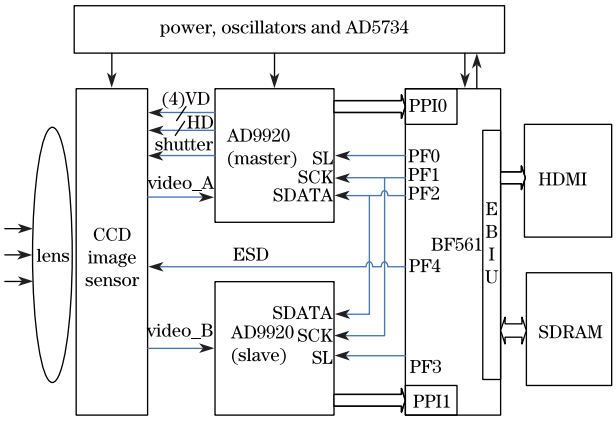



Fig. 1. Block diagram of CCD imaging system.

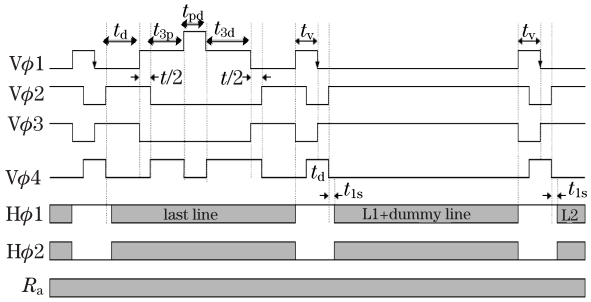



Fig. 2. Photodiode transfer timing.

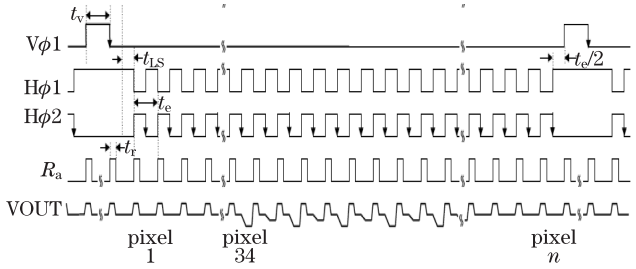



Fig. 3. Line and pixel timing.

architecture, high frame rate, high sensitivity, low noise, and electronic shutter function. The main parameters of KAI-01050 are as follows[7]: 1) maximum pixel clock speed: 40 MHz; 2) optical format: 0.5 inch; 3) number of active pixels: 1 024 (H)×1 024 (V); 4) maximum frame rate: single output for 30 Hz, dual output for 60 Hz, quad output for 120 Hz.

The main role of the CCD control circuit is that the optical signal is transformed into electrical signals. The timing-driven of CCD is shown in Figs. 2 and 3. The specific process of imaging includes the following steps: 1) under the control of the electronic shutter pulse, the light signals were converted into electric charge and stored by photosensitive element in photosensitive area; 2) under the control of the vertical timing- driven of charge transfer, the charge is transferred from photosensitive area to vertical storage area; 3) under vertical timing-driven of line transfer, the charge of vertical storage unit downward shift to the level storage unit, each transfer is done only within each horizontal blanking interval, and only one pixel charge is shifted by each memory of vertical column. It ensure that each level memory unit has only one row of pixels charge after each transfer; 4) under control of horizontal timing-driven, charge which has been transferred into level memory sequentially was shifted to an amplifier and then outputted voltage signal.

The high performance dual-core DSP processor ADSP-BF561 is used in this system as the control chip, which is new generation production of ADI. The ADSP-BF561 processor is a high performance member of the Blackfin family of products targeting a variety of multimedia, industrial, and telecommu-nications applications. At the heart of this device are two independent analog devices blackfin proce-ssors. ADSP-BF561 integrates a set of general purpose digital image processing peripherals, so it can create complete digital image processing and multimedia applications on-chip system-level solutions[8,9].

Its main features are as follows: 1) dual symmetric 600 MHz high performance Blackfin cores, 328 Kbytes of on-chip memory; 2) two 16-bit MACs, two 40-bit ALUs, four 8-bit video ALUs, 40-bit shifter; 3) RISC-like register and instruction model for ease of programming and compiler-friendly support; 4) 0.8 to 1.35-V core VDD with on-chip voltage regulator, 2.5 and 3.3 V compliant I/O; 5) two parallel input/output peripheral interface units supporting ITU-R 656 video and glueless interface to analog front end DCs; 6) two dual channel, full duplex synchronous serial ports; 7) dual 12-channel DMA controllers (supporting 24 peripheral DMAs), four memory-to-memory DMAs; 8) 12 general-purpose 32-bit timers/counters with PWM capability; 9) 48 programmable flags (GPIO); 10) external memory controller with glueless support for SDRAM, mobile SDRAM, SRAM, flash.

Analog Devices's AD9920A is used as the chip of timing and A/D converter. The AD9920A is a highly integrated CCD signal processor for digital still camera applications. It includes a complete AFE with A/D conversion, combined with a full-function programmable timing generator and 19-channel vertical driver (V-driver). The AFE includes black level clamping, variable gain CDS, and a 12-bit ADC. The timing generator is capable of supporting up to 24 vertical clock signals to control advanced CCDs. The AD9920A also contains six GPOs that can be used for shutter and system functions[10].

ADSP-BF561 via 3-wire serial interface (SDATA, SCK, SL) to configure AD9920A registers. AD9920A configuration mainly included driving signal waveform, GPO outputting signals, CDS setting the sampling signal, variable gain amplifier, clamp level, horizontal and vertical sync signals etc. The timing-driven was generated by timer of AD9920A for KAI-01050, which controlled output of CCD charge; CCD analog video signal was amplified by emitter-follower to AD9920A, eliminated noise by the correlated double sampling, and then through variable gain amplifier (VGA) was send to the 12-bit ADC, then was converted into digital video signal, ultimately send to the ADSP-BF561 for further processing.

The thesis introduces the software development process based on Visual DSP++, which integrated development environment of ADI. Software program included DSP's initialization, AD9920A's configu- ration, the video image stitching etc[11]. Flowcharts of system software is shown in Fig. 4.

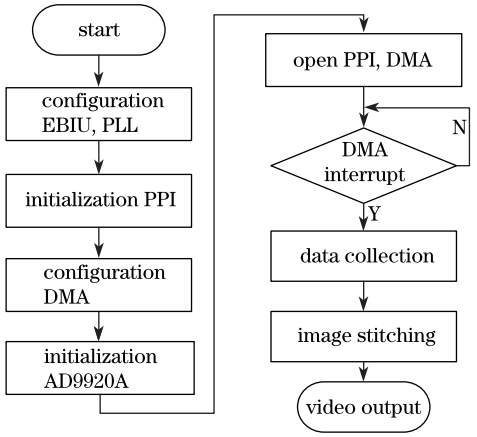



Fig. 4. Software processes of CCD imaging system.

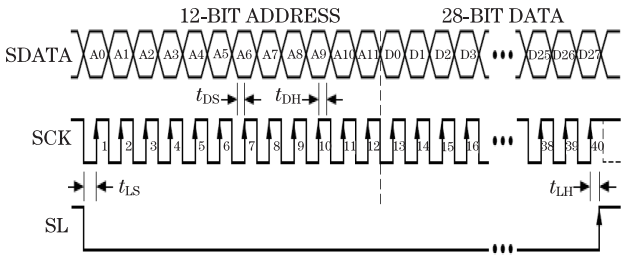



Fig. 5. Serial write operation.

Specifically process includes 1) system initialization includes: EBIU, PLL, SDRAM, PPI port, and DMA configuration. Within these PPI interface model was written through PPI_CONTROL, PPI_DELAY and PPI_COUNT registers; 2) AD9920A configuration: DSP calls subroutine of AD9920A's configuration to set AD9920A's register, which can enable AD9920A to generate CCD drive timing pulse; 3) turn on PPI and DMA: DSP check that the DMA channel is free or not. If the DMA channel is free, DSP enable PPI interface and DMA channels to receive data after HD pulse; 4) image stitching: two-way video data that were collected by the PPI interface and sent to internal memory of DSP, then stitched this two-way data by DSP and output to SDRAM or displayed by the HDMI interface.

In order to realize the various kind functions of the chip AD9920A, it is need to configure its internal register correctly. A 3-wire serial interface (SDATA, SCK, SL) is used to configure the internal register, and there are two configuration methods: serial write operation and continuous serial write operation. In this system, continuous serial write operation method was used; the operation sequence is shown as Fig. 5. Due to there are some default values of the register in AFE of AD9920A, according to the system demand, just part of the values of the register need to set. Configure of AD9920A must be written strictly with the three line serial write operation timing, specifically as follows: data start to write in low level of SL; write one bit data (SDATA) at each clock (SCK) rising edge; continuously write 12-bit address signals and 28-bit data signals; data (SDATA) should be latched at the rising edge of SL.

For completing each register's configuration of AD9920A, the two-way programmable PF interface of ADSP-BF561 is used in programming realization process to simulate the timing of the three line serial interface. We configured the corresponding pins to output mode individually by the direction flag register, and different values were set for FIO_FLAG_S and FIO_FLAG_C in order to definite output state (high or low) of these pins. In the program design, the configuration of programmable flags memory-mapped register of PF interface can be used to do simulation. First, putting the address signals and data signals packed into a 40-bit array, and then using the data in circulation program written into AD9920A register serially, that is the way which can complete the configuration of chip AD9920A.

This system required the frame rate of 60 Hz, according to the CCD parameters; it needs to send 2-way parallel CCD images simultaneously to achieve. The diagram of CCD pixel output is shown in Fig. 6, the output of first way image data and second way image data are the mirror in the horizontal direction which can be seen from Fig. 6. Therefore, the second way image needs to be corrected, so that it ensures the output image in order, and stitch in the back of first way image, eventually a complete 60-Hz sequence of video images could be obtain.

In the process of real-time video capture, the video data of collection, transmission and stitching should be executed in parallel. Through PPI0 and PPI1 interfaces capture the video data input to the ADSP-BF561 internal data store at the same time, and then stitching completes the display via HDMI output. In order to achieve this process, the ADSP-BF561 sets two buffers each PPI channel for storing 2-line video data, and accomplishes correction and stitching of video data by ping-pong operation. The schematic of ping-pong operation is shown in Fig. 7, and its specific ideas and processes of implementation is as follows: 1) first way is video data stored in Buffer A and Buffer B, and second way is video data stored in Buffer C and Buffer D, each Buffer only stores one line video data; 2) the number $N$ line video data of first and second ways are differently written in Buffer A and Buffer C, at same time the number $N-1$ line video data of first and second ways are differently read out form Buffer B and Buffer D for stitching and output; 3) similarly, the number $N+1$ line video data of first and second ways are differently written in Buffer B and Buffer D, at same time the number $N$ line video data of first and second ways are differently read out form Buffer A and Buffer C, stitching and output; 4) note the outputs of first and second way image data are mirrored. So, when reading Buffer C and Buffer D video data of the second way, it is needed to read from high to low order.

Through the development of hardware circuit debugging, the hardware fault is eliminated and each program experiment validated is written. Plus configured each register of the AD9920A, according to the test, the CCD drive signal timings are in line with the parameters of the KAI-01050 requirements. Figure 8 shows the CCD

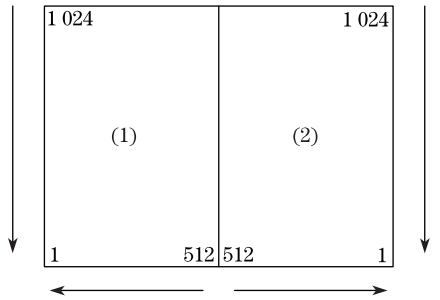



Fig. 6. CCD camera output sequence.

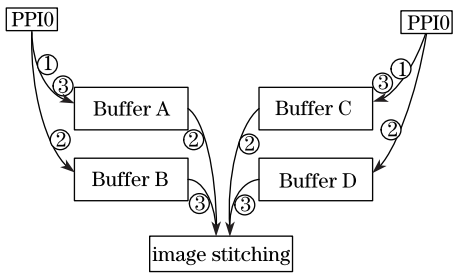
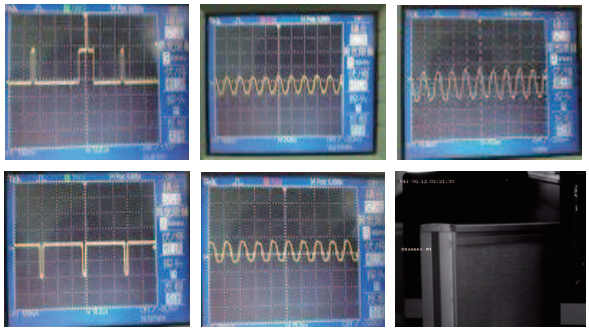



Fig. 7. Schematic diagram of ping-pong operation.



(a) (b) (c)

Fig. 8. CCD drive signal and output video signal. (a) Vertical drive signal; (b) horizontal drive signal; (c) output video image.

drive timing signal which is tested by oscilloscope and the actual output of the video image. Figure 8(a) is the measured vertical drive signal waveform (upper picture shows the V1, the next picture shows the V2), Fig. 8(b) is the horizontal drive signal waveform (upper picture shows the H1, the next picture shows the H2), Fig. 8(c) is the actual output for the CCD the analog video signal waveform and video display image (upper picture shows the analog video signal waveform, the next picture shows the encoded output video via HDMI interface displays).

In conclusion, based on Kodak's high performance area array interline transfer type KAI-01050 as CCD image sensor, ADI's high performance dual-core ADSP- BF561 DSP chip as the master core, and ADI's AD9920A as the timing and A/D conversion chip, we successfully design an image collection system with high frame rate and high resolution. Results of experiments and test show this system designed reasonable, hardware circuit is reliable, drive timing signals meet the design requirements, which can capture real-time digital video signal with 1-M pixels and 60 Hz. The system has high frame frequency, high practical value, and high resolution imaging effect etc, which meet the market requirements of aerial camera.

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